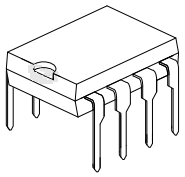
UC3848

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE CONTROLLERS



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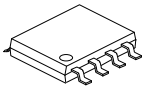


SOP-8

■ DESCRIPTION

The UTC **UC3848** is designed to provide several special enhancements to satisfy the needs, for example, Power-Saving mode for low standby power (<0.3W), Frequency Hopping , Constant Output Power Limiting , Slope Compensation ,Over Current Protection (OCP), Over Voltage Protection (OVP), Over Load Protection (OLP), Under Voltage Lock Out (UVLO), Short Circuit Protection (SCP) , Over Temperature Protection (OTP) etc. IC will be shutdown or can auto-restart in situations.

■ FEATURES

* Low Startup Current (about 22μA)
* Fixed Switching Frequency(Norm. is 68KHz)
* Frequency Hopping for Improved EMI Performance.
* Lower than 0.3W Standby Power Design
* Linearly Decreasing Frequency to 26KHz During Light Load
* Soft Start
* Internal Slope Compensation
* Constant Power Limiting for Universal AC input Range
* Gate Output Maximum Voltage Clamp(15V)
* Max Duty Cycle 74%
* Over Temperature Protection
* Overload Protection
* Over Voltage Protection
* Leading Edge Blanking
* Cycle-by-Cycle Current Limiting
* Under Voltage Lock Out
* Short Circuit Protection

■ ORDERING INFORMATION

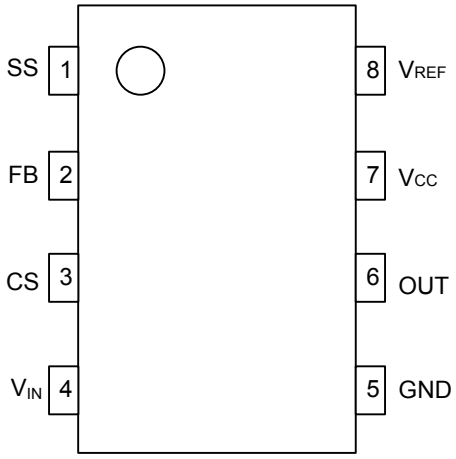
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3848L-D08-T	UC3848G-D08-T	DIP-8	Tube
UC3848L-S08-R	UC3848G-S08-R	SOP-8	Tape Reel

UC3848L-D08-T

(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) D08: DIP-8, S08: SOP-8
(3) L: Lead Free, G: Halogen Free

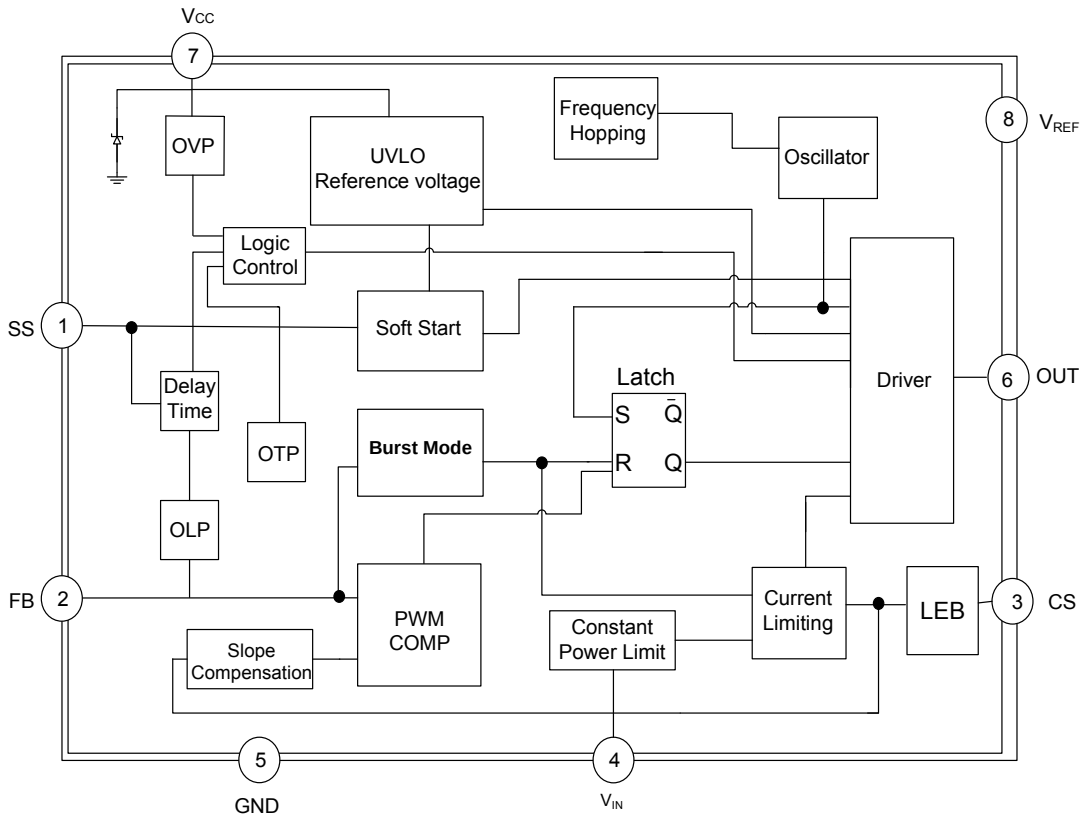
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	SS	Soft-start
2	FB	Feedback
3	CS	Controller current sense input
4	V_{IN}	Connected R_{VIN} to line voltage compensating V_{CSTH}, and providing constant output power limiting for universal AC input Range
5	GND	Ground
6	OUT	Output to the gate of external power MOS
7	V_{CC}	Supply voltage
8	V_{REF}	Inter Reference Voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	30	V
Input Voltage to V_{IN} Pin	V_{IN}	30	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 6.2	V
Input Voltage to CS Pin	V_{CS}	-0.3 ~ 2.8	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	8.2 ~ 22	V

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
Start Up Current		I_{STR}	$V_{CC}=V_{THD(ON)}$-0.1V		22	45	μA
Supply Current with switch	OFF	I_{OFF}	V_{SS} = 0, I_{FB} = 0		7	9	mA
	ON	I_{ON}	V_{SS} = 5V, I_{FB} = 0		7	9	mA
UNDER-VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage		$V_{THD(ON)}$		13.5	14.2	15	V
Min. Operating Voltage		$V_{CC(MIN)}$		7.5	8.2	9	V
Hysteresis		$V_{CC(HY)}$			6		V
INTERNAL VOLTAGE REFERENCE							
Reference Voltage		V_{REF}	Measured at pin V_{REF}	6.3	6.5	6.7	V
CONTROL SECTION							
V_{FB} Operating Level		V_{MIN}		0.5			V
		V_{MAX}				4.4	V
Burst-Mode Enter FB Voltage		V_{FB-IN}	V_{CS}=0		1.5		V
Reduce-Frequency end FB Voltage		V_{FB-END}	V_{CS}=0		1.6		V
Burst-Mode Out FB Voltage		V_{FB-out}	V_{CS}=0		1.7		V
Switch Frequency	Normal	$F_{(SW)}$	V_{FB} = 4V	61	68	75	kHz
	Power-Saving		Before enter burst mode	20		40	kHz
Duty Cycle		D_{MAX}	V_{FB}=4.4V,V_{CS}=0	68	74	80	%
		D_{MIN}	V_{FB} < 0.5V	0			%
Feedback Resistor		R_{FB}	V_{FB} =0V	16	21	26	kΩ
Soft-Start Time		T_{SS}	C_{SS}=0.47uF	9.9	11.2	12.6	ms
PROTECTION SECTION							
OVP threshold		V_{OVP1}	V_{SS} < 3.5V, V_{FB} > 5V		19		V
		V_{OVP1}	V_{SS}=4.8V,V_{FB}=3V		28		
OLP threshold		$V_{FB(OLP)}$	V_{CS} > 0V, SS Open	4.7	4.9	5.1	V
Delay Time Of OLP		T_{D-OLP}	C_{SS}=0.47uF	55	62	70	mS
OTP threshold		$T_{(THR)}$		120	135	150	°C
OVP Disable threshold		$V_{SS(DEACT)}$	V_{FB} > 5V, V_{CC}=22V	3.9	4.1	4.3	V
OLP Enable threshold		$V_{SS(ACT)}$	V_{FB} > 5V	5.1	5.4	5.7	V
CURRENT LIMITING SECTION							
LEB		t_{LEB}			220		ns
Peak Current Limitation		V_{CS}	V_{FB}=4.4V		0.86	1	V
Threshold Voltage For I_{VIN}=60uA		$V_{SENSE-L}$	I_{VIN}=60uA		0.77		V
DRIVER OUTPUT SECTION							
Output Voltage Low State		V_{OL}	I_{SOURCE} = 200 mA			2.5	V
Output Voltage High State		V_{OH}	I_{SINK} = 200 mA	12.2			V
Output Voltage Rise Time		t_R	C_L = 1.0 nF		200	300	ns
Output Voltage Fall Time		t_F	C_L = 1.0 nF		50	90	ns

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at V_{CC} > $V_{THD\ (ON)}$, and shutdown at V_{CC} < $V_{CC\ (MIN)}$.

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by voltage V_{SS} on soft-start capacitor and V_{CS} on current sense resistor at beginning. After V_{SS} reach 4.2V, the whole soft-start phase end, and driver duty cycle depend on V_{FB} and V_{CS}. The relation among V_{SS}, V_{FB} and V_{OUT} as followed FIG.3.

Furthermore, soft-start phase should end before V_{CC} reach $V_{CC\ (MIN)}$ during V_{CC} power on. Otherwise, if soft-start phase remain not end before V_{CC} reach $V_{CC\ (MIN)}$ during V_{CC} power on, IC will enter auto-restart phase and not set up V_{OUT}. So the value of C_{SS} should be between 0.1μFand 4.7μF.

Finally soft-start also set OVP1 active phase. OVP1 active phase between 0 and $V_{SS(DEACT)}$, OVP1 will not be sensed after V_{SS} reach $V_{SS(DEACT)}$.The Soft-start phase T_{SS}：T_{SS} = 23.8×C_{SS} (ms) (Example: C_{SS}=0.47μF, then T_{SS}=23.8×0.47=11.2ms).

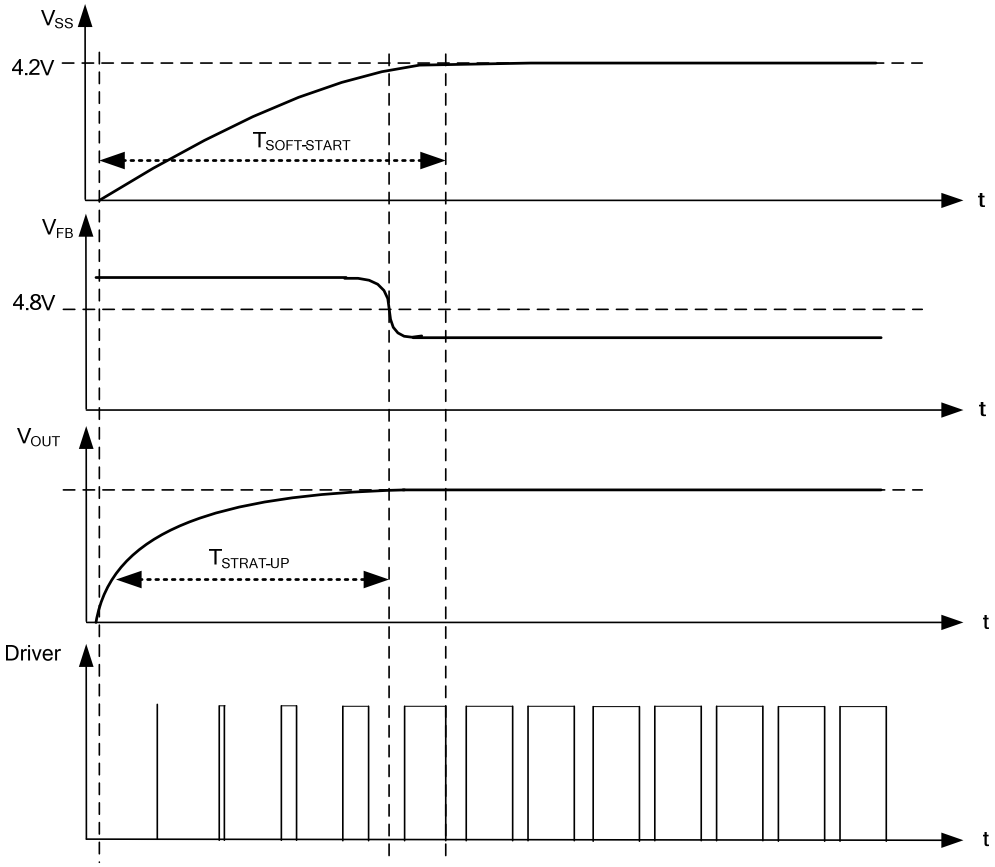


FIG.3 Soft-start phase

■ FUNCTIONAL DESCRIPTION(Cont.)

(2) Switch Frequency Set

The maximum switch frequency is set to 68kHz. Switch frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the subber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT\ (MAX)}$ as followed FIG.4.

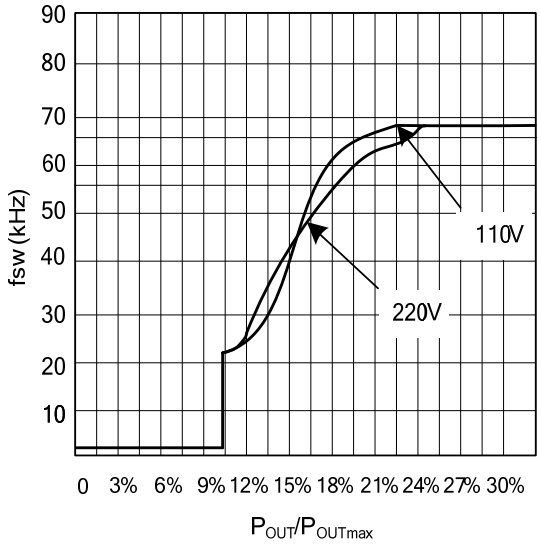


FIG.4 The relation curve between f_{SW} and relative output power $P_{OUT}/ P_{OUT\ (MAX)}$

(3) Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

■ FUNCTIONAL DESCRIPTION(Cont.)

(4) Frequency Hopping For EMI Improvement

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed FIG.5. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

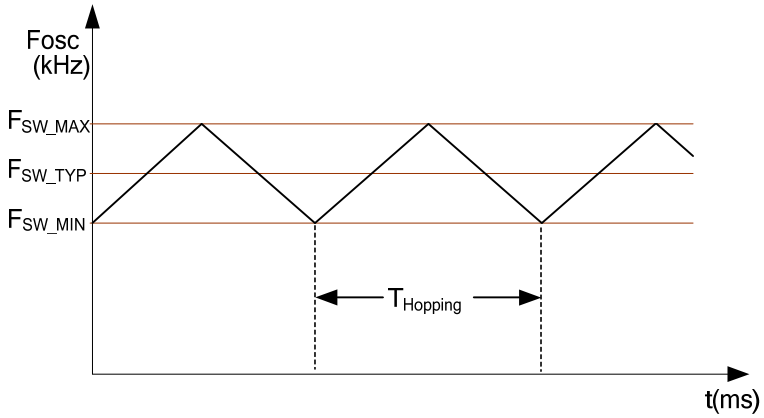


FIG.5 Frequency Hopping

(5) Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_S, reaches the threshold voltage, around 0.8V, the output GATE drive will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the V_{IN} current. Since V_{IN} pin is connected to the rectified input line voltage through a resistor R_{VIN}, a higher line voltage will generate higher V_{IN} current into the V_{IN} pin. The threshold voltage is decreased if the V_{IN} current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

(6) Driver Output Section

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 15V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

(7) Protection section

The IC takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart, V_{CC} power on and driver is reset after V_{CC} power on again.

OTP

OTP will shut down driver when junction temperature $T_J > T_{(THR)}$ for continual a blanking time.

■ FUNCTIONAL DESCRIPTION(Cont.)

(7)Protection section (Cont.)

OLP

After soft-start phase end, IC will shutdown driver if over load state occurs for continual T_{D-OLP}. OLP function will not inactive during soft-start phase. OLP case as followed FIG. 6. The test circuit as followed FIG.8. $T_{D-OLP}=5.53\times T_{SS}$.

OVP

There are two kinds of OVP circuits, the first OVP function are enabled only when $V_{SS}<V_{SS\ (DEACT)}$ & $V_{FB}>V_{FB(OLP)}$ during soft-start phase. During above condition, driver will be shutdown if over voltage state occurs ($V_{CC}>V_{OVP1}$) for continual a blanking time. The first OVP function will not inactive after soft-start phase. The second OVP will shutdown the switching of the power MOSFET whenever $V_{CC}>V_{OVP2}$. The first OVP case as followed FIG.7. The test circuit as followed FIG. 9.

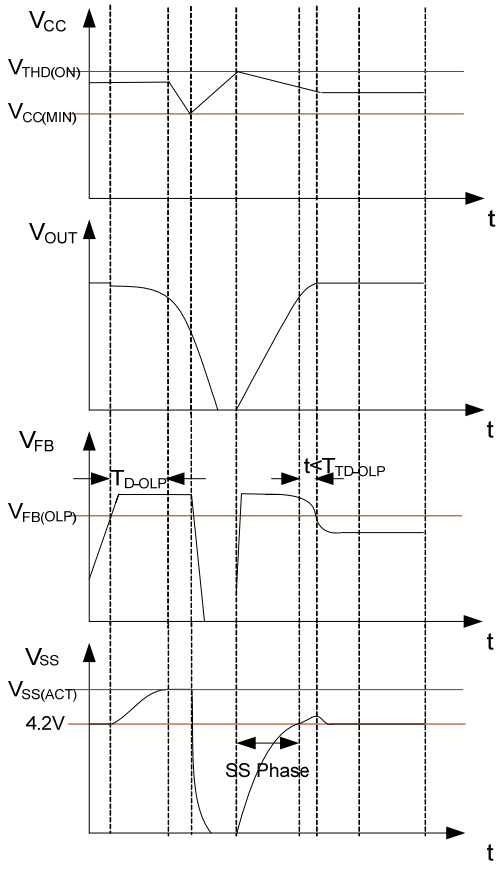


FIG.6 OLP case

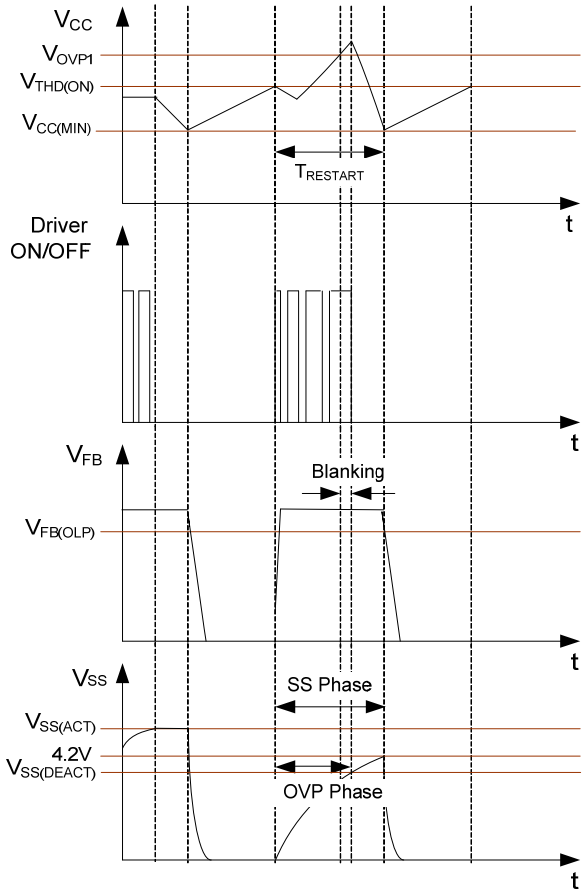


FIG.7 OVP case

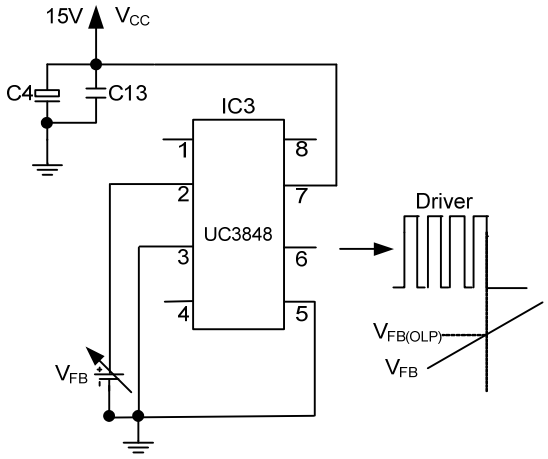


FIG.8 OLP test circuit

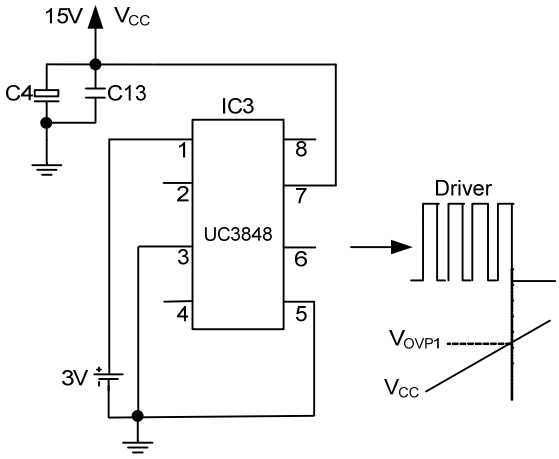


FIG.9 OVP test circuit

■ TYPICAL APPLICATION CIRCUIT

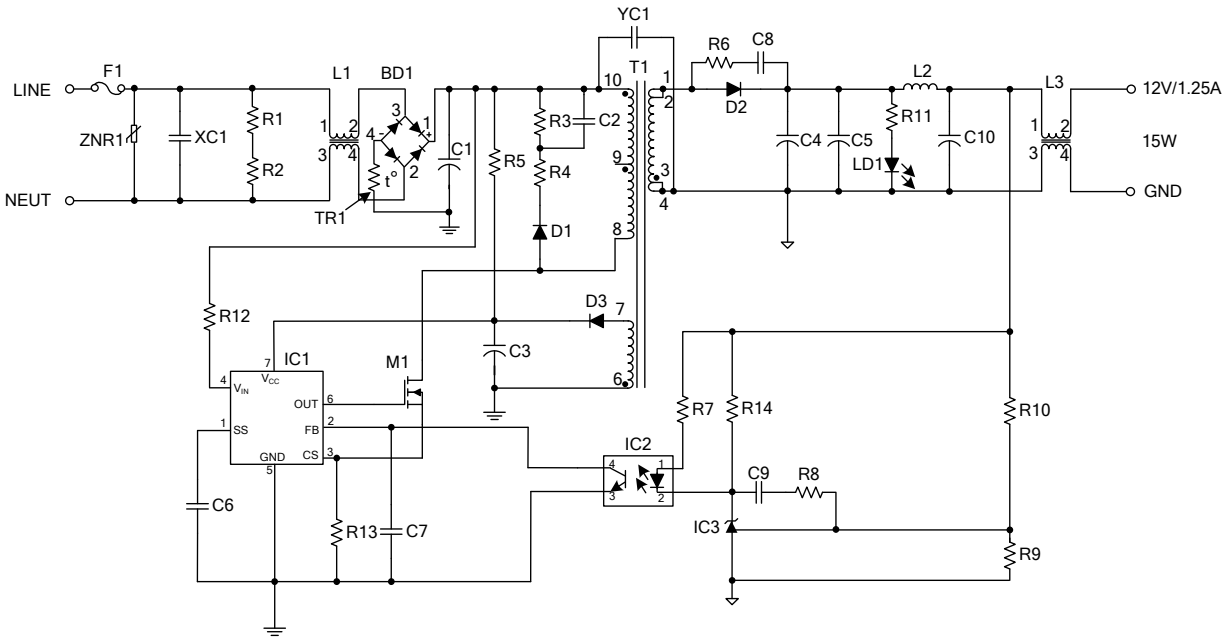


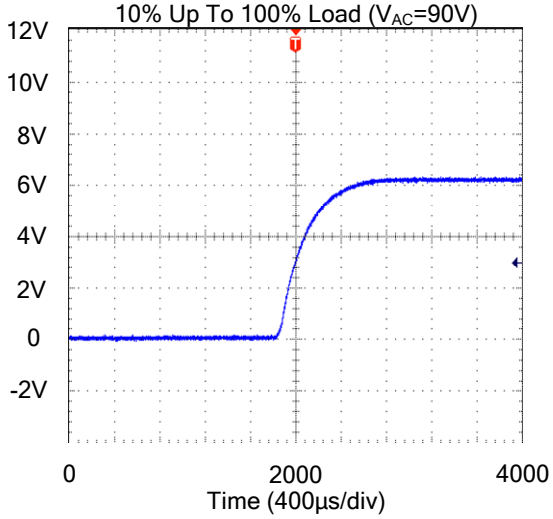
FIG.12 UC3848 Typical Application Circuit

Table1 Components Reference description for UC3848 application circuit

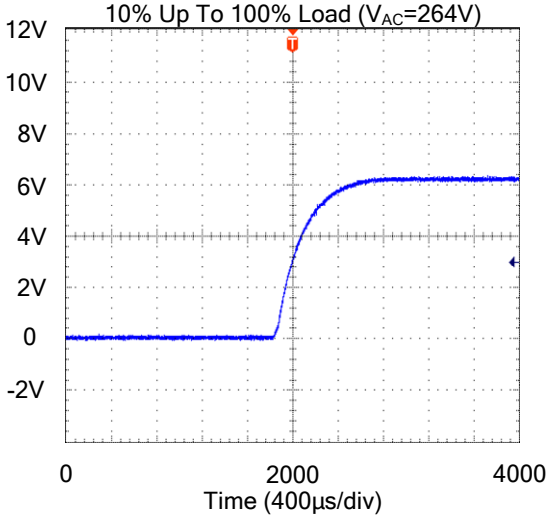
DESIGNATOR	PART TYPE		DESIGNATOR	PART TYPE		DESIGNATOR	PART TYPE
C1	33μF		R1	2.2MΩ		D1	FR107
C2	0.001μF		R2	2.2MΩ		D2	SB5100
C3	22μF		R3	68KΩ		D3	RS1D
C4	470μF		R4	100Ω		IC1	**UC3848**
C5	470μF		R5	1MΩ		IC2	PC-817
C6	0.1μF		R6	15Ω		IC3	TL431
C7	0.01μF		R7	560Ω		YC1	222
C8	0.001μF		R8	1KΩ		T1	EE25
C9	0.1μF		R9	3.9KΩ		L1	UU10.5
C10	220μF		R10	15KΩ		L2	2μH
			R11	10KΩ		L3	Ring Choke
			R12	1.5MΩ~4MΩ		LD1	LED
			R13	1.0Ω		F1	2A/250V
			R14	1.8KΩ		ZNR1	7D471K
						TR1	SCK102R55A
						XC1	334/275V
						BD1	KBP205

■ TYPICAL CHARACTERISTICS

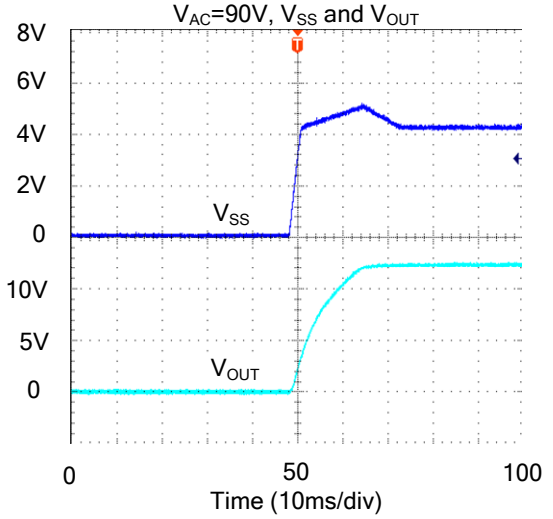
Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{AC}=90V)



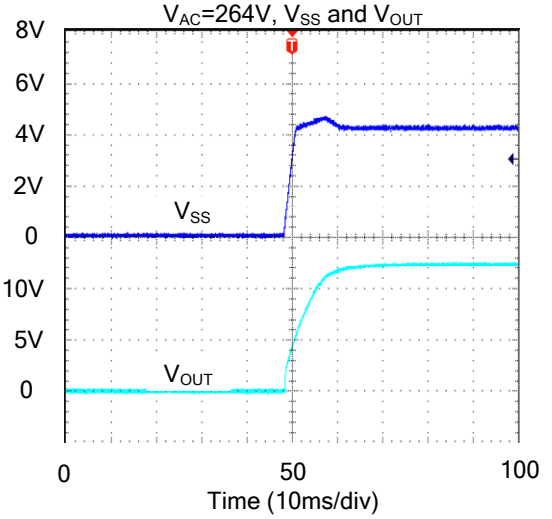
Feedback Voltage During Loadjump From 10% Up To 100% Load (V_{AC}=264V)



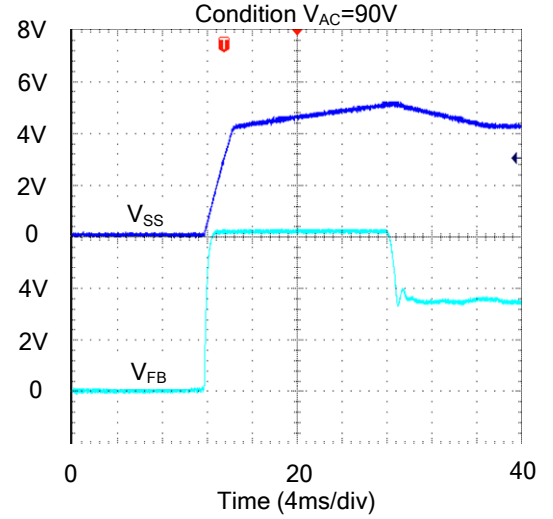
Startup With Full Load Condition at V_{AC}=90V, V_{SS} and V_{OUT}



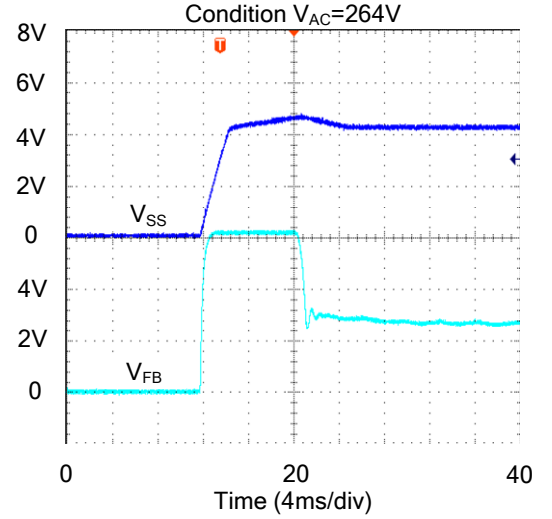
Startup With Full Load Condition at V_{AC}=264V, V_{SS} and V_{OUT}



Startup Behavior At Nominal Load Condition V_{AC}=90V



Startup Behavior At Nominal Load Condition V_{AC}=264V



■ TYPICAL CHARACTERISTICS(Cont.)