

Memory FRAM

2 M (256 K × 8) Bit SPI

MB85RS2MTA

■ DESCRIPTION

MB85RS2MTA is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 262,144 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

MB85RS2MTA adopts the Serial Peripheral Interface (SPI).

The MB85RS2MTA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS2MTA can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

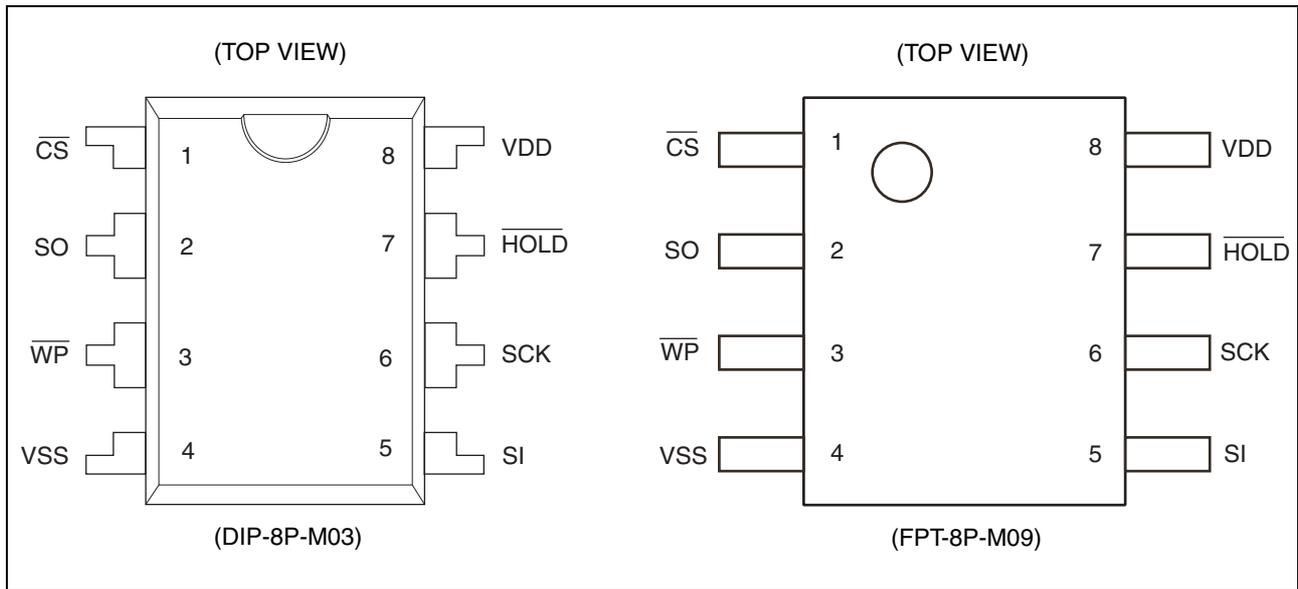
MB85RS2MTA does not take long time to write data like Flash memories or E²PROM, and MB85RS2MTA takes no wait time.

■ FEATURES

- Bit configuration : 262,144 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 40MHz (Max)
- High endurance : 10^{13} times / byte
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption :
Operating power supply current 2.3mA (Max@40 MHz)
Standby current 50 μA (Max)
Sleep current 10 μA (Max)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M09)
8-pin plastic DIP (DIP-8P-M03)
RoHS compliant

MB85RS2MTA

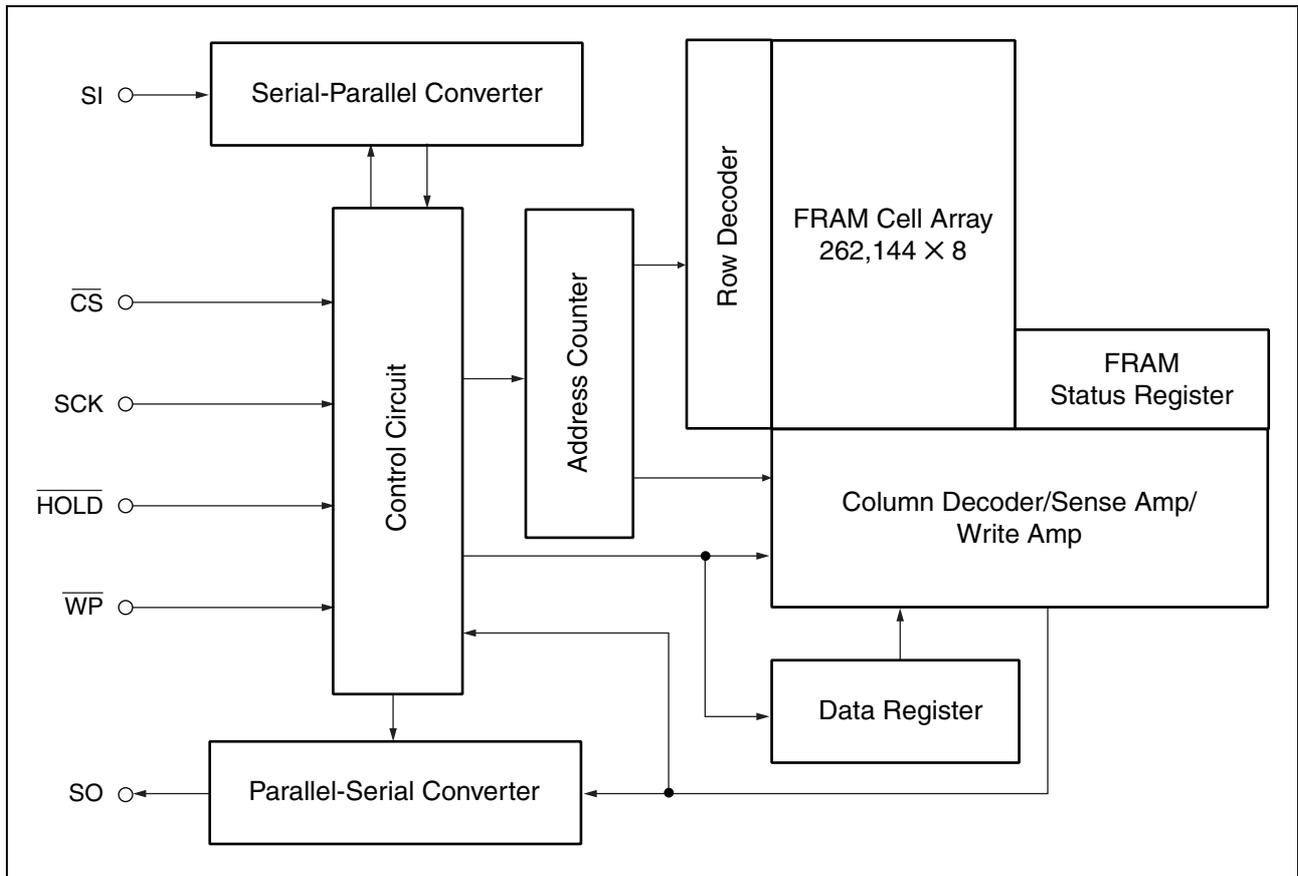
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	\overline{CS}	Chip Select pin This is an input pin to make chips select. When \overline{CS} is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When \overline{CS} is "L" level, device is in select (active) status. \overline{CS} has to be "L" level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	\overline{WP}	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with \overline{WP} and WPEN. See "■ WRITING PROTECT" for detail.
7	\overline{HOLD}	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When \overline{HOLD} is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, \overline{CS} has to be retained "L" level.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

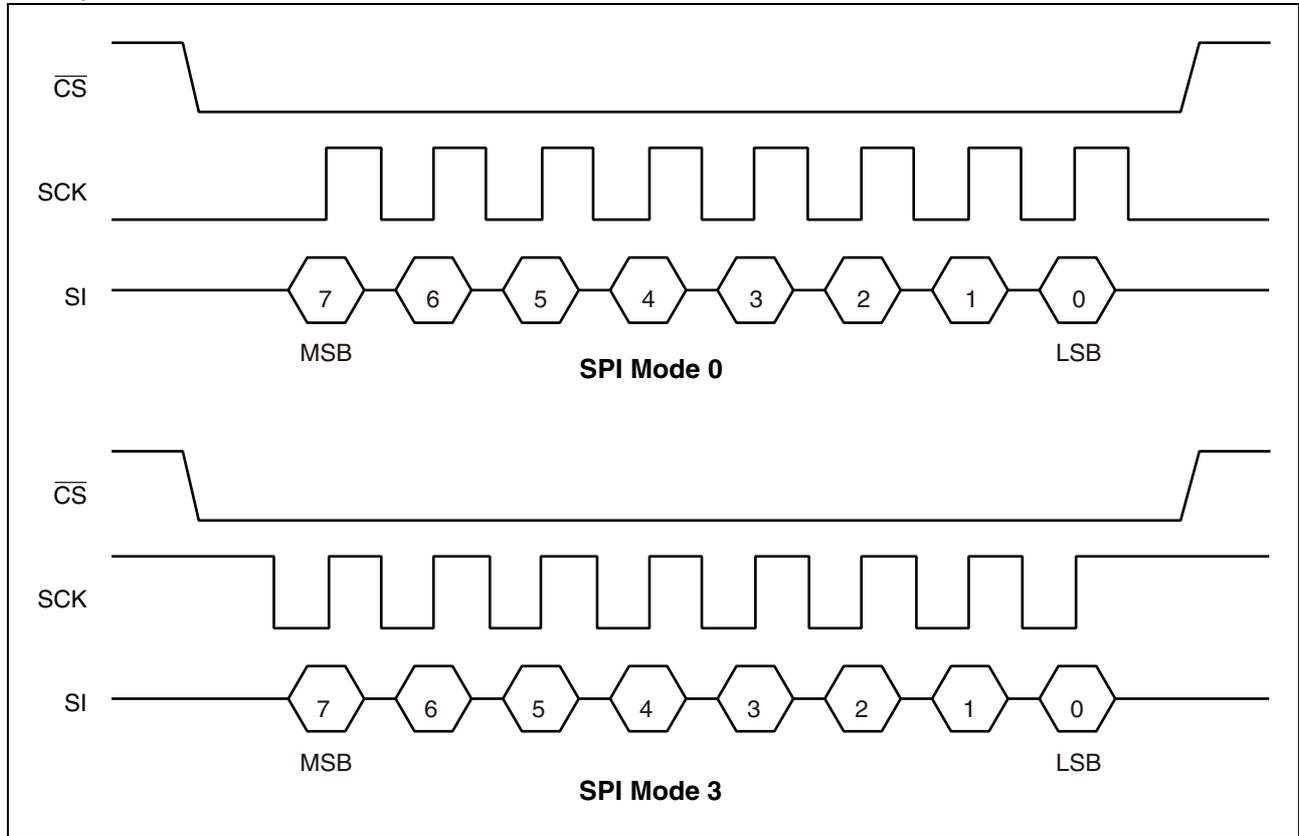
■ BLOCK DIAGRAM



MB85RS2MTA

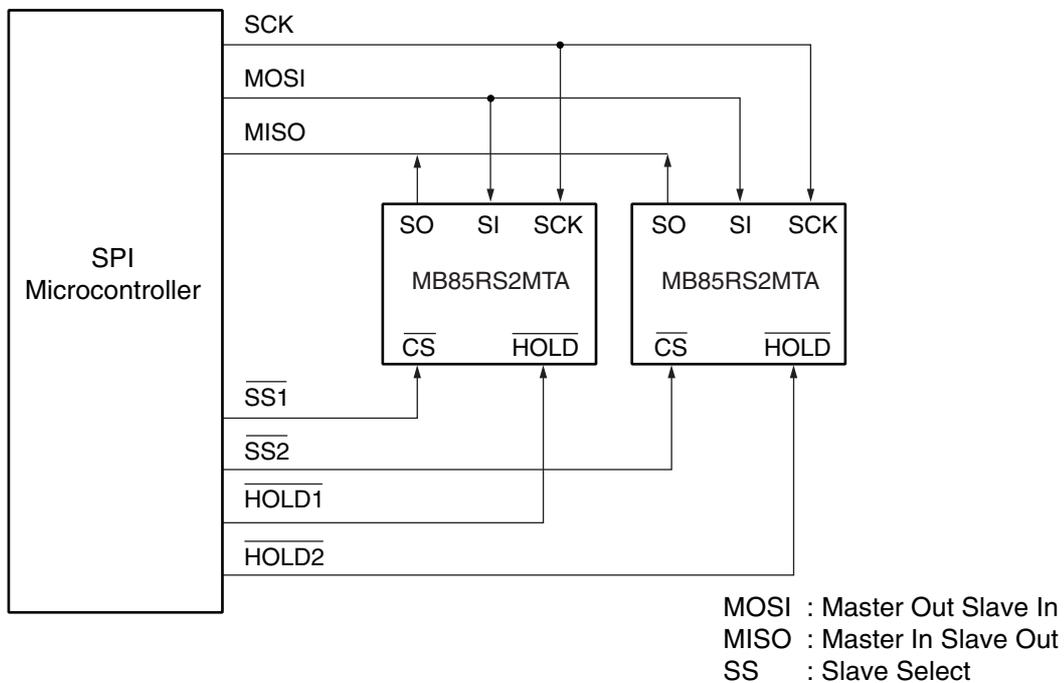
■ SPI MODE

MB85RS2MTA corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).

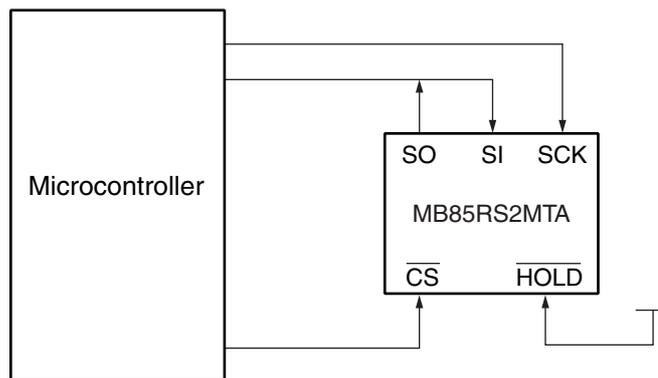


■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS2MTA works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to “■WRITING PROTECT”) relating with \overline{WP} input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. This device supports continual programming mode. After the following operations, without resetting WEL, this device can be programmed continually. After WRSR command. After WRITE command.
0	0	This is a bit fixed to “0”.

■ OP-CODE

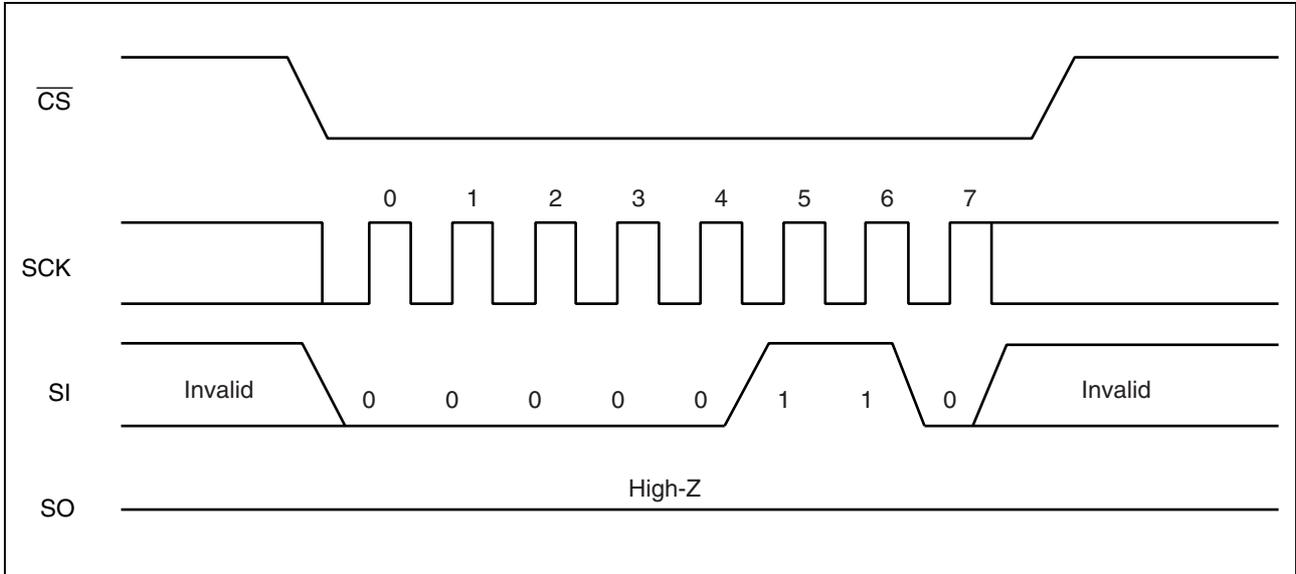
MB85RS2MTA accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If \overline{CS} is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 _B
WRDI	Reset Write Enable Latch	0000 0100 _B
RDSR	Read Status Register	0000 0101 _B
WRSR	Write Status Register	0000 0001 _B
READ	Read Memory Code	0000 0011 _B
WRITE	Write Memory Code	0000 0010 _B
RDID	Read Device ID	1001 1111 _B
FSTRD	Fast Read Memory Code	0000 1011 _B
SLEEP	Sleep Mode	1011 1001 _B

■ COMMAND

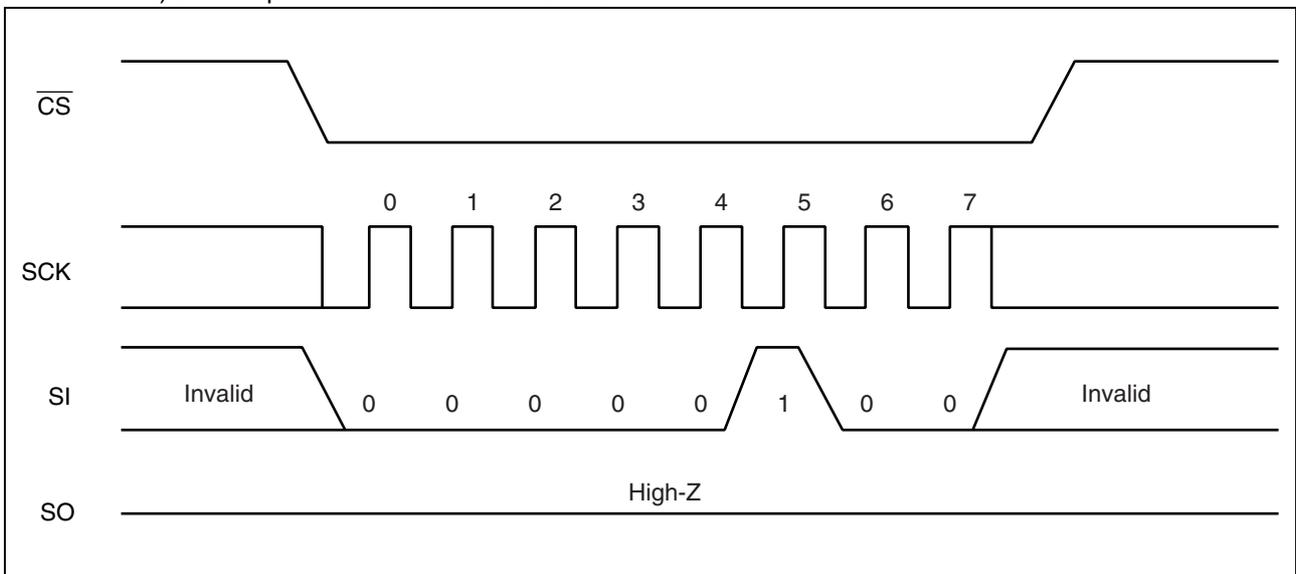
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



• WRDI

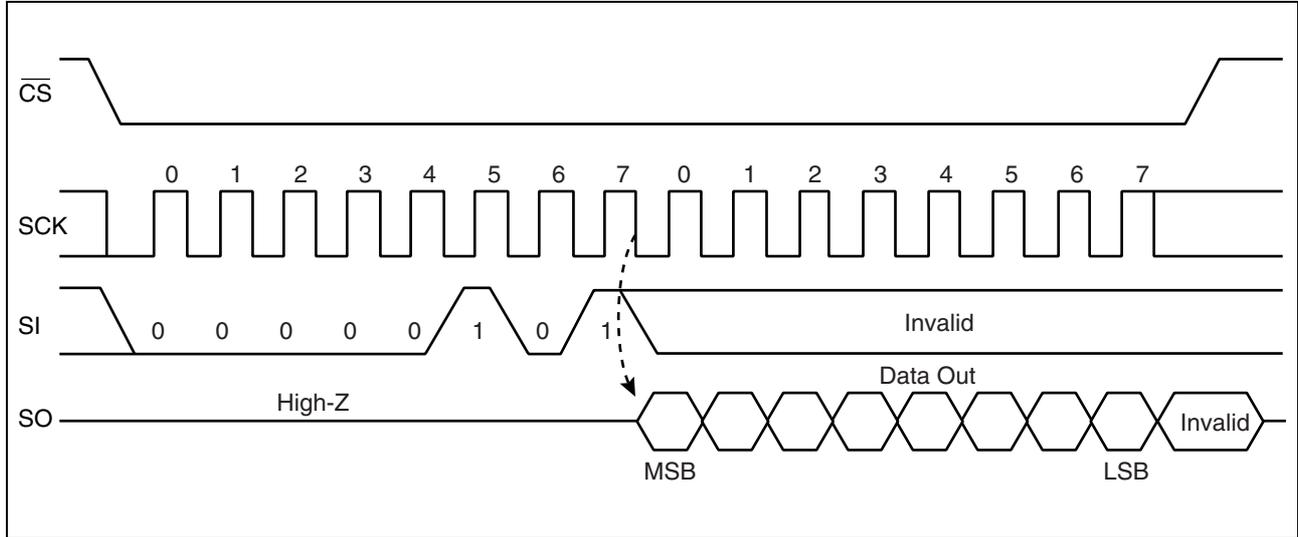
The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.



MB85RS2MTA

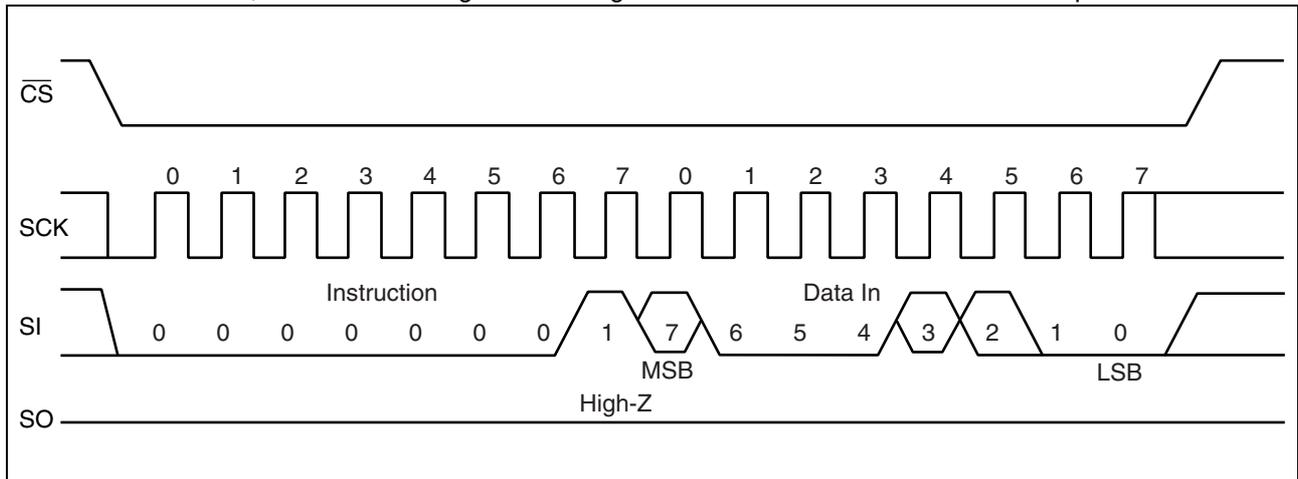
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of \overline{CS} .



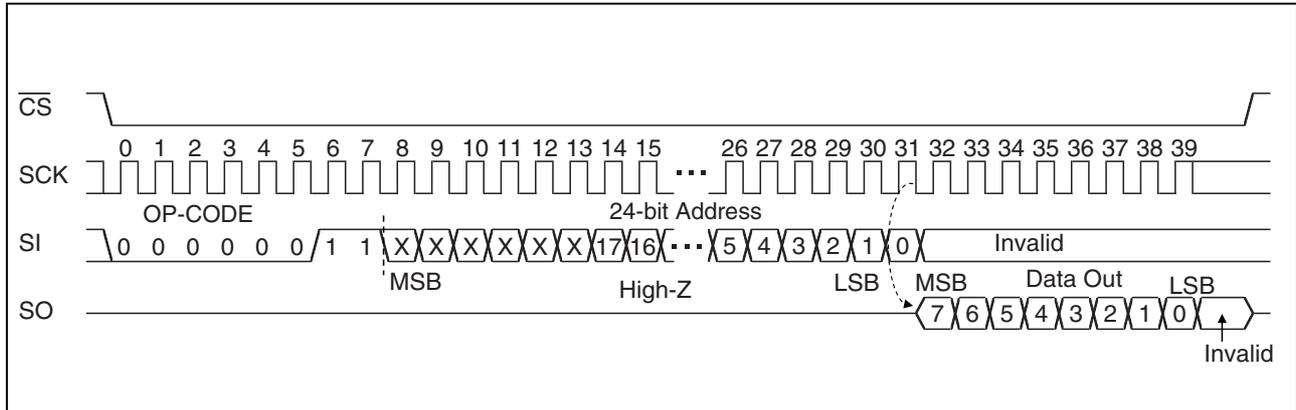
• WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. \overline{WP} signal level shall be fixed before performing WRSR command, and do not change the \overline{WP} signal level until the end of command sequence.



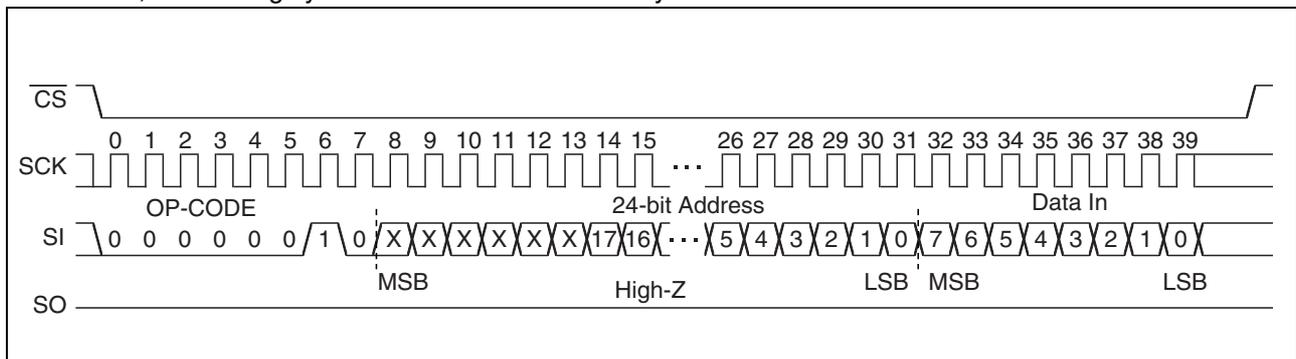
• READ

The READ command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



• WRITE

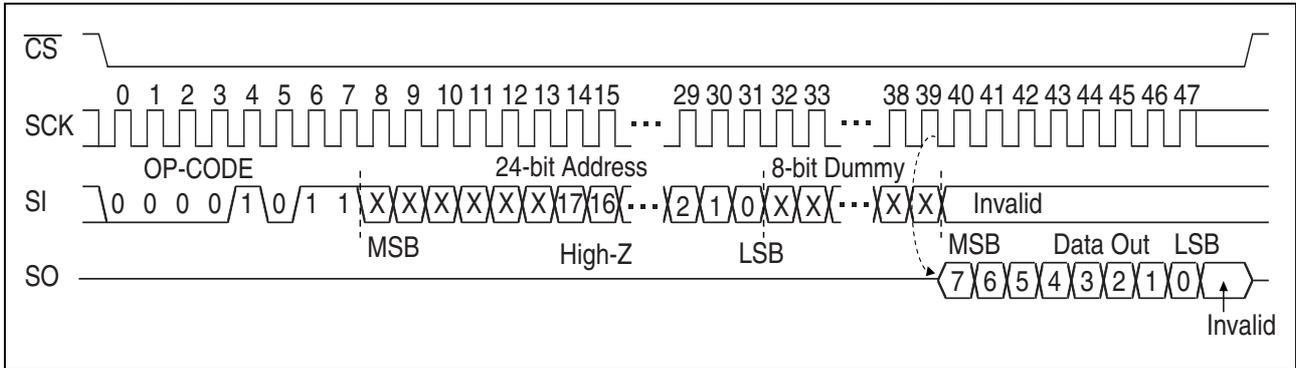
The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 6-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen \overline{CS} will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.



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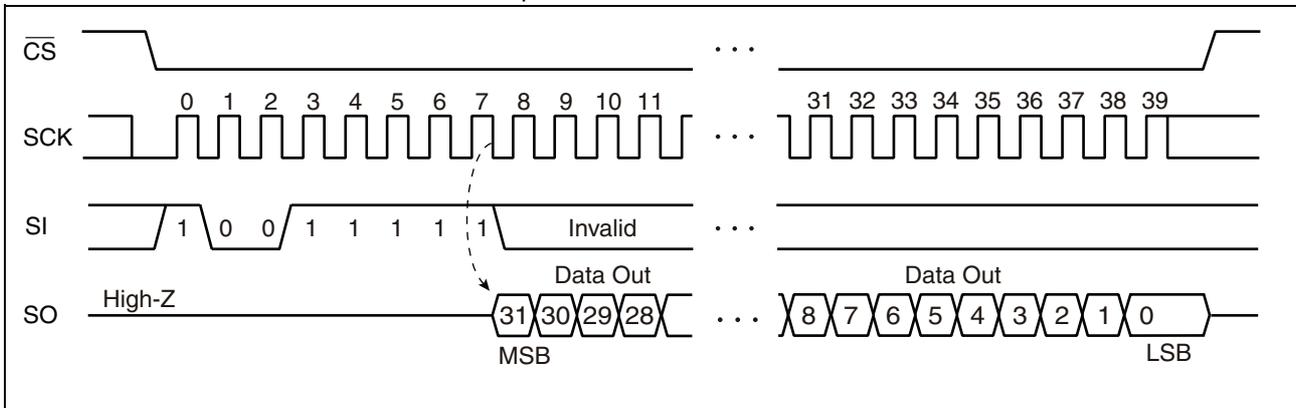
• FSTRD

The FSTRD command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



• RDID

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until \overline{CS} is risen.



	bit								Hex	
	7	6	5	4	3	2	1	0		
Manufacturer ID	0	0	0	0	0	1	0	0	04 _H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	7F _H	

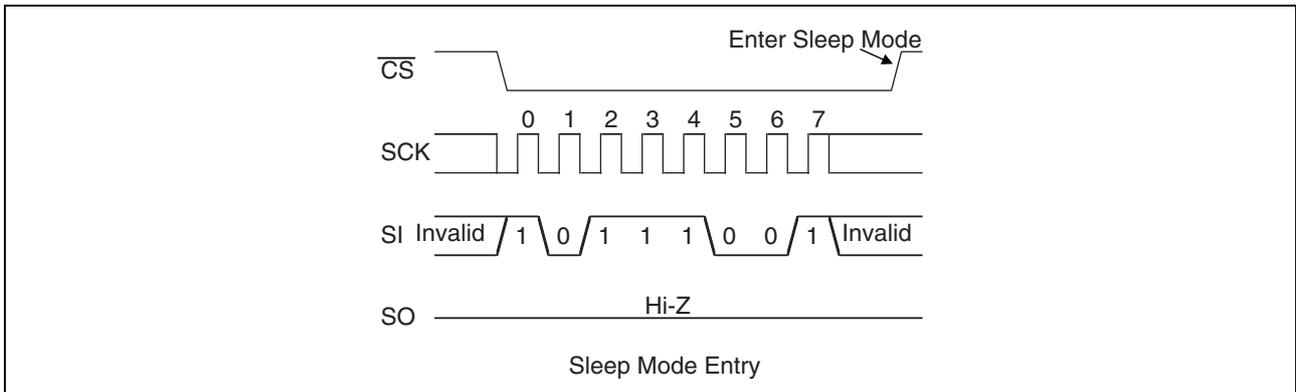
	Proprietary use				Density				Hex	
Product ID (1st Byte)	0	1	0	0	1	0	0	0	48 _H	Density: 01000 _B = 2 Mbit

	Proprietary use								Hex
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03 _H

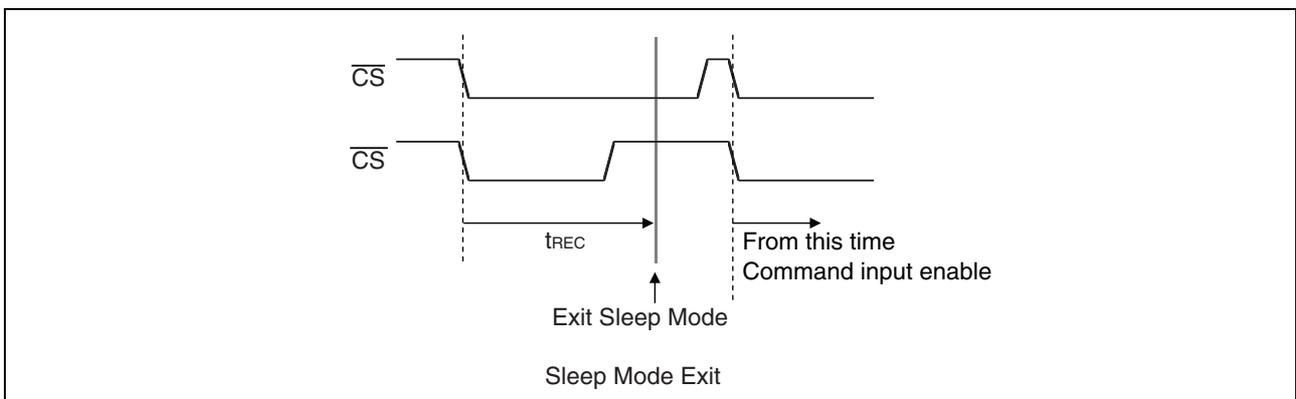
• SLEEP

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of \overline{CS} after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of \overline{CS} after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a Hi-Z state.



Returning to a normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μ s) time from the falling edge of \overline{CS} (see the figure below). It is possible to return \overline{CS} to H level before t_{REC} time. However, it is prohibited to bring down \overline{CS} to L level again during t_{REC} period.



■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	30000 _H to 3FFFF _H (upper 1/4)
1	0	20000 _H to 3FFFF _H (upper 1/2)
1	1	00000 _H to 3FFFF _H (all)

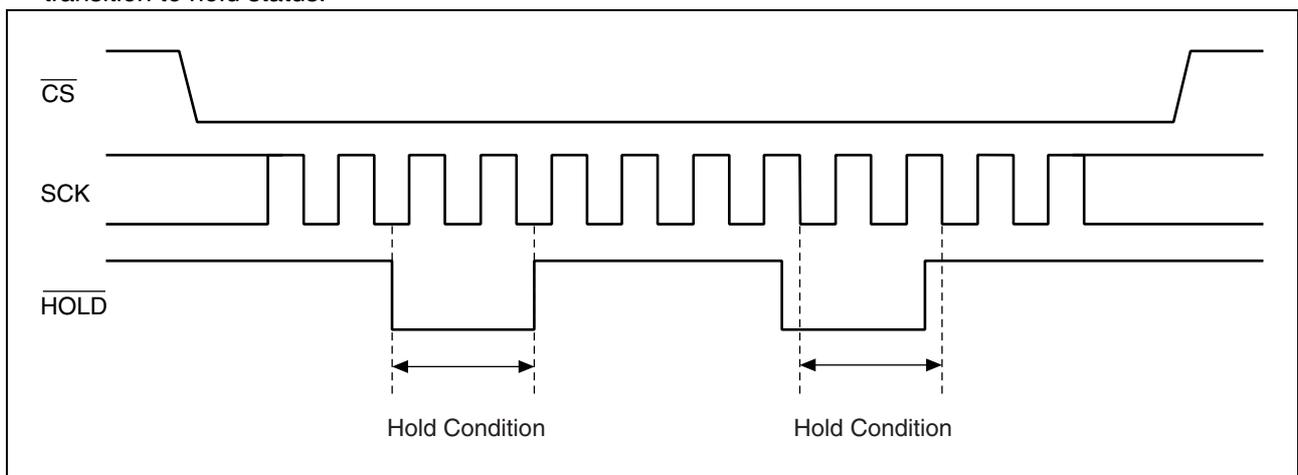
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, \overline{WP} as shown in the table.

WEL	WPEN	\overline{WP}	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if \overline{HOLD} is "L" level while \overline{CS} is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a \overline{HOLD} pin input is transitioned to the hold condition as shown in the diagram below. In case the \overline{HOLD} pin transitioned to "L" level when SCK is "L" level, return the \overline{HOLD} pin to "H" level at SCK being "L" level. In the same manner, in case the \overline{HOLD} pin transitioned to "L" level when SCK is "H" level, return the \overline{HOLD} pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If \overline{CS} is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+ 4.0	V
Input voltage*	V_{IN}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Output voltage*	V_{OUT}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Operation ambient temperature	T_A	- 40	+ 85	°C
Storage temperature	T_{stg}	- 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage ^{*1}	V_{DD}	1.8	3.3	3.6	V
Operation ambient temperature ^{*2}	T_A	- 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	I _{Lil}	$0 \leq \overline{CS} < V_{DD}$	—	—	200	μA
		$\overline{CS} = V_{DD}$	—	—	1	
		$\overline{WP}, \overline{HOLD}, SCK$ $SI = 0 \text{ V to } V_{DD}$	—	—	1	
Output leakage current*2	I _{Lol}	$SO = 0 \text{ V to } V_{DD}$	—	—	1	μA
Operating power supply current	I _{DD}	$SCK = 1 \text{ MHz}$	—	0.16	—	mA
		$SCK = 33 \text{ MHz}$	—	1.6	2.0	
		$SCK = 40 \text{ MHz}$	—	1.9	2.3	
Standby current	I _{SB}	$SCK = SI = \overline{CS} = V_{DD}$	—	—	50	μA
Sleep current	I _{ZZ}	$\overline{CS} = V_{DD}$ All inputs V_{SS} or V_{DD}	—	—	10	μA
Input high voltage	V _{IH}	$V_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$	$V_{DD} \times 0.7$	—	$V_{DD} + 0.5$	V
Input low voltage	V _{IL}	$V_{DD} = 1.8 \text{ V to } 3.6 \text{ V}$	-0.5	—	$V_{DD} \times 0.3$	V
Output high voltage	V _{OH}	$I_{OH} = -2 \text{ mA}$	$V_{DD} - 0.5$	—	—	V
Output low voltage	V _{OL}	$I_{OL} = 2 \text{ mA}$	—	—	0.4	V
Pull up resistance for \overline{CS}	R _P	—	18	33	80	kΩ

*1 : Applicable pin : \overline{CS} , \overline{WP} , \overline{HOLD} , SCK , SI

*2 : Applicable pin : SO

2. AC Characteristics

Parameter	Symbol	Value				Unit
		V _{DD} = 1.8 V to 2.7 V		V _{DD} = 2.7 V to 3.6 V		
		Min	Max	Min	Max	
SCK clock frequency	f _{CK}	0	33	0	40	MHz
Clock high time	t _{CH}	13	—	11	—	ns
Clock low time	t _{CL}	13	—	11	—	ns
Chip select set up time	t _{CSU}	10	—	10	—	ns
Chip select hold time	t _{CSH}	10	—	10	—	ns
Output disable time	t _{OD}	—	12	-	12	ns
Output data valid time	t _{ODV}	—	13	-	9	ns
Output hold time	t _{OH}	0	—	0	—	ns
Deselect time	t _D	40	—	40	—	ns
Data in rising time	t _R	—	50	-	50	ns
Data falling time	t _F	—	50	-	50	ns
Data set up time	t _{SU}	5	—	5	—	ns
Data hold time	t _H	5	—	5	—	ns
HOLD set uptime	t _{HS}	10	—	10	—	ns
HOLD hold time	t _{HH}	10	—	10	—	ns
HOLD output floating time	t _{HZ}	—	20	—	20	ns
HOLD output active time	t _{LZ}	—	20	—	20	ns
SLEEP recovery time	t _{REC}	—	400	—	400	μs

AC Test Condition

Power supply voltage : 1.8 V to 3.6 V

Operation ambient temperature : - 40 °C to + 85 °C

Input voltage magnitude : $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$

$0 \leq V_{IL} \leq V_{DD} \times 0.3$

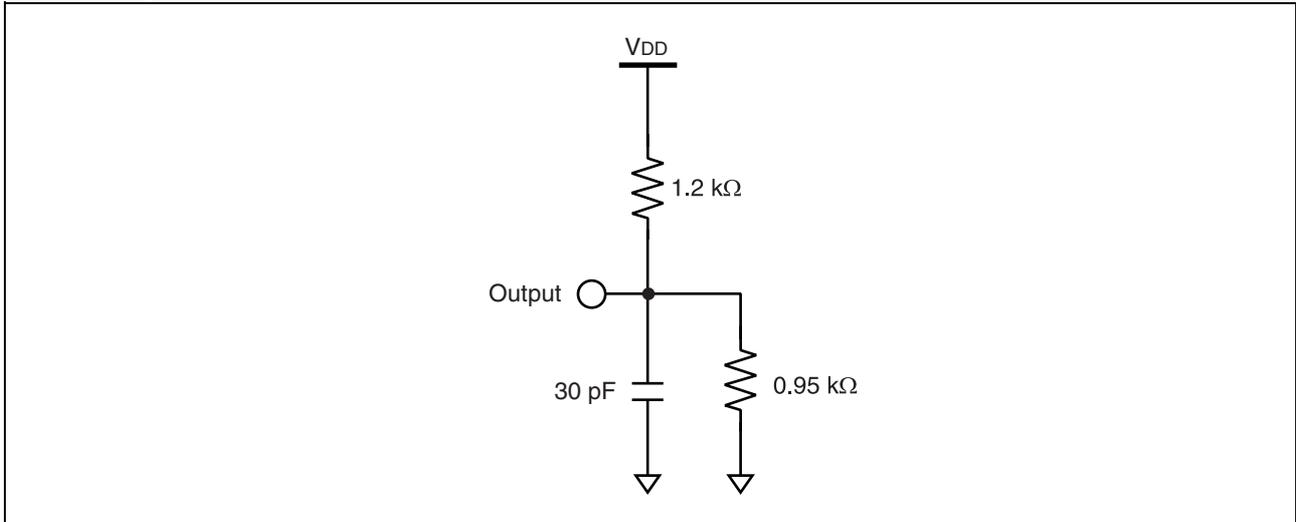
Input rising time : 5 ns

Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

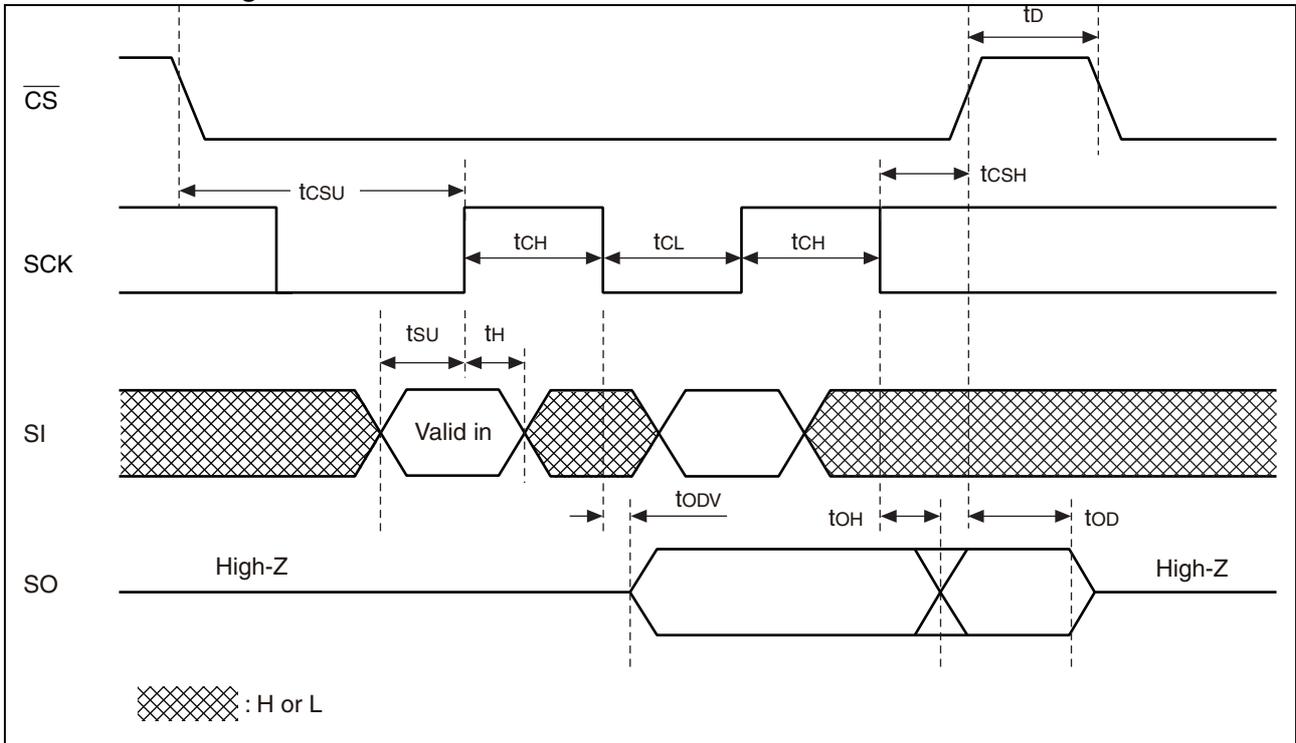


3. Pin Capacitance

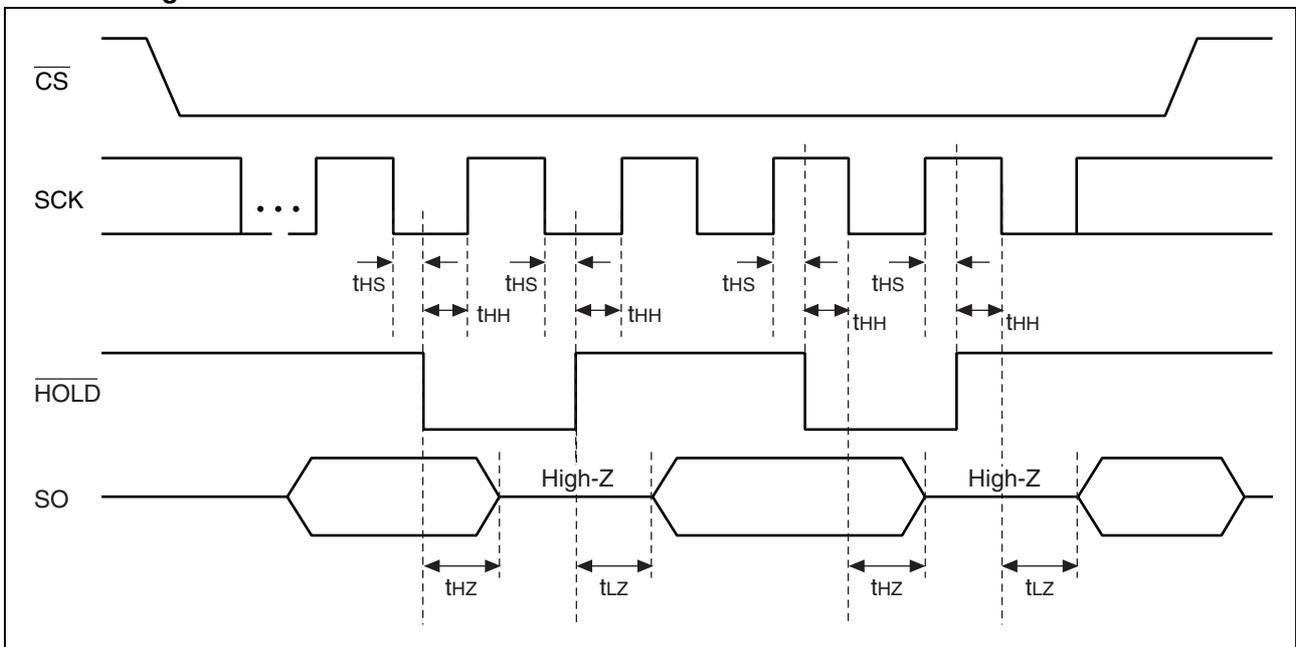
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_o	$V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ °C}$	—	8	pF
Input capacitance	C_i		—	6	pF

■ TIMING DIAGRAM

• Serial Data Timing

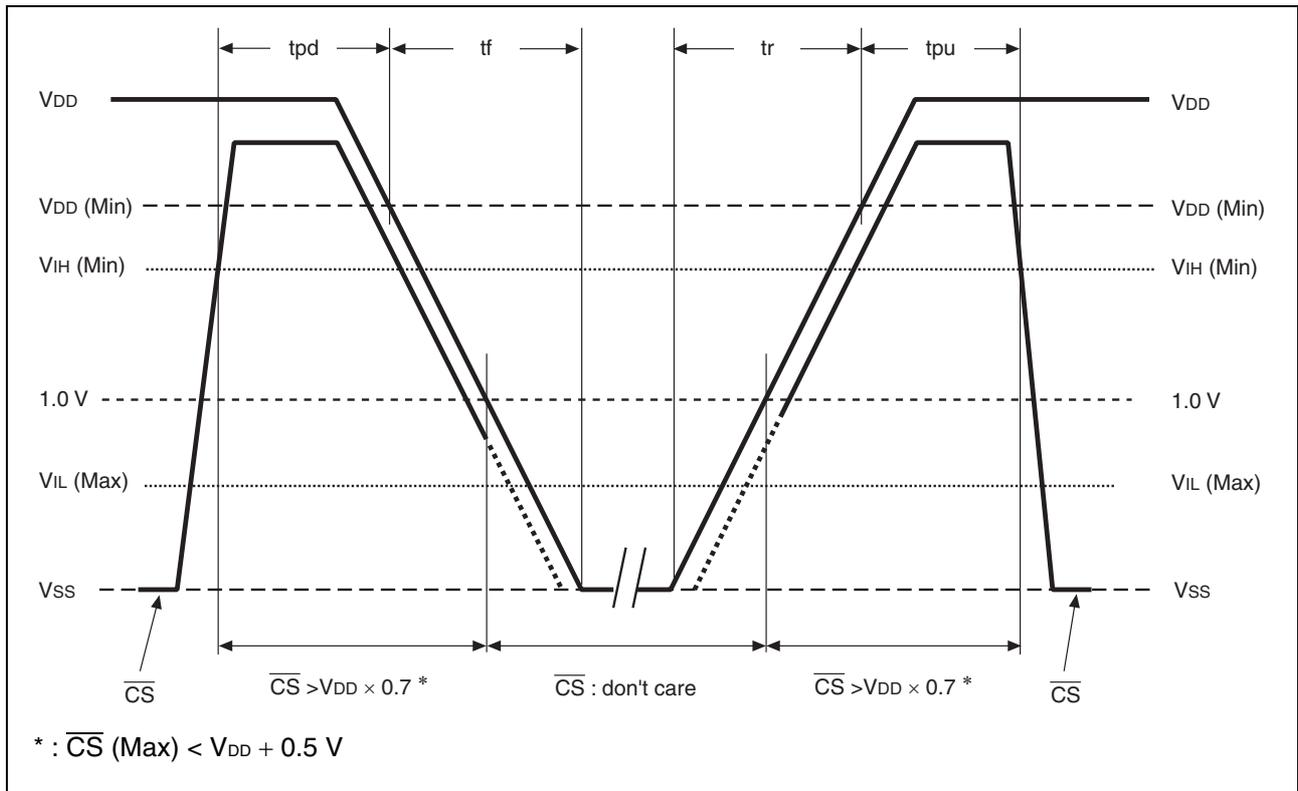


• Hold Timing



MB85RS2MTA

POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit	Parameters
		Min	Max		
\overline{CS} level hold time at power OFF	tpd	0	—	ns	$V_{DD} = 2.7\text{V to } 3.6\text{V}$
		400	—		$V_{DD} = 1.8\text{V to } 2.7\text{V}$
\overline{CS} level hold time at power ON	tpu	250	—	μs	
Power supply rising time	tr	0.05	—	ms/V	
Power supply falling time	tf	0.1	—	ms/V	

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

FRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance	10^{13}	—	Times/byte	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$ Total numbers of reading and writing
Data Retention	10	—	Years	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$ Retention time of the first reading/writing data right after shipment

Note : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

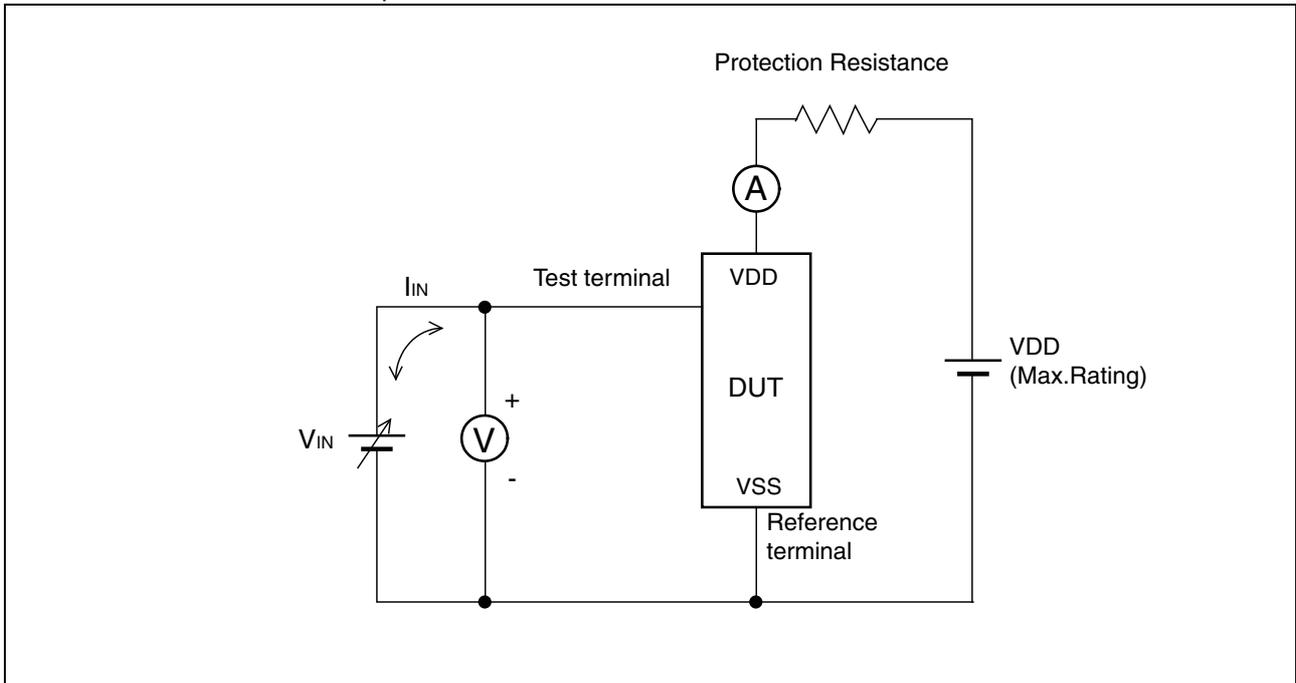
NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS2MTAPNF-G-BDE1 MB85RS2MTAPH-G-JNE2	$\geq 1000 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq 1000 \text{ V} $
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

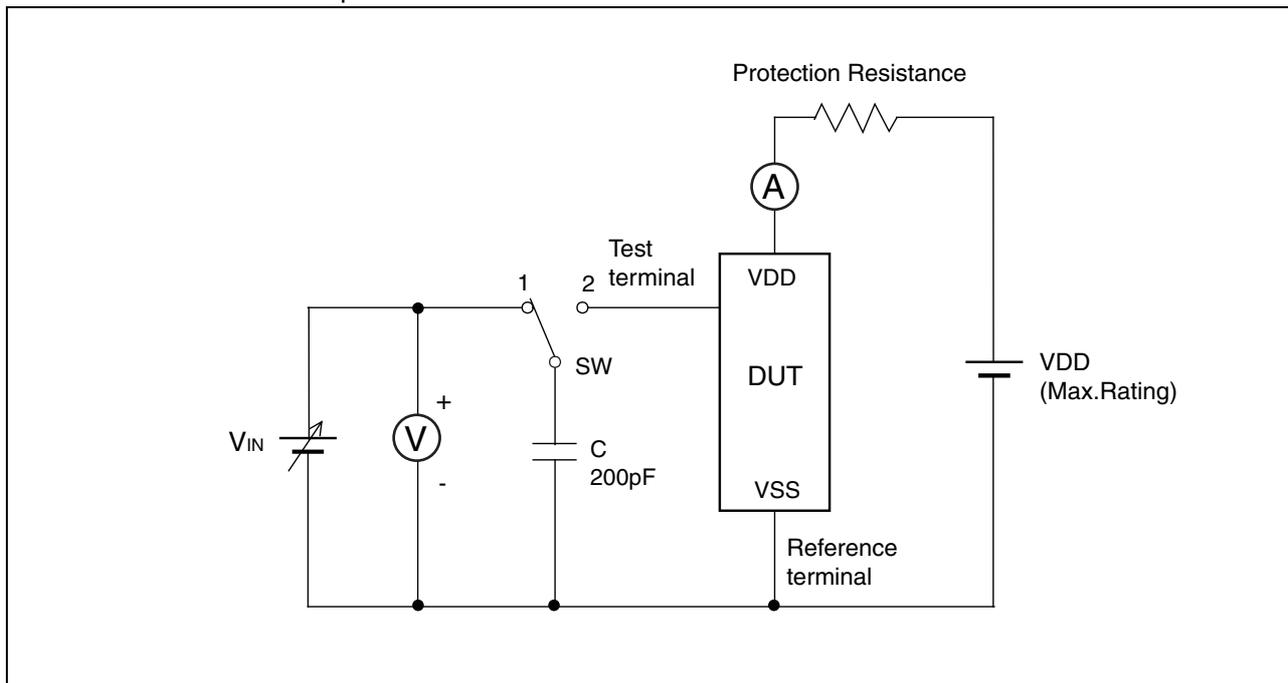
- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
 Confirm the latch up does not occur under $I_{IN} = \pm 300 \text{ mA}$.
 In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

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- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ MB85RS2MTAPNF (8-pin plastic SOP) REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

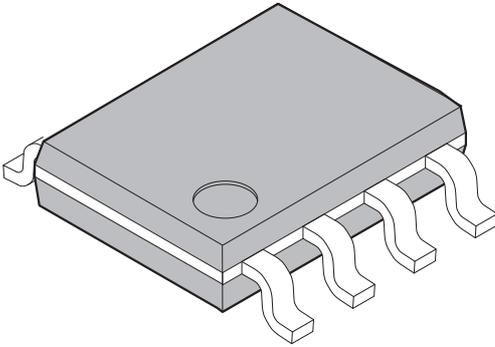
■ ORDERING INFORMATION

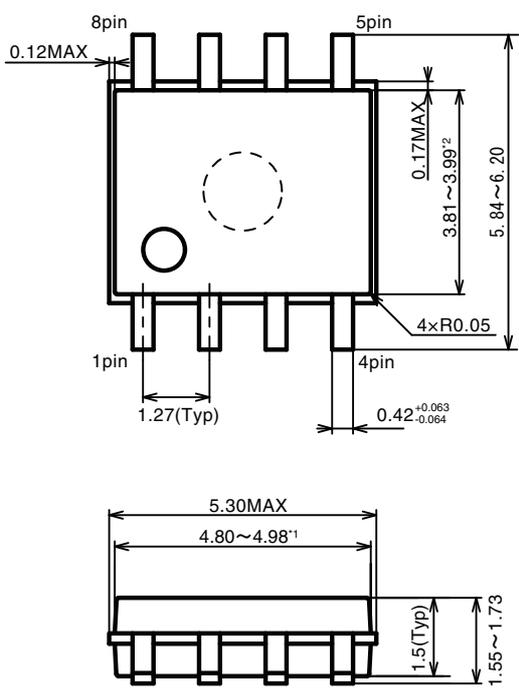
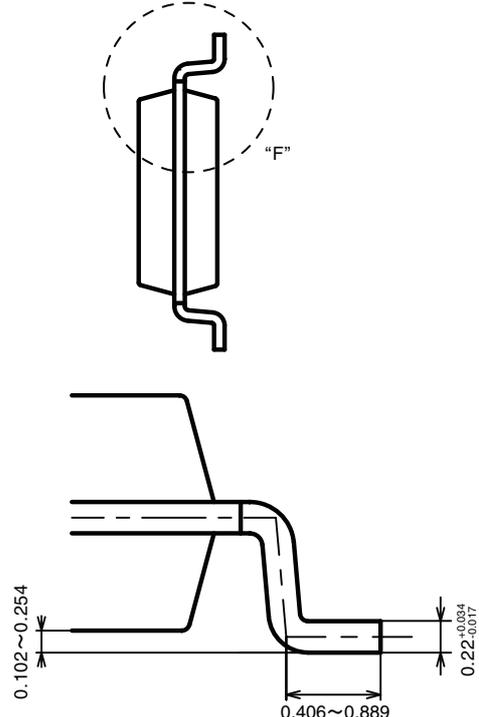
Part number	Package	Shipping form	Minimum shipping quantity
MB85RS2MTAPNF-G-BDE1	8-pin plastic SOP (FPT-8P-M09)	Tube	— *
MB85RS2MTAPNF-G-BDERE1	8-pin plastic SOP (FPT-8P-M09)	Embossed Carrier tape	1500
MB85RS2MTAPH-G-JNE2	8-pin plastic DIP (DIP-8P-M03)	Tube	— *

* : Please contact our sales office about minimum shipping quantity.

MB85RS2MTA

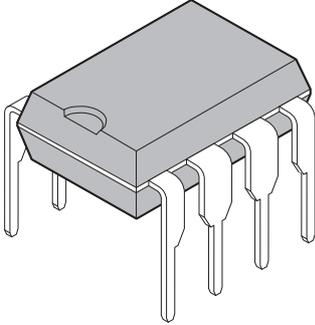
■ PACKAGE DIMENSION

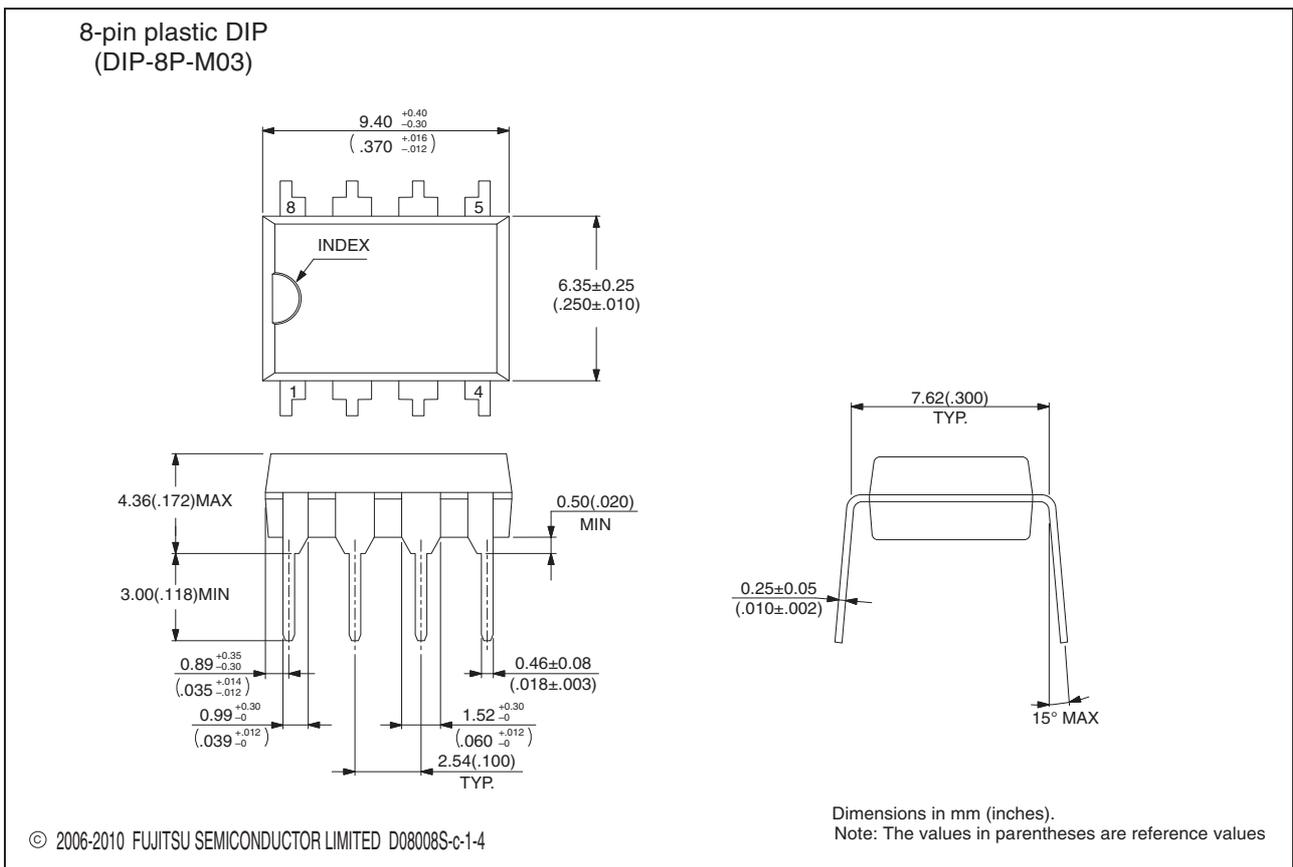
<p>8-pin plastic SOP</p>  <p>(FPT-8P-M09)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 4.89 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.73 mm MAX
	Weight	0.08 g

<p>8-pin plastic SOP (FPT-8P-M09)</p> 	<p>Note 1) *1: These dimensions do not include resin protrusion. Note 2) *2: These dimensions do not include resin protrusion.</p>  <p>Details of "F" part</p> <p>Dimensions in mm</p>
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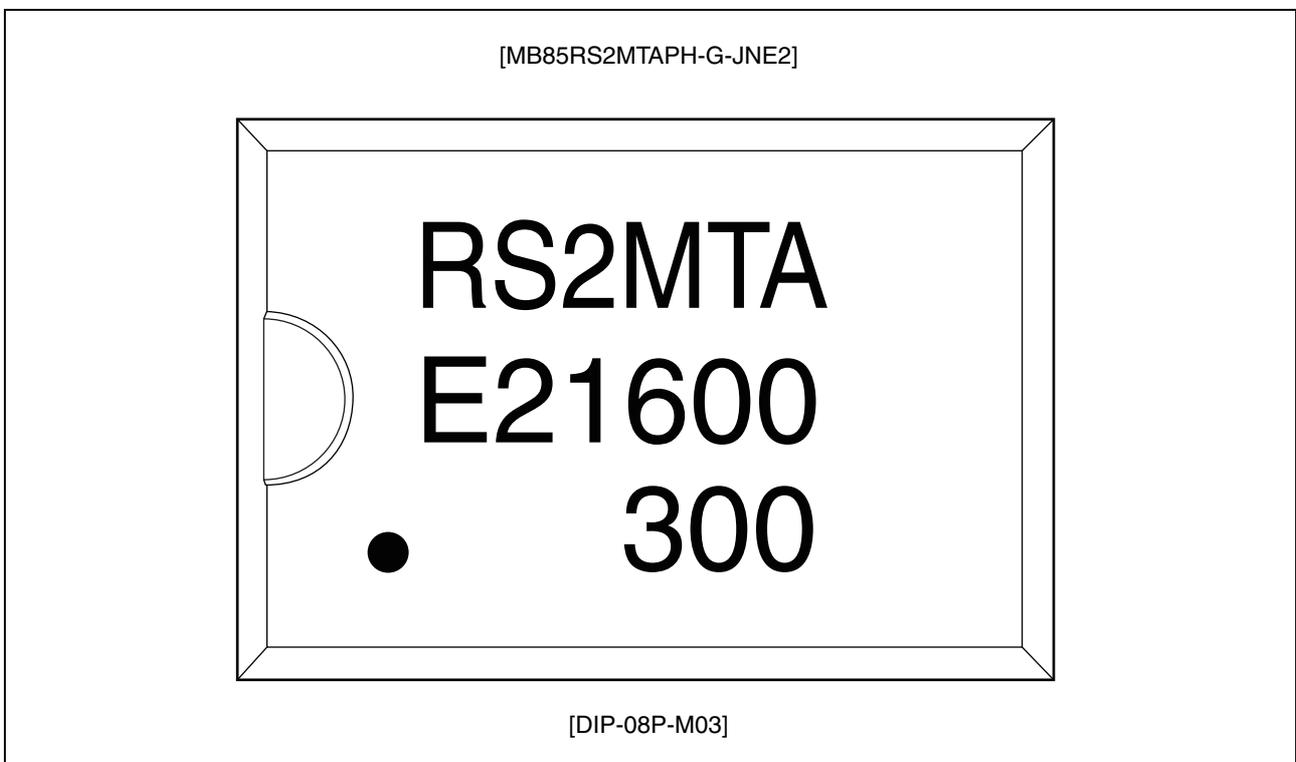
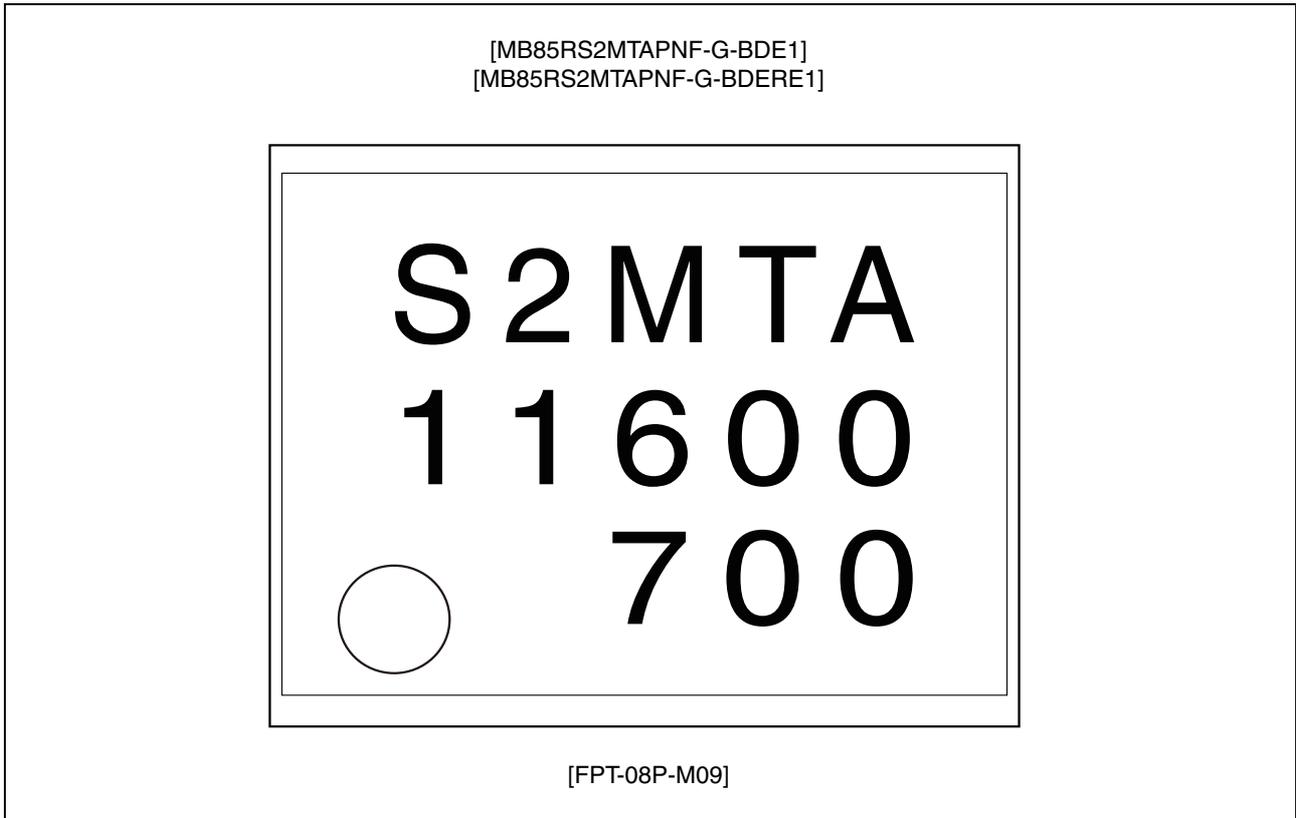
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<p style="text-align: center;">8-pin plastic DIP</p>  <p style="text-align: center;">(DIP-8P-M03)</p>	Lead pitch	2.54 mm
	Sealing method	Plastic mold
	Weight	0.46 g



■ MARKING



■ MAJOR CHANGES IN THIS EDITION

Changes on pages are indicated by vertical lines drawn on the left side of that pages.

Page	Section	Change Results
1	■ FEAUTURES	Operating power supply current IDD SCK=40MHz 2.0mA --> Operating power supply current IDD SCK=40MHz 2.3mA
6	■ STATUS REGISTER Write Enable Latch	Addition of the following comments; This device supports continual programming mode. After the following operations, without resetting WEL, this device can be programmed continually. After WRSR command. After WRITE command.
13	■ ABSOLUTE MAXIMUM RATIGS Input voltage (Max), Output voltage (Max)	$V_{DD} + 0.5 \rightarrow V_{DD} + 0.5 (\leq 4.0)$
14	■ ELECTRICAL CHARACTERISTICS 1. DC Characteristics	Operating power supply current IDD SCK=40MHz 2.0mA --> Operating power supply current IDD SCK=40MHz 2.3mA Operating power supply current IDD SCK=33MHz 2.0mA
16	AC Load Equivalent Circuit	3.3V --> V_{DD}
18	■ POWER ON/OFF SE- QUENCE \overline{CS} level hold time at power OFF (Min)	$\overline{CS} > V_{DD} * 0.8V \rightarrow \overline{CS} > V_{DD} * 0.7V$ GND --> V_{SS} 400ns --> 0ns ($V_{DD}=2.7V$ to 3.6V), 400ns ($V_{DD}=1.8V$ to 2.7V)
24	■ MARKING [MB85RS2MTAPH-G-JNE2]	E11600 --> E21600

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