NVMFS5C450NL

Power MOSFET

40 V, 2.8 mΩ, 110 A, Single N−Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C450NLWF − Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	110	A
		T_C = 100°C		81	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	68	W
		T_C = 100°C		34	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	27	A
		T_A = 100°C		19	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.7	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	740	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to + 175	°C
Source Current (Body Diode)			I_S	76	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 7 A)			E_{AS}	215	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	2.2	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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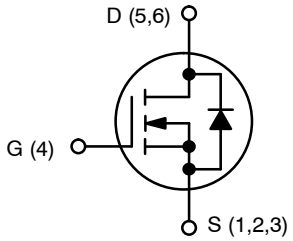
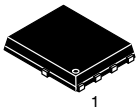
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	2.8 mΩ @ 10 V	110 A
	4.4 mΩ @ 4.5 V	

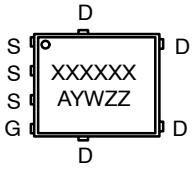


N−CHANNEL MOSFET



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



XXXXXX = 5C450L
(NVMFS5C450NL) or
450LWF
(NVMFS5C450NLWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				1.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 60 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 40 A		3.5	4.4	mΩ
		V_{GS} = 10 V	I_D = 40 A		2.3	2.8	
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 40 A			120		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			2100		pF
Output Capacitance	C_{OSS}				1000		
Reverse Transfer Capacitance	C_{RSS}				42		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 40 A			16		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 40 A			35		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 40 A			4		nC
Gate−to−Source Charge	Q_{GS}				7		
Gate−to−Drain Charge	Q_{GD}				5		
Plateau Voltage	V_{GP}				3.2		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 40 A, R_G = 1 Ω			11		ns
Rise Time	t_r				110		
Turn−Off Delay Time	$t_{d(OFF)}$				21		
Fall Time	t_f				5		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 40 A	T_J = 25°C		0.84	1.2	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 40 A			41		ns
Charge Time	t_a				19		
Discharge Time	t_b				22		
Reverse Recovery Charge	Q_{RR}				31		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

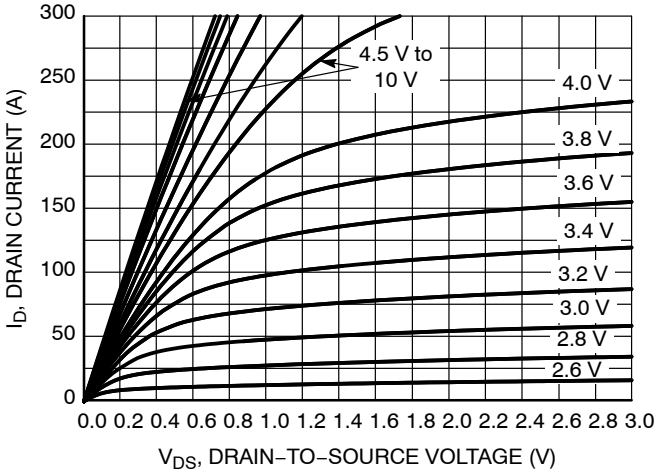


Figure 1. On−Region Characteristics

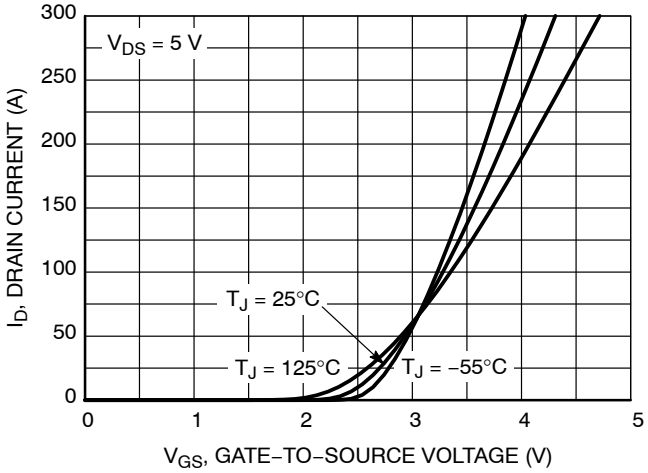


Figure 2. Transfer Characteristics

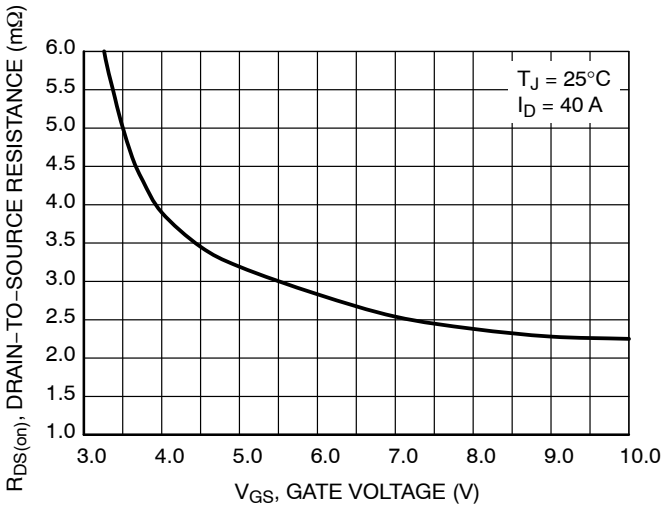


Figure 3. On−Resistance vs. Gate−to−Source Voltage

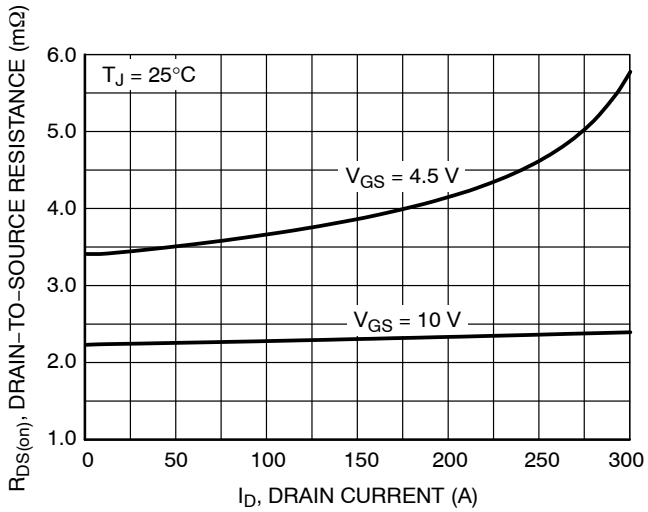


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

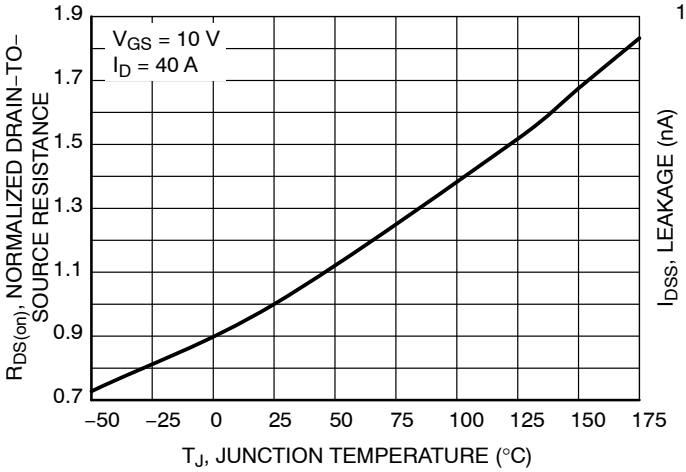


Figure 5. On−Resistance Variation with Temperature

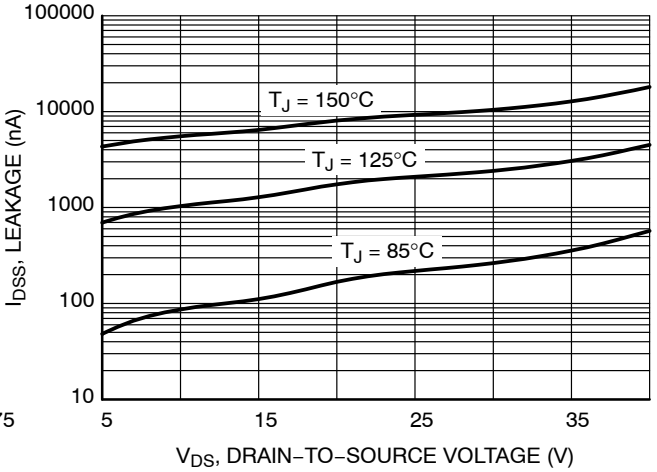


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

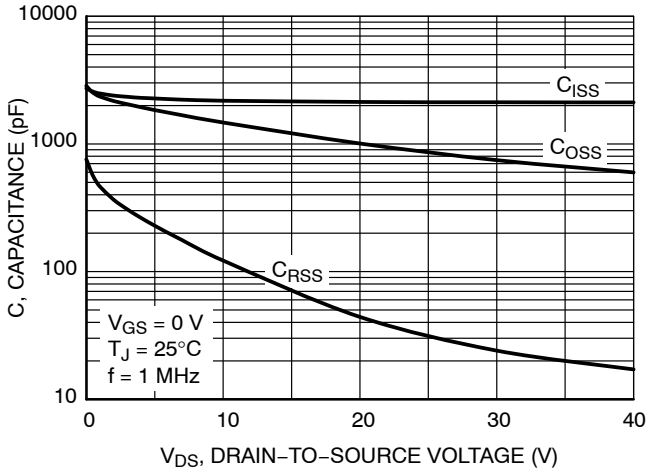


Figure 7. Capacitance Variation

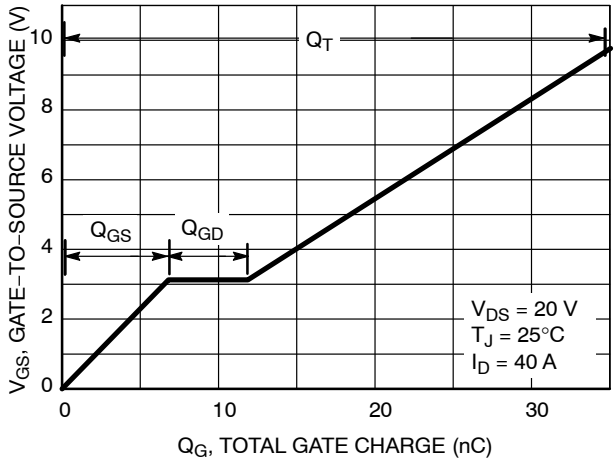


Figure 8. Gate−to−Source Voltage vs. Total Charge

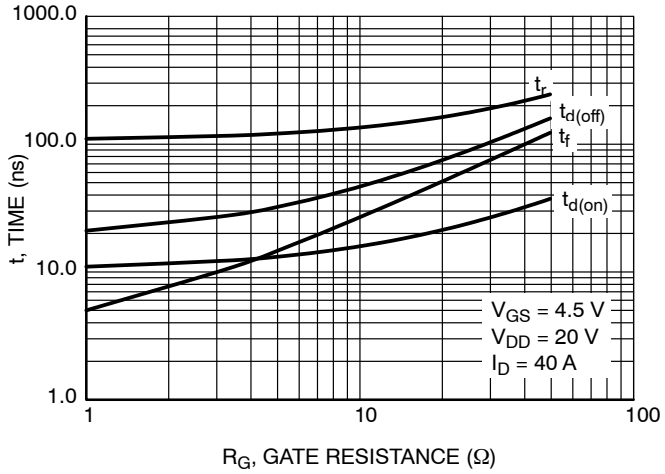


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

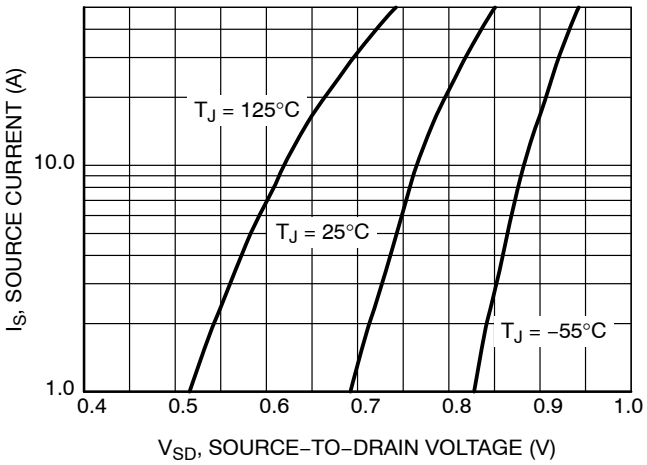


Figure 10. Diode Forward Voltage vs. Current

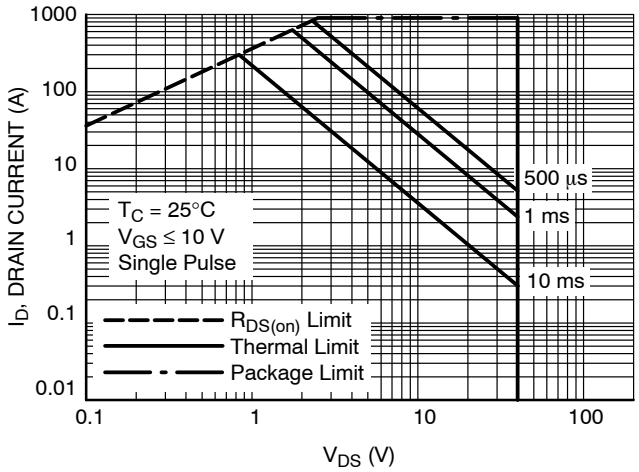


Figure 11. Safe Operating Area

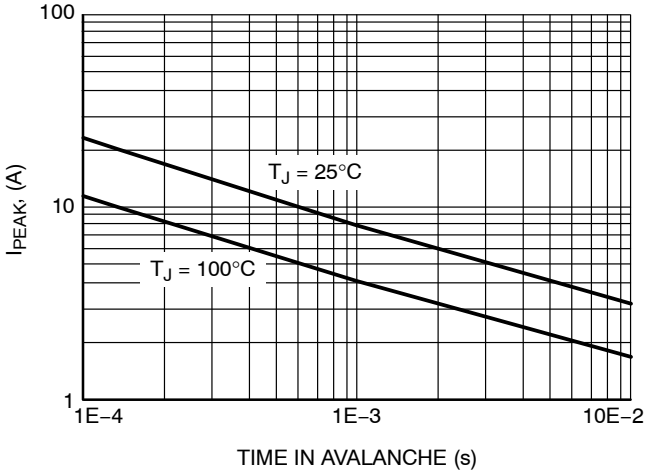


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

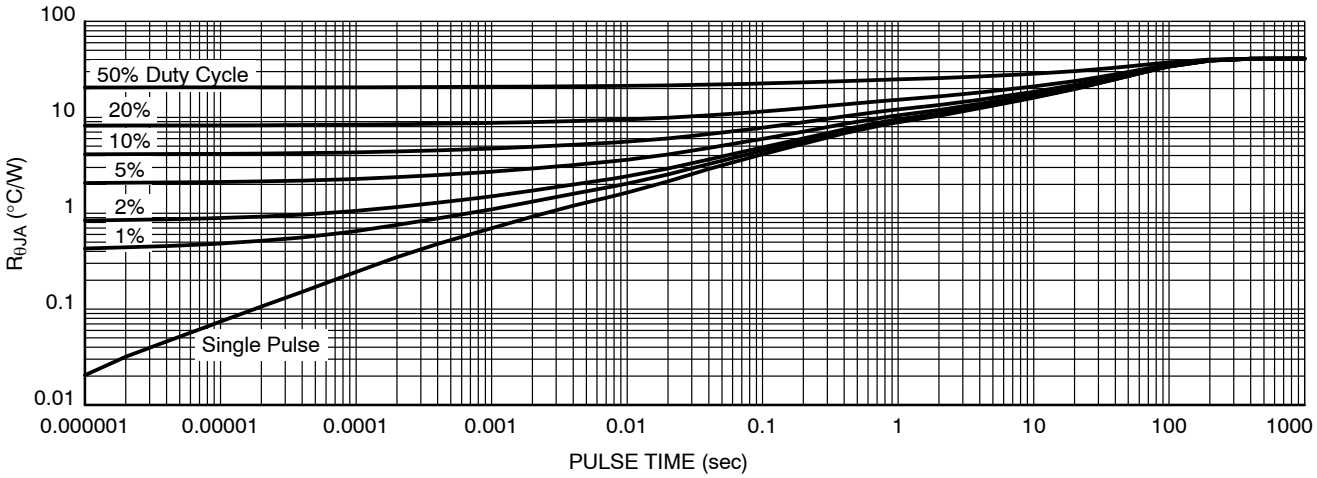


Figure 13. Thermal Characteristics

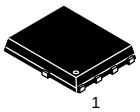
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5C450NLT1G	5C450L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5C450NLWFT1G	450LWF	DFN5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C450NLT3G	5C450L	DFN5 (Pb−Free)	5000 / Tape & Reel
NVMFS5C450NLWFT3G	450LWF	DFN5 (Pb−Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C450NLAFT1G	5C450L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5C450NLWFAFT1G	450LWF	DFN5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

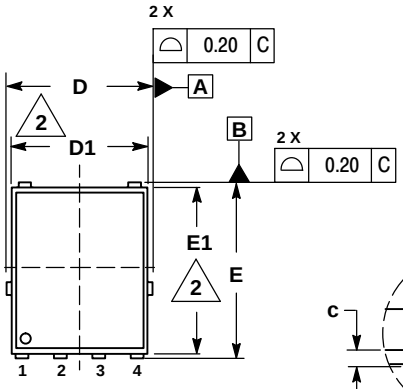
ON Semiconductor®



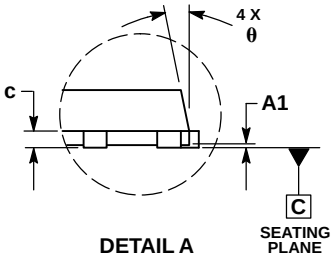
SCALE 2:1

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE M

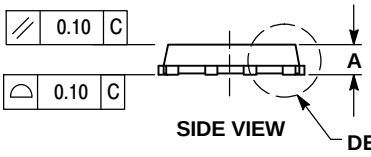
DATE 27 MAY 2015



TOP VIEW

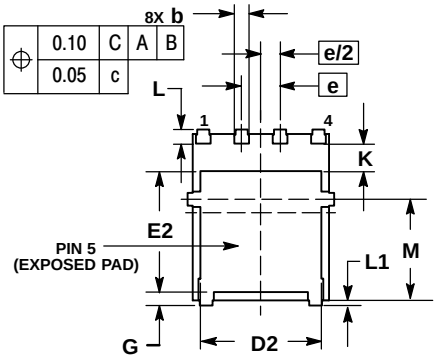


DETAIL A



SIDE VIEW

DETAIL A

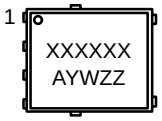


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

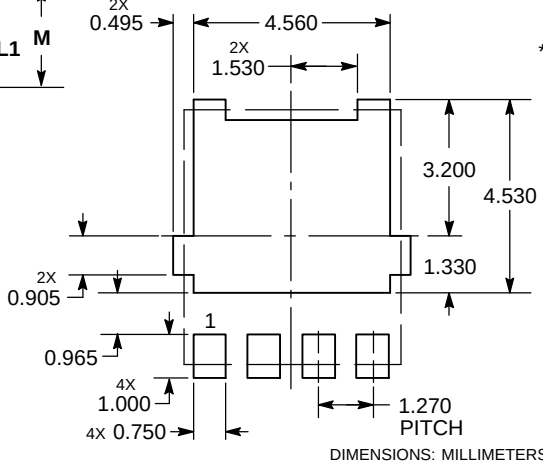
GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON14036D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC MO−240A	
DESCRIPTION:	DFN5 5X6, 1.27P (SO−8FL)	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY K. KIME.	13 JAN 2004
A	ADDED STYLE 1. REQ. BY K. KIME.	23 MAR 2004
B	ADDED DIMENSION M AND SOLDERING FOOTPRINT. UPDATED DESCRIPTION. REQ. BY K. KIME.	31 AUG 2005
C	CHANGED DIMENSION A NOM FROM 0.99 TO 1.00 & MAX FROM 1.20 TO 1.10. REQ. BY L. DELUCA.	29 JUN 2007
D	CHANGED PACKAGE DESCRIPTION FROM DFN6 TO DFN5. REQ. BY D. TRUHITTE.	31 MAR 2009
E	ADDED STYLE 2. REQ. BY D. TRUHITTE.	17 AUG 2010
F	CORRECTED MARKING DIAGRAM TO ADD LOT TRACEABILITY. REQ. BY J. CARTER.	12 APR 2012
G	CHANGED K DIMENSIONS TO 1.2 MIN, 1.35 NOM, 1.5 MAX. REQ. BY D. TRUHITTE.	23 APR 2012
H	MODIFIED DIMENSIONS D1, D2, E1, & E2. REQ. BY I. MARIANO.	05 MAR 2013
J	ADDED MIN AND MAX VALUES TO DIMENSIONS D AND E. REQ. BY D. TRUHITTE.	17 JUN 2014
K	CHANGED DIMENSION L1 TO NOMINAL VALUE OF 0.125. REQ. BY D. TRUHITTE.	10 JUL 2014
L	ROTATED SOLDER FOOTPRINT 180 DEGREES TO MATCH TOP VIEW PIN ONE ORIENTATION. REQ. BY D. TRUHITTE.	26 SEP 2014
M	CHANGED NOMINAL VALUES FOR DIMENSIONS G AND L TO 0.575. REQ. BY I. HYLAND.	27 MAY 2015

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

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For additional information, please contact your local Sales Representative

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