Data sheet

Rev. 0.1

PPS964A

Integrated Module for Heart rate monitors

Specification Revisions

- Revision history.

Rev	Date	Revision history
0.1	2017.07.12	Initial Release

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PPS964A(GGI)

Integrated Module for Heart rate monitors

1. Overview

1.1 Brief Description

The PPS964A is an integrated module for PPG applications like Heart rate monitoring.
It supports 2 simultaneous switching LEDs incident on a single Photodiode. The current from the Photodiode is converted into a voltage by the Transimpedance amplifier and digitized using an ADC. The ADC code can be read out using an I2C interface. The PPS964A also has a fully integrated LED driver with a 6-bit current control.

Features

- Pulse frequency 10 SPS to 1000 SPS
- Flexible pulse sequencing and timing control
- Clocked by external clock or by internal oscillator
- Flexible clock options :
  - i) External clocking : 4-60 MHz input clock
  - ii) Internal clocking : 4 MHz oscillator
- I2C interface

Transmitter :

- Supports common anode LED configurations
- 100 dB of dynamic range
- 6-bit programmable LED current to 100 mA
- Programmable LED On-time
- Simultaneous support of 3 LEDs for optimized HRM or multi-wavelength HRM

Receiver:

- 24-bit representation of a current input from a photodiode in Twos complement format
- Individual DC offset subtraction DAC at TIA Input for each LED and ambient phase
- Digital ambient subtraction at ADC output
- Programmable transimpedance gain from 10K-2MΩ
- 100 dB of dynamic range
- Dynamic power saving mode to reduce current to less than 300 uA

Physical Characteristics

- Operation temperature: -30 to +85 °C
- Supply voltage:
  Rx : 2.0 to 3.6 V, Tx : 3.0V to 5.25V
- Small size package : 6.8X2.8X1.25mm, 12 LGA
- Dual Green LED Package

1.2. Block Diagram

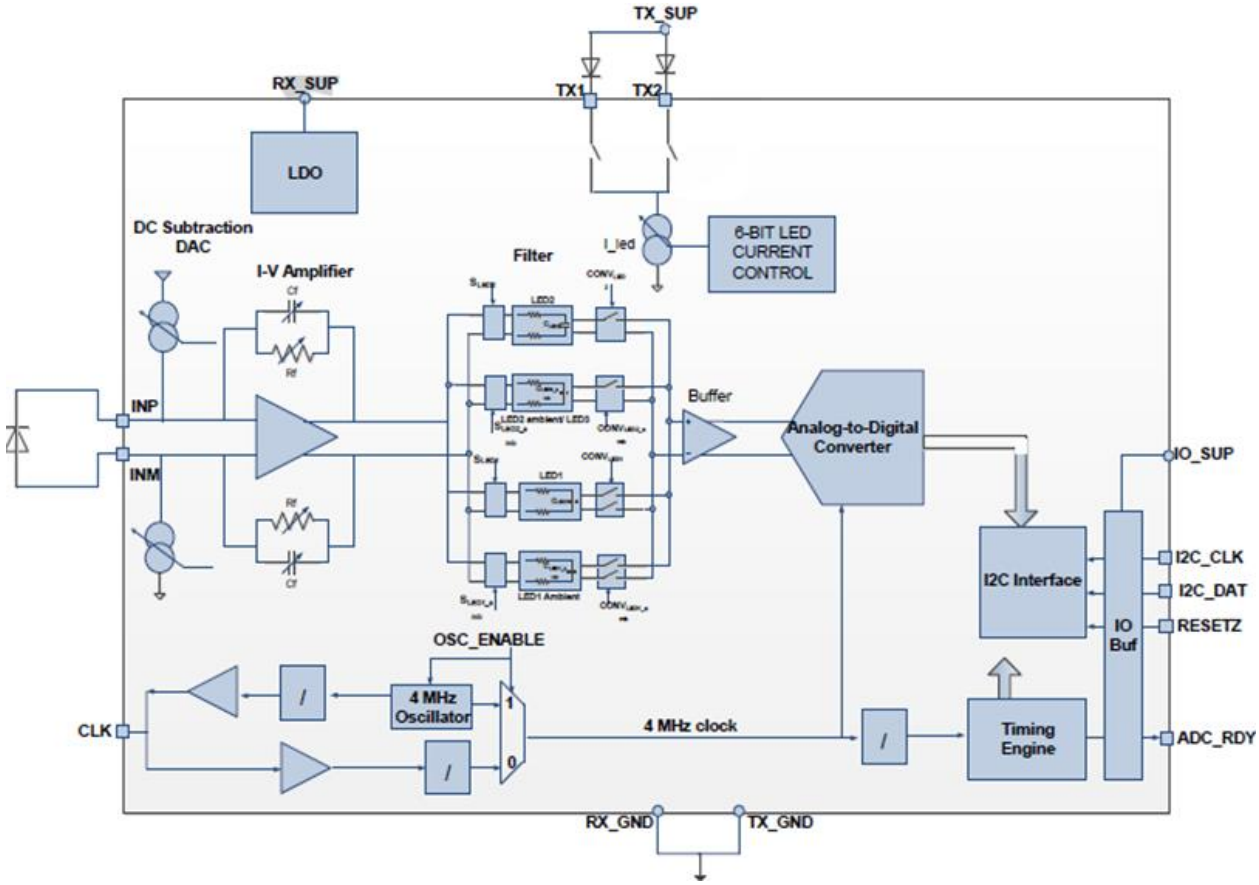


Figure 1. Block Diagram.

1.3 Applications

- Mobile devices (smart phones and tablet PC)
- Wearable devices and Fitness assistant devices
  - Activity Tracker & Smart Watch
  - Bio-headset, helmets, Ear-set,,, and so on

1.4 Pin Configurations

• 12 -LGA (PPS964A)

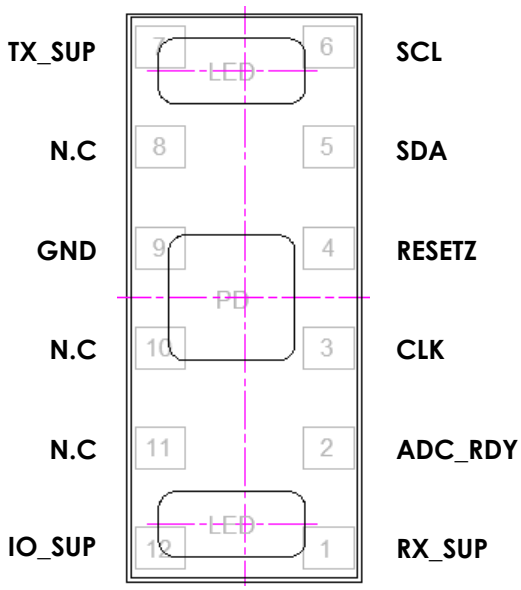


Figure 2. PKG Diagram.

(Top View)

1.5 Pin Description

Table 1. Pin Description.

PIN No.	PIN Name	Description
1	RX_SUP	Receiver supply. 2-3.6V, 1uF decap to GND
2	ADC_RDY	ADC ready interrupt signal (Output)
3	CLK	Clock Input/ Output selectable based on register. Default is input (external clock mode). Can be set using register to output the clock when the oscillator is enabled.(1)
4	RESETZ	RESETZ/ PWDN – function based on (active low) width of RESETZ pulse >25 to 50 us width: RESET mode active >200 us width: PWDN active
5	SDA	I2C data, External pull-up resistor to IO_SUP
6	SCL	I2C clock input, External pull-up resistor to IO_SUP
7	TX_SUP	Transmitter supply. 1uF decap to GND
8	NC	Not connected
9	GND	Common ground
10	NC	Not connected
11	NC	Not connected
12	IO_SUP	Separate supply for Digital I/O. Should be less than or equal to RX_SUP. Can be tied to RX_SUP.

(1) In both hardware powerdown (PWDN) and software powerdown (PDNAFE) modes, the CLK pin gets driven by the AFE to 0V. So if operating in external clock mode, take care to shut off the external clock to the AFE when in these powerdown modes.

2. IC Characteristics

2.1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter	Conditions	Min.	Max.	Units
Supply voltage range	RX_SUP to GND	-0.3	4	V
	IO_SUP to GND	-0.3	4	V
	IO_SUP-RX_SUP	-0.3		V
	TX_SUP to GND	-0.3	6	V
Voltage applied to Analog inputs		Max[-0.3, (RX_GND-0.3)]	Min[4, (RX_SUP+0.3)]	V
Voltage applied to Digital inputs		Max[-0.3, (RX_GND-0.3)]	Min[4, (IO_SUP+0.3)]	V
Max duty cycle(Cumulative): Sum of all LED phase durations as a fraction of total period	50mA LED current mode(ILED Shift=0)		10	%
	100mA LED current mode(ILED Shift=1)		3	%

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Min.	Typ	Max.	Units
RX_SUP		2		3.6	V
IO_SUP		1.7		MIN(3.6, RX_SUP)	V
TX_SUP		[3.0 or (0.5 + VLED)(1) whichever is greater]		5.25	V
Digital Inputs			0 to IO_SUP		V
Analog inputs			0 to IO_SUP		V
Operating temperature range		-30		85	°C
Storage temperature range		-40		100	°C

(1) VLED refers to the maximum voltage drop across the external LED (at maximum LED current). This is usually governed by the forward drop voltage(V_{FB}) of the LED.

2.3 Electrical characteristics

Minimum and maximum specifications are at TA = –20°C to 70°C, typical specifications are at 25°C. TX_SUP = 4 V, RX_SUP = IO_SUP = 3V, 100 Hz PRF, 8 MHz external clock (with CLKDIV_EXTMODE set to Divide by 2), detector Cin=50 pF, CLKDIV_PRF set to 1, (unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
PRF – Pulse repetition frequency(1)		10(2)		1000	SPS
Receiver					
DC cancellation DAC current range		-7		7	uA
DC cancellation DAC current step			0.47		uA
TIA gain setting		10K		2M	Ω
Cf setting		2.5		25	pF
Switched RC filter bandwidth			2.5(3)		kHz
ADC averages		1		16	
ADC resolution				24	Bit
Transmitter					
LED current range	ILED_2X=0	0		50	mA
	ILED_2X=1	0		100	
LED current resolution			6		Bits
Clocking – Internal Oscillator					
Frequency			4		MHz
Accuracy	Room temperature		±1		%
Frequency drift with temperature	Full temperature range		±0.5		%
jitter (RMS)			100		Ps
Output clock high level			IO_SUP		V
Output clock low level			0		V
Output clock rise/fall times	10-90%, 15pF load cap on CLK		<30		ns
Clocking – External Oscillator					
Frequency range(4)		4		60	MHz
Input clock high level			IO_SUP		V
Input clock low level			0		V
Input capacitance of CLK pin	Capacitance to ground		<4		pF
I2C Interface					
Max clock speed			400		kHz
I2C Slave address			0x58		
Performance					
CMRR	f_{CM} = 50Hz and 60Hz		80		dB
PSRR	f_{CM} = 50Hz and 60Hz		85		dB
Receiver SNR	SNR over 20Hz bandwidth for 500kΩ gain setting, 50% FS output , 2% LED and sampling pulse width, ADC average set to 16		100		dBFS(5)
Transmitter SNR	SNR over 20Hz bandwidth For 50mA LED current setting		100		dBFS(5)

(1) PRF refers to the rate at which samples from each of 4 phases are output from the AFE.
(2) To extend the lower range of PRF down to 10 Hz, program the CLKDIV_PRF setting.
(3) The effective bandwidth of the Switched RC filter scales as a function of the sampling duty cycle. For example, at 2% sampling width duty cycle, effective bandwidth of the Switched RC filter is about 50 Hz.
(4) With appropriate setting of clock divider ratio (CLKDIV_EXTMODE).
(5) dBFS here refers to a full scale voltage of 2V

2.3 Electrical characteristics(continued)

Minimum and maximum specifications are at TA = –20°C to 70°C, typical specifications are at 25°C. TX_SUP = 4 V, RX_SUP = IO_SUP = 3V, 100 Hz PRF, 8 MHz external clock (with CLKDIV_EXTMODE set to Divide by 2), detector Cin=50 pF, CLKDIV_PRF set to 1, (unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Current consumption					
RX_SUP current	Normal operation, External clock mode		620		uA
	Normal operation, Internal oscillator mode		670		uA
	In dynamic powerdown mode(6)		300		uA
	Hardware powerdown(PWDN) mode(7)		3		uA
	Software powerdown(PDNAFE) mode(7)		35		uA
IO_SUP current	Normal operation, External clock mode		20		uA
	Normal operation, Internal oscillator mode		5		uA
	In dynamic powerdown mode(6)		20		uA
	Hardware powerdown(PWDN) mode(7)		3		uA
	Software powerdown(PDNAFE) mode(7)		5		uA
TX_SUP current	Normal operation, External clock mode(8)		25		uA
	Normal operation, Internal oscillator mode(8)		25		uA
	In dynamic powerdown mode(6)(8)		5		uA
	Hardware powerdown(PWDN) mode(7)(8)		2		uA
	Software powerdown(PDNAFE) mode(7)(8)		2		uA
Transient recovery					
Recovery from PWDN mode (T_{ACTIVE})	Time for signal chain to be functional(9)		10		ms
Recovery from any event causing a charge in signal characteristics ($T_{CHANNEL}$)	PRF=100Hz, Sampling duty cycle (each phase) of 2%(10)		200		ms
Digital Inputs					
Logic high level, V_{IH}		0.9*IO_SUP	IO_SUP		V
Logic low level, V_{IL}			0	0.1*IO_SUP	V
Digital Outputs					
Logic high level, V_{OH}			IO_SUP		V
Logic low level, V_{OL}			0		V

(6) In Dynamic powerdown for 90% and Active for 10% of the period. With External clock.
(7) External clock mode with external clock switched off
(8) LED currents set to 0
(9) For full performance to be restored, a longer time as governed by $T_{CHANNEL}$ might be applicable.
(10) $T_{CHANNEL}$ scales inversely with the sampling duty cycle.

2.4 LED Characteristics

Table 2. Green LED(LED1) Characteristics. T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Limits			Unit	Remark
		Min	Typ	Max		
V_F	Forward Voltage		2.7	3.2	V	IF=20mA
V_R	Reverse current			2.0	uA	Vr=5V
I_v	Luminous intensity	1300		1700	mcd	IF=20mA
Λ_d	Dominant Wavelength	515		535	nm	IF=20mA
Δλ	Spectrum Width, Half Power		35		nm	IF=20mA

Table 3. IR LED(LED2) Characteristics. T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Limits			Unit	Remark
		Min	Typ	Max		
V_F	Forward Voltage	1.5	1.65	1.7	V	IF=100mA
I_R	Reverse Current			5	uA	Vr=10V
P_o	Radiant Power	18		23	mW	IF=100mA
Λ_p	Peak Wavelength		945		nm	IF=100mA
Δλ	Spectrum Width, Half Power		30		nm	IF=100mA

2.5 Photo diode Characteristics

T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
I_D	Reverse dark current	V_R=10V, Ee=0mW/cm^2			20	nA
$V_{(BR)R}$	Reverse breakdown voltage	I_R=100uA, Ee=0mW/cm^2	33			V
C_t	Total capacitance	V_R=5V, Ee=0mW/cm^2 F=1MHZ		1.6		pF
t_{on}/t_{off}	Turn-on/Turn-off Time	V_R=5V, R_L=50Ω, λ=850nm		50/50		ns
λ	Sensitivity wavelength range	-	300		1100	nm
λ_p	Peak sensitivity wavelength	-		850		nm

3. Detailed Description

3.1 Overview

The PPS964A has an integrated transmitter and receiver for Optical heart rate monitoring applications.
The system is characterized by a parameter called the PRF (Pulse repetition frequency) which determines the periodicity of repetition of a sequence of operations. Every cycle of a PRF results in four 24-bit digital samples at the output of the PPS964A, each of which is stored in a separate register.

3.2 Feature Description

3.2.1 TIA and switched R-C filter

The receiver input pins INP/INM are meant to be connected differentially to a Photodiode. The signal current from the Photodiode is converted to a differential voltage using a TIA (Transimpedance amplifier). The TIA gain is set by its feedback resistor (R_f) and can be programmed from 10K-2M Ω. The transimpedance gain between the input current and output differential voltage of the TIA is equal to $2*R_f$. At the output of the TIA is a switched RC filter. There are 4 parallel instances of the filter and each of them is connected to the TIA output signal during one of 4 sampling phases.
The signal chain is kept fully differential throughout in order to enable excellent rejection of common mode noise as well as noise on power supplies. For ease of illustration, the scheme with the 4 parallel filters is shown in Figure 3 for a single-ended representation of the signal chain. The signal marked as ADCRST corresponds to the collection of the active phases of four ADCRST pulses named as ADCRST0, ADCRST1, ADCRST2, and ADCRST3.

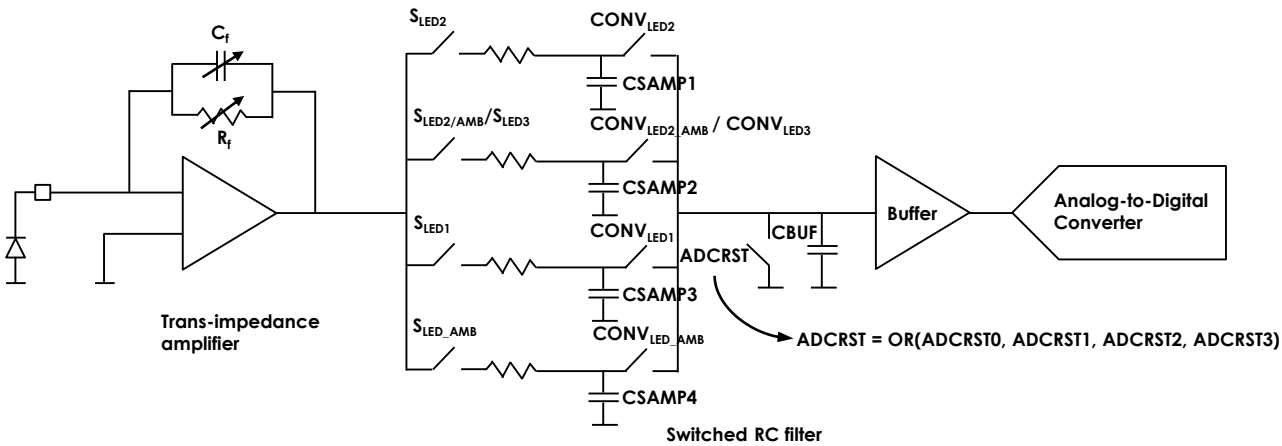


Figure 3. Illustration on Four Phases of Sampling and Conversion

3.2.1.1 Operation with Three LEDs

The 4 sampling phases can correspond to either of the following signal state sequences received by the Photodiode :
3-LED mode: LED2 → LED3 → LED1 → Ambient
The sequence of the phases within a pulse repetition cycle is shown in Figure 4.

Feature Description(continued)

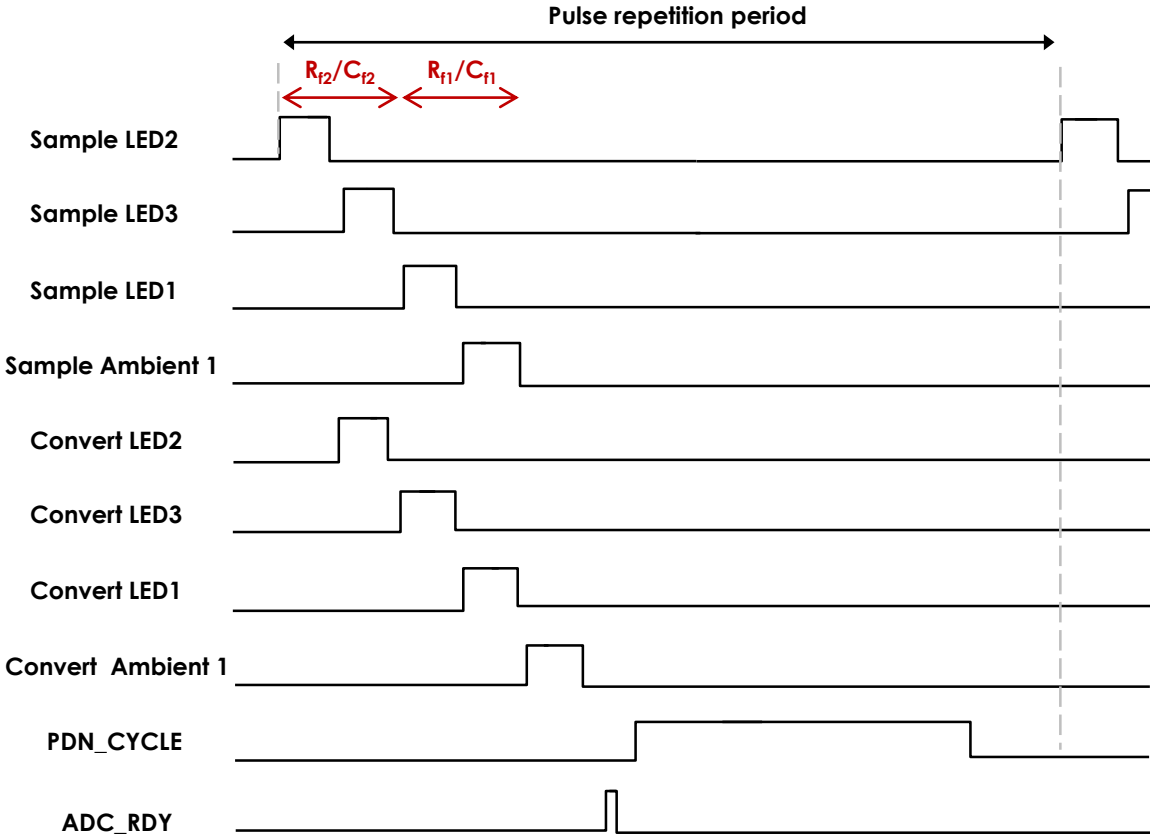


Figure 4. Illustration on Sequence of Four Phases of Sampling and conversion

In the 3-LED mode; LED1, LED2, and LED3 are pulsed during the corresponding sampling instants. As mentioned in TIA Gain settings and Operation with Two and Three LEDs, the TIA gain (R_f) and Feedback capacitor (C_f) can be programmed differently between 2 sets – R_{f1}/C_{f1} and R_{f2}/C_{f2}. The way these sets are applied to the 4 phases is shown in Figure 4.

3.2.1.2 LED Current Setting

The LED current range is from 0-100 mA. The individual currents of each of the three LEDs can be controlled independently, each with a separate 6-bit control.
Taken as a decimal number, the 6-bit setting provides 63 equal steps between 0 mA and 100 mA.
Each increment of the 6-bit code of ILED1 causes the LED1 current setting to increment by roughly 1.6 mA.
For details, see Register 22h (offset = 22h) [reset = 0h].

3.2.1.3 TIA Gain settings

The TIA gain is set by programming the value of R_f, the feedback resistor of the TIA. R_f setting is controlled using the register bit TIA_GAIN. For details see Register 21h (offset = 21h) [reset = 0h]
By default, the same TIA_GAIN setting is applied for all the four phases of the receiver. It is possible to set separate gain for two of the four phases by setting the EN_SEP_GAIN bit. When the EN_SEP_GAIN bit is enabled, TIA_GAIN register controls R_{f1} setting and TIA_GAIN_SEP register controls R_{f2} settings.
The mapping of the R_{f1}/R_{f2} values to the two sets of 3-bit controls are shown in Table 50.

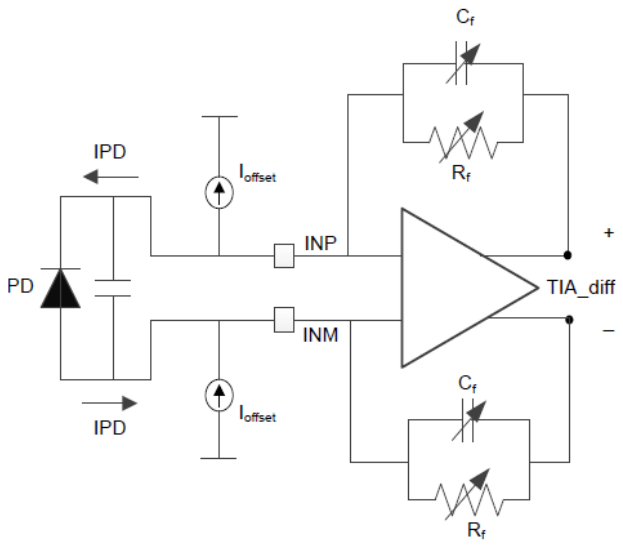
Feature Description(continued)

3.2.1.4 TIA Bandwidth Setting

TIA Bandwidth settings is similar to TIA Gain settings. The TIA bandwidth is set by programming the value of Cf, the feedback capacitance of the TIA. The product of Rf and Cf gives the time constant of the TIA and should be set about 1/5th of the LED/ sampling pulsewidths or less. This is so that the TIA is able to pass the incoming pulses from the photodiode.
Cf is controlled using the register bit TIA_CF. For details, see Register 21h (offset = 21h) [reset = 0h].
By default, the same TIA_CF setting is applied for all the four phases of the receiver. Similar to the TIA gain settings, it is possible to set a separate Cf for two of the four phases by setting the EN_SEP_GAIN bit. When the EN_SEP_GAIN bit is enabled, TIA_CF register controls Cf1 settings and TIA_CF_SEP controls Cf2 settings. The mapping of the Cf1/Cf2 values to the two sets of 3-bit controls are the same as shown in Table 51.

3.2.2 Offset cancellation DAC

Typical optical heart rate signal has a DC component as well as an AC component. While a higher TIA gain maximizes the AC signal at the AFE output, the magnitude of the DC component limits the maximum gain possible in the TIA. In order to decouple the effect of DC level on the allowed AC signal gain, a current DAC is placed at the input of the PPS964A. By setting a programmable cancellation current (based on the DC current signal level), the effective signal that is gained up by the TIA can be reduced. This results in ability to set a higher TIA gain than what would have been possible without enabling the offset correction. In each of the 4 phases of operation, a separate programmable current value can be set by programming 4 different set of register bits. These cancellation currents are automatically presented to the input of the TIA in the appropriate phase. The ability to set a different cancellation current in each of the 4 phases can be used to cancel out the ambient current in the Ambient Phase. In the LED ON phase, this ability can be used to cancel out the sum of the ambient current and DC current of the Heart rate signal. The polarities of signal current and offset cancellation current is shown below. The polarity of the offset cancellation current can be reversed by programming the POL_OFFDAC bits.



With the photodiode connected as shown, In figure 5, the output code of the PPS964A would be positive with the offset cancellation DAC set to zero (Ioffset=0). With Ioffset set negative (POL_OFFFAC=1), a DC offset can be subtracted from the signal, and the AC signal could be amplified with a higher gain than would be otherwise possible.

Figure 5. Illustration on Polarity of offset Cancellation Current

Feature Description(continued)

An illustration of the signal current and voltage levels is shown below for a choice of signal levels.
In the below table, a parameter called CTR (current transfer ratio) is used to depict the relation between the set LED current and the resultant photodiode current (IPD). It is a function of the optical and mechanical parameters as well as the human physiology.

Phase	ILED mA	CTR uA/ mA	Isig uA	Iamb uA	IPD uA	Ioffset uA	Ieff uA	Rf Meg	TIA diff
LED2	25	0.025	0.625	1	1.625	-1.4	0.225	1	0.45
LED3	50	0.025	1.25	1	2.25	-1.87	0.38	0.5	0.38
LED1	12.5	0.025	0.3125	1	1.3125	-0.93	0.3825	0.5	0.3825
AMB1	0	0.025	0	1	1	-0.93	0.07	2	0.28

ILED: Set LED current
CTR: Current transfer ratio (in uA/mA)
Isig: Photodiode current because of LED pulsing (Isig = ILED*CTR)
Iamb: Ambient current (which is there in all phases and adds to Isig)
IPD: Total input current (Isig+Iamb)
Ioffset: Current setting of offset cancellation DAC
Ieff: Effective current after offset cancellation (IPD+Ioffset)
Rf: TIA gain setting
TIA diff: Output differential signal of the TIA(note that this should be within the range of +/-1V

3.2.2.1 Offset Cancellation DAC controls

The bits marked as I_OFFDAC control the magnitude of the current subtracted (or added) at the TIA input. The bits marked as POL_OFFDAC control the polarity of the current and determine whether the current is subtracted from the input or added to it. For details see Register 3Ah (offset = 3Ah) [reset = 0h]

3.2.3 ADC

The PPS964A has an ADC that provides a 22-bit representation of the current from the photodiode. The code can be read out from a 24-bit registers in Twos complement format. The ADC full scale input range is +/-1.2V and fills up bits 21..0. The two MSBs handle the case where the ADC input voltage exceeds the full scale range.

Table 5. Mapping of ADC Input Voltage to ADC code

Differential Input Voltage at ADC Input	24-bit ADC Output Code
-1.2V	111000000000000000000000
$(-1.2/2^{21})$V	111111111111111111111111
0	000000000000000000000000
$(+1.2/2^{21})$V	000000000000000000000001
+1.2V	000111111111111111111111

The two MSBs of the 24-bit word serve as sign extension bits to the 22-bit ADC code and are equal to MSB of the 22-bit ADC code when the input to the ADC is within its full scale range. See Table 6

Table 6. Using Sign Extension Determine Input Operating Voltage

Bits[23:21]	State of Input
000	Positive and Lower than positive full scale (Within fullscale range)
111	Negative and Higher than negative full scale (Within fullscale range)
001	Positive and Higher than positive full scale (Outside fullscale range)
110	Negative and Lower than negative full scale (Outside fullscale range)

It is to be noted that the TIA has an operating range of +/-1V even though the ADC input full scale range is +/-1.2V. This is illustrated below.

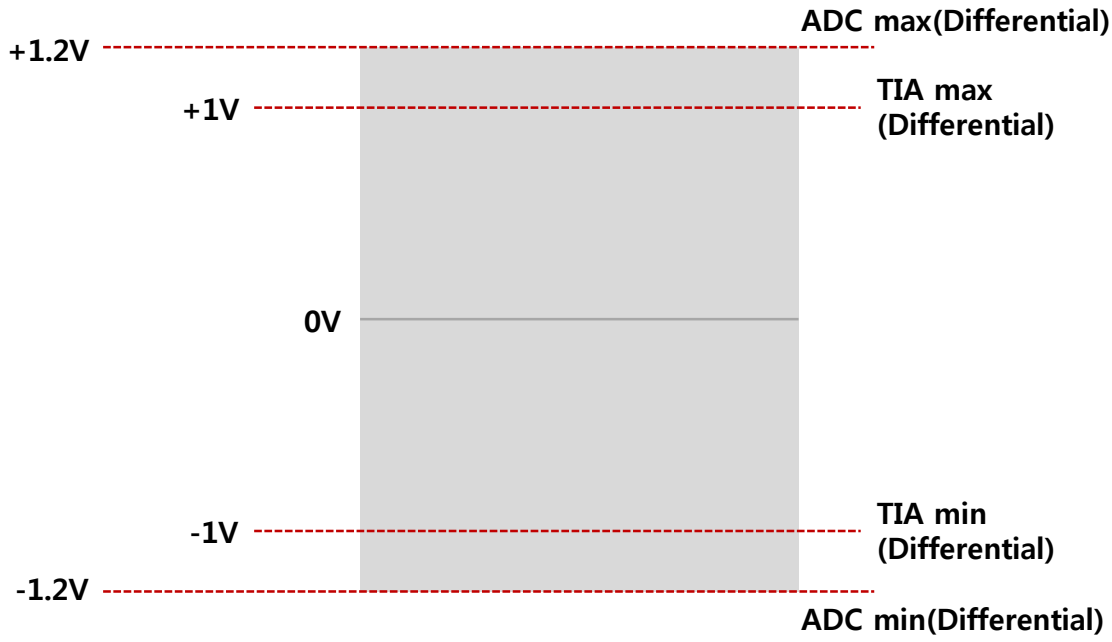


Figure 6. TIA and ADC Dynamic Ranges

3.2.4 I2C interface

The PPS964A has an I2C interface for communication that can run up to 400 kHz. The I2C_CLK and I2C_DAT lines require external pull-up resistors to IO_SUP.
The DATA on I2C_DAT should be stable during the high level of I2C_CLK and may transition during the low level of I2C_CLK as shown in Figure 7.

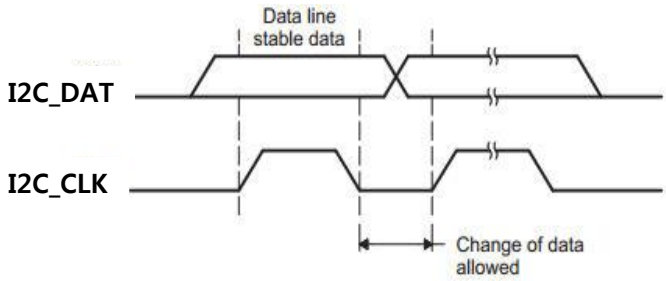


Figure 7. Allowed Window for Data Transition

The START condition is indicated by a High to Low transition of the I2C_DAT line when the I2C_CLK is high. A STOP condition is indicated by a Low to High transition of the I2C_DAT line when the I2C_CLK is high.

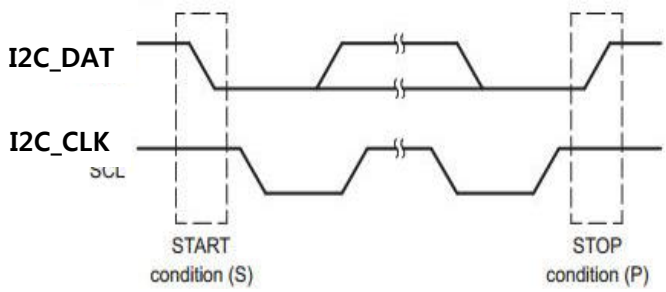


Figure 8. Start and Stop Condition

With the above mentioned protocols for Data, START and STOP conditions, the Write and Read operation are as shown in Figure 9 and Figure 10 respectively. operations are as shown in the next page. In the diagrams, the slave address for the PPS964A (indicated as SA6..SA0) is a 7-bit representation of the number 0x58. The bit marked as R/W is the Read/Write bit.
Only the ADC output registers (addressed from 42-47) are available for read-out.
In these diagrams, the activity done by the host is shown in Black whereas the activity from the PPS964A is shown in Red. So during Write operation, after the Host has sent the slave address, the PPS964A pulls the I2C_DAT line low (shown as ACK) if the slave address matches with 0x58. Similarly, the host pulls the I2C_DAT line high (shown as NACK) as acknowledgement of a successfully completed Read operation involving 3 bytes of data. Continuous read/ write mode is not supported.

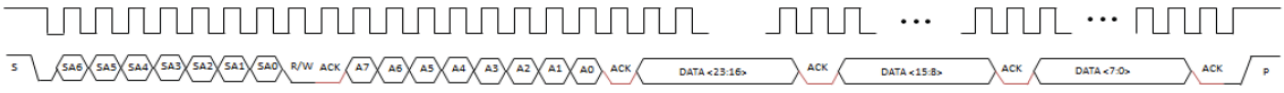


Figure 9. I2C Write Option Timing

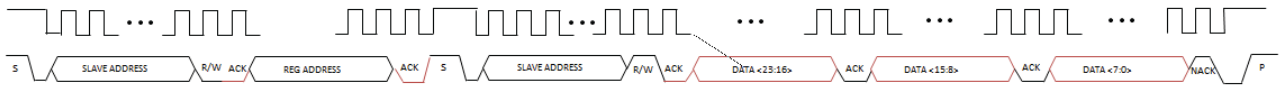


Figure 10. I2C Read Option Timing

3.2.5 Timing Engine

The AFE has a fully integrated timing engine which can be programmed to generate all the clock phases for synchronized transmit drive, receive sampling and data conversion. To enable the timing engine (after powering up the device), enable the TIMEREN bit.

3.2.5.1 Timer and PRF Controls

The timing engine inside the AFE has a 16-bit counter. The duration of the count with respect to an internal clock (the Timer clock) determines the pulse repetition period. The PRF (Pulse repetition frequency) can be set using the PRPCT register bits, which represent the high value of the counter (the low value of the counter is 0). The counter automatically counts till PRPCT and returns back to 0 to start the next count. To suspend the count and keep the counter in reset state, enable the TM_COUNT_RST bit.

3.2.5.2 Timing control registers

The start and stop counts for the various dynamic signals generated by the timing engine are shown in Table 7. The timing edge numbers are referenced to the Figure 11.

Table 7. Timing Register and Edge Details

Timing control notation	Description	Register Address (Hex)	Timing Edge
LED2STC	Sample LED2 start	1h	TE3
LED2ENDC	Sample LED2 end	2h	TE4
LED1LEDSTC	LED1 start	3h	TE17
LED1LEDENDC	LED1 end	4h	TE18
ALED2STC\ LED3STC	Sample Ambient 2 (or Sample LED3) start	5h	TE11
ALED2ENDC\ LED3ENDC	Sample Ambient 2 (or Sample LED3) end	6h	TE12
LED1STC	Sample LED1 start	7h	TE19
LED1ENDC	Sample LED1 end	8h	TE20
LED2LEDSTC	LED2 start	9h	TE1
LED2LEDENDC	LED2 end	Ah	TE2
ALED1STC	Sample Ambient 1 start	Bh	TE25
ALED1ENDC	Sample Ambient 1 end	Ch	TE26
LED2CONVST	LED2 convert phase start	Dh	TE7
LED2CONVEND	LED2 convert phase end	Eh	TE8
ALED2CONVST\ LED3CONVST	Ambient 2(or LED3) convert phase start	Fh	TE15
ALED2CONVEND\ LED3CONVEND	Ambient 2(or LED3) convert phase end	10h	TE16
LED1CONVST	LED1 convert phase start	11h	TE23
LED1CONVEND	LED1 convert phase end	12h	TE24
ALED1CONVST	Ambient 1 convert phase start	13h	TE29
ALED1CONVEND	Ambient 1 convert phase end	14h	TE30
ADCRSTSTCT0	ADC reset phase 0 start	15h	TE5
ADCRSTENDCT0	ADC reset phase 0 end	16h	TE6
ADCRSTSTCT1	ADC reset phase 1 start	17h	TE13
ADCRSTENDCT1	ADC reset phase 1 end	18h	TE14
ADCRSTSTCT2	ADC reset phase 2 start	19h	TE21
ADCRSTENDCT2	ADC reset phase 2 end	1Ah	TE22
ADCRSTSTCT3	ADC reset phase 3 start	1Bh	TE27
ADCRSTENDCT3	ADC reset phase 3 end	1Ch	TE28

When 3 LEDs are to be used within a single period, the receiver timing controls corresponding to the third LED correspond to the phase marked as Ambient 2 in the above table. The timing controls for driving the third LED are as shown in Table 8.

Table 8. Timing Controls for Driving the Third LED

Timing control notation	Description	Register Address (Hex)	Timing Edge
LED3LEDSTC	LED3 start	36h	TE9
LED3LEDENDC	LED3 end	37h	TE10

The timing diagram for the case where all 3 LEDs are active is shown in Figure 11.

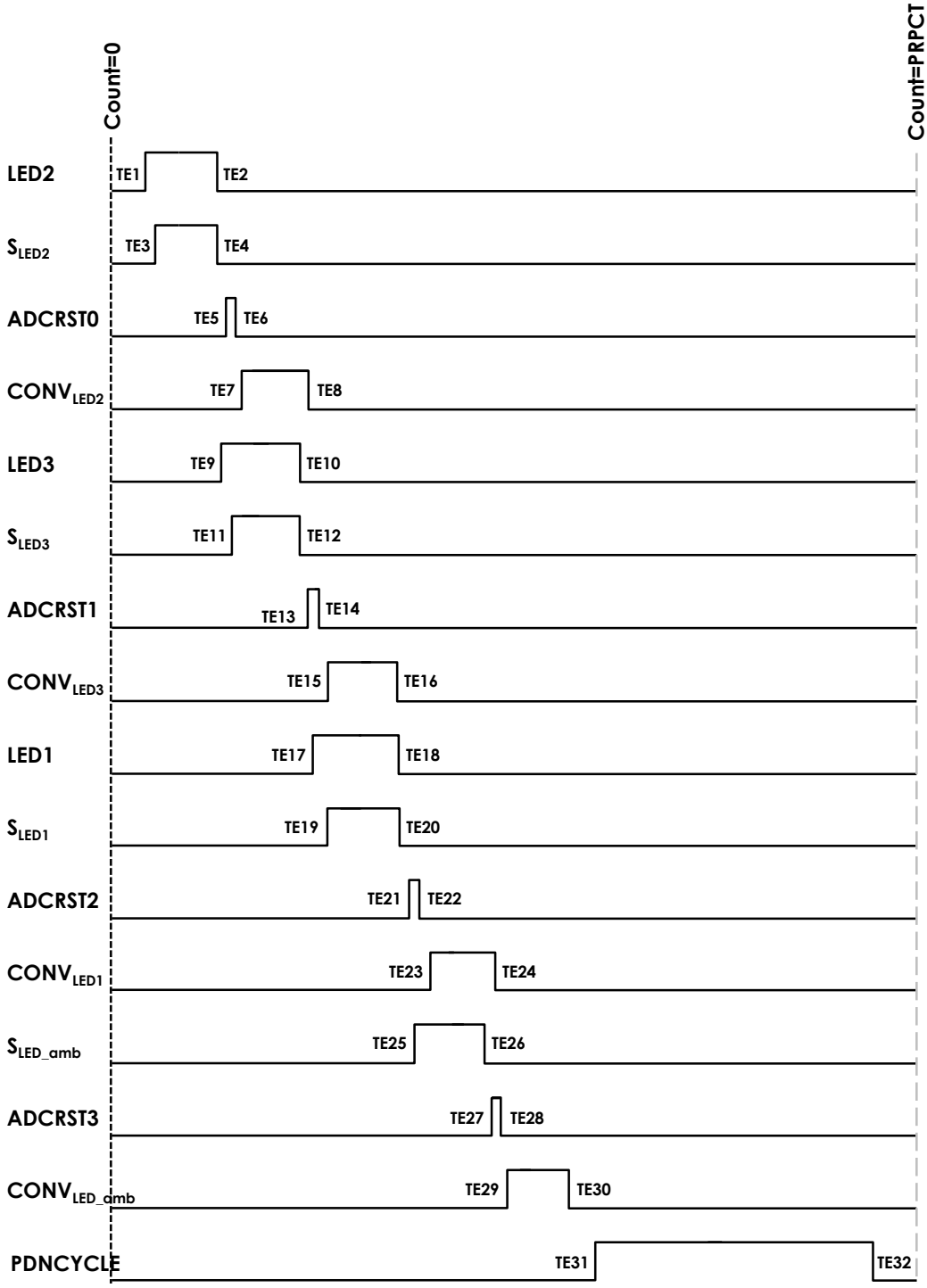


Figure 11. Timing Diagram

3.2.5.3 Receiver timing

The timing engine can be programmed to set the different phases of the receiver. The relative timings of the LED phase, sampling phase, ADC reset phase and ADC conversion phase are shown in Figure 12 and Table 9.

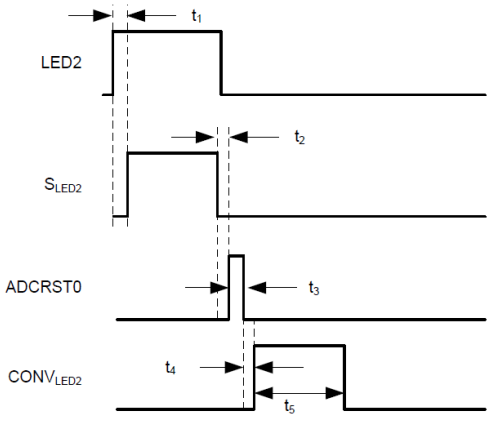


Figure 12. Receiver Timing Guidelines

Table 9. Receiver Timing Details

	Description	Min value	Max value
T1	Start of LED to start of sampling	Max [25, (0.2*LED pulse duration)] us	
T2	End of LED to start of ADC Reset phase	2 count(1)	
T3	Duration of ADC reset phase	6 count	
T4	End of ADC reset phase to start of ADC Conversion phase	2 count	2 count
T5	Duration of ADC Conversion phase(2)	[(NUMAV+2)* 200*T_{ADC}+15](3) us	

(1) "Count" refers to 1 clock period of CLK_TE
(2) See Figure 15 for notations of the clocking domain.
(3) $T_{ADC} = 1/f_{ADC}$

The fourth of the ADCRST* signals in a period also defines the start of the ADC_RDY pulse. The rising edge of the ADC_RDY signal can be used as an interrupt by the MCU to read out the registers corresponding to the preceding 4 conversions in that period.

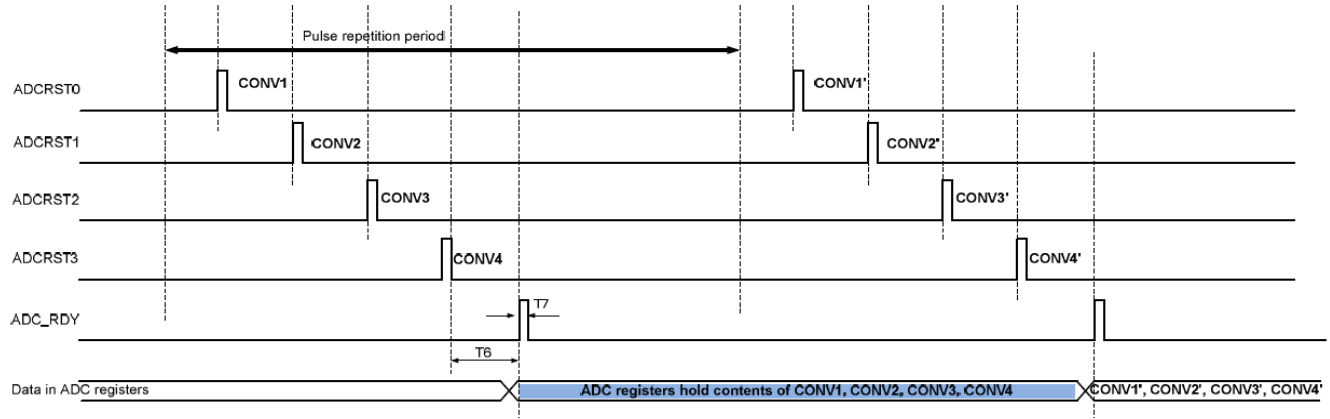


Figure 13. ADC_RDY Generation Scheme

Table 10. ADC_RDY Timing Details

Parameter	Description	Typ value[us]	Max value [us]
T6	End of 4th ADC Reset phase to start of ADC_RDY pulse	(NUMAV+1)*200*T_{ADC}	(NUMAV+2)*200*T_{ADC} + 15
T7	Width of ADC_RDY pulse	T_{ADC}(1)	

(1) If a lager pulse width is needed for the ADC_RDY interrupt, use PROG_TG_EN to enable a programmable timing signal to come out of the ADC_RDY pin. The location of the signal can be using the PROG_TG_STC and PROG_TG_ENDC counts.

3.2.5.4 Dynamic Powerdown Timing

The dynamic powerdown feature can be used to shut down the receiver inside every cycle to save power. See Figure 14 and Table 11 .

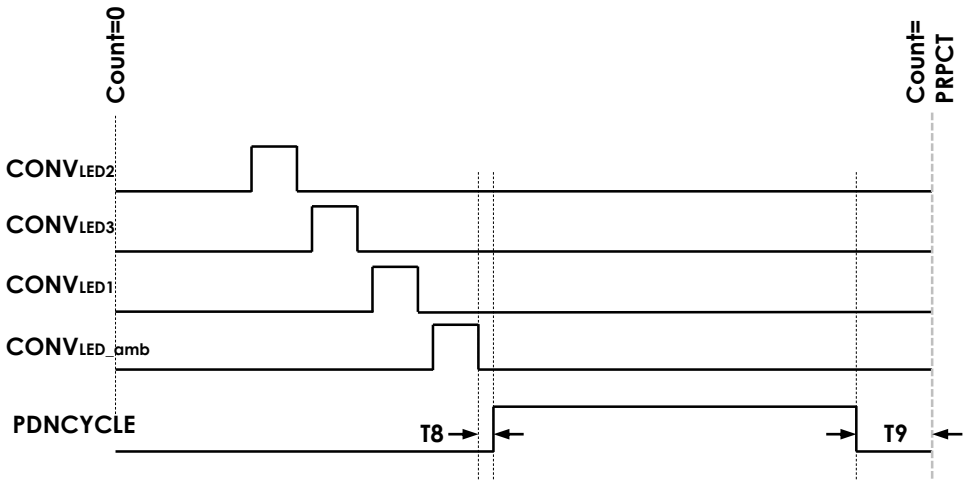


Figure 14. Dynamic Powerdown Timing Diagram

Table 11. Dynamic Powerdown Timing Details

Parameter	Description	Recommended min value
T8	End of 4th conversion phase to the start of PDNCYCLE	200 us
T9	End of PDNCYCLE to start of next period	200 us

Table 12. Timing Controls for Dynamic Powerdown

Timing Control Notation	Description	Register Address	Timing Edge(1)
PDNCYCLESTC	PDNCYCL Start	32h	TE31
PDNCYCLEENDC	PDNCYCL End	33h	TE32

(1) Refer to Figure 11

3.2.5.5 Sample Register Values

Table 13 shows a sample of the register settings for generating the different timing signals. These sample settings correspond to a CLK_INT=4 MHz and a PRF of 100 Hz. Three LEDs are used in a cycle, each with a duty cycle of 1%, which corresponds to a pulse width of 100 us. The conversion widths are set so as to accommodate 4 averages (NUMAV=3). Two cases are shown – one for a CLKDIV_PRF=1 (CLK_TE=4 MHz) and the other for a CLKDIV_PRF=16 (CLK_TE = 250 kHz). The dynamic power-down signal (PDNCYCLE) is set such that the AFE is in power-down mode for about 87% of the time each cycle.

Table 13. Sample Register Settings

Signal[1]	Register Field	No division of clock to Timing Engine Clock CLKDIV_PRF=1		ADC clock to Timing Engine Clock divided by 16 CLKDIV_PRF=16	
		Time duration(us)	Register setting[2]	Time duration(us)	Register setting[2]
	PRPCT	10000	39999[3]	10000	2499[3]
LED2	LED2LEDSTC	100	0	100	0
	LED2LEDENDC		399		24
S_{LED2}	LED2STC	80	80	80	5
	LED2ENDC		399		24
ADCRST0	ADCRSTSTCT0	1.75	401	8	26
	ADCRSTENDCT0		407		27
$CONV_{LED2}$	LED2CONVST	265	408	268	28
	LED2CONVEND		1467		94
LED3	LED3LEDSTC	100	400	100	25
	LED3LEDENDC		799		49
S_{LED3}	ALED2STC LED3STC	80	480	80	30
	ALED2ENDC LED3ENDC		799		49
ADCRST1	ADCRSTSTCT1	1.75	1469	8	96
	ADCRSTENDCT1		1475		97
$CONV_{LED3}$	ALED2CONVST LED3CONVST	265	1476	268	98
	ALED2CONVEND LED3CONVEND		2535		164
LED1	LED1LEDSTC	100	800	100	55
	LED1LEDENDC		1199		74
S_{LED1}	LED1STC	80	880	80	55
	LED1ENDC		1199		74
ADCRST2	ADCRSTSTCT2	1.75	2537	8	166
	ADCRSTENDCT2		2543		167
$CONV_{LED1}$	LED1CONVST	265	2544	268	168
	LED1CONVEND		3603		234
S_{LED_AMB}	ALED1STC	80	1279	80	79
	ALED1ENDC		1598		98
ADCRST3	ADCRSTSTCT3	1.75	3605	8	236
	ADCRSTENDCT3		3611		237
$CONV_{LED\_AMB}$	ALED1CONVST	265	3612	268	238
	ALED1CONVEND		4671		304
PDNYCLE	PDNCYCLESTC	8432.25	5471	8384	354
	PDNCYCLEENDC		39199		2449

(1) For signal names, refer Figure 3.
(2) Time duration = (End count – Start count + 1) / F_{TE}
(3) For PRPCT, start count = 0

3.3 Device Functional Modes

3.3.1 Power modes

The PPS964A has the following power modes:
1. Normal mode
2. Hardware powerdown mode(PWDN) – this is set using the RESETZ pin. When the RESETZ pin is pulled low for greater than 200 us , the device enters in Hardware powerdown mode where the power consumption is very low (few uA)
3. Software powerdown mode(PDNAFE) using a register bit
4. Dynamic powerdown mode – this is enabled by set the start and end points of a signal called PDN_CYCLE which is controlled using the Timing engine. During the high phase of PDN_CYCLE, the blocks (as selected by the DYNAMIC* bits) are powered down. When choosing to powerdown the TIA in the dynamic powerdown mode, consideration has to be given to the dynamics of the photodiode. With the TIA powered down, there is no longer any feedback mechanism to maintain zero bias across the photodiode. This can result in a drifting of the voltage across the photodiode. When the AFE comes out of dynamic powerdown into the active mode, it can result in a transient recovery time for the photodiode. The INP/INM nodes can be additionally shorted through a switch to an internal reference voltage (VCM) to keep the photodiode in zero bias whenever the TIA is in powerdown mode. This is done by setting the bit ENABLE_INPUT_SHORT to '1'. By setting this bit in conjunction with the DYNAMIC3 bit, the dynamics of the photodiode can be controlled better during the dynamic powerdown mode.

3.3.2 RESET modes

The PPS964A has internal registers that need to be reset before valid operation. There are 2 ways to reset the device :
1. RESETZ pin – a reset signal can be issued by pulsing the RESETZ pin low for a time between 25 to 50 us.
2. Software RESET register bit SW_RESET.

3.3.3 Clocking modes

The PPS964A has an internal oscillator that can generate a 4 MHz clock. This clock can be made to come out of the CLK pin for use by the rest of the system.

The default mode is to use an external clock. The frequency range of this external clock is between 4-60 MHz. A programmable internal division ratio between 1-12 needs to be set so that the divided clock is between 4-6 MHz.

The accuracy of the internal oscillator is +/-2.5% (TBD). So for high accuracy measurements, it is preferable to operate the PPS964A using an input (external) clock that has high accuracy. If a high accuracy measurement is required while using the internal oscillator, a correction scheme could be used in the MCU to digitally compensate for the inaccuracy in the oscillator. One method of doing this would be to accurately estimate the PRF by measuring the ADC_RDY periodicity in terms of a high-accuracy MCU clock (for example, a 32 kHz clock) to establish the accurate PRF. This information can then be used to digitally correct the heart rate computation.

3.3.4 PRF programmability

By default, the internal clock is 4 MHz. This clock also goes to the timing engine which has a 16-bit counter. The maximum setting of this counter (all 16 bits set to '1') determines the lowest value of PRF. This results in a minimum PRF of 62.5 Hz. To extend the lower range of PRF, an independent programmable divider is introduced in the clock going to the Timing engine. By programming this divider between 1-16, the lower range of PRF can be extend from 62.5 Hz to 3.90625 Hz (limit minimum PRF to 10 Hz).

The various clocking domains and controls are illustrated in Figure 15.

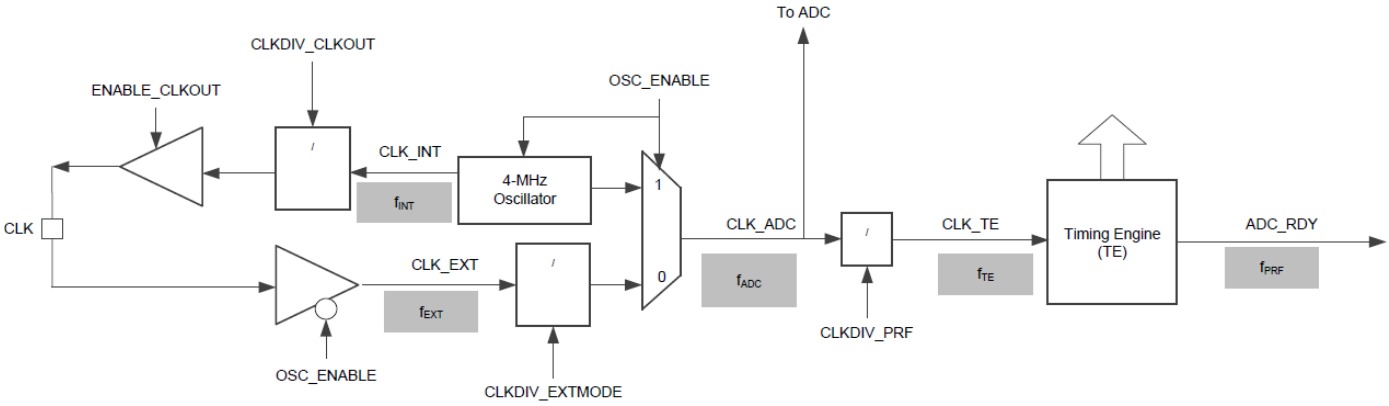


Figure 15. Clocking Domains Illustration

Table 14. Clocking Domains and Operation Range

Clock	Description	Freq.	Freq. range	Comments
CLK_INT	Clock generated by internal oscillator	F_{INT}	4 MHz(1)	Internal clock when Oscillator is enabled
CLK_EXT	External clock	F_{EXT}	4-60 MHz	Set division ratio using CLKDIV_EXTMODE such that CLK_ADC is 4-6 MHz
CLK_ADC	Clock used by the ADC for conversion	F_{ADC}	4-6 MHz	Selected as either internal clock or divided version of external clock
CLK_TE	Clock used by the timing engine	F_{TE}	F_{ADC} divided by 1-16	Division ratio set by CLKDIV_PRF
ADC_RDY	Interrupt to MCU at the rate same as the PRF	F_{PRF}	Limit to 10-1000 Hz Also Limit to 1000/(Division ratio as set by CLKDIV_PRF)	Set by PRPCOUNT and F_{TE}

(1) See the Electrical Characteristics table for the accuracy of the internal oscillator.

3.3.5 Averaging Modes

To reduce the noise, input to the ADC (Sampled on the CSAMPx Capacitors) can be converted by the ADC multiple times and averaged. The number of averages is set using the register control NUMAV based on the equation:

Number of averages = (NUMAV+1).

By default, NUMAV = 0. So the default mode corresponds to the ADC converting its input once in each of the 4 phases and storing the content into the register corresponding to that phase.

When NUMAV is programmed, for example if NUMAV = 3, then the ADC converts its input four times in each phase, averages the four conversions and stores the averaged value in the register corresponding to that phase.

Since the input to the ADC is the same (corresponding to the voltage sampled on the four CSAMPx caps in Figure 3), averaging only helps to reduce the ADC noise. Number of samples that can be averaged ranges from 1 to 16 (NUMAV programmed from 0 to 15). Higher the number of averages, larger the conversion time needs to be. This is shown in Table 9.

The averaging is implemented in the following manner:
The number of ADC samples corresponding to the number of averages (NUMAV+1) are accumulated.

$$\text{SUMADC} = \sum_{i=1}^{(NUMAV+1)} (ADCi)$$

Where ADCi is the i^{th} sample converted by the ADC. The accumulator output, SUMADC is then divided by a factor 'D' which is realized as D = 128 ÷ X , X being an integer.
Averaged output = ADCOUT = SUMADC ÷ D
Where D = 128 ÷ X, X being an integer.
The above implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from ideal values for other settings. This is illustrated in Table 15.

Table 15. Averaging Mode Settings

NUMAV	Number of averages	X	Division factor, D
0	1	128	1.0
1	2	64	2.0
2	3	43	2.97
3	4	32	4.0
4	5	26	4.92
5	6	21	6.10
6	7	18	7.11
7	8	16	8.0
8	9	14	9.14
9	10	13	9.85
10	11	12	10.67
11	12	11	11.64
12	13	10	12.8
13	14	9	14.22
14	15	9	14.22
15	16	8	16.0

3.3.6 Decimation Mode

The AFE4404 has a decimation mode that can be used to improve the performance at low pulse repetition frequencies (PRFs). In this mode, up to N (N = 2, 4, 8, or 16) consecutive data samples can be averaged. The averaged output comes out one time every N clock cycles. The ADC_RDY frequency also reduces to PRF / N.

A timing diagram is shown in Figure 37 for where the decimation factor = 4 and PRF = 100 Hz. Figure 37 is only intended to illustrate the change in periodicity of ADC_RDY and the update rate of the registers relative to the pulse repetition period. However, the timing of all other signals continues to be as per the descriptions mentioned in the *Timing Engine section*.

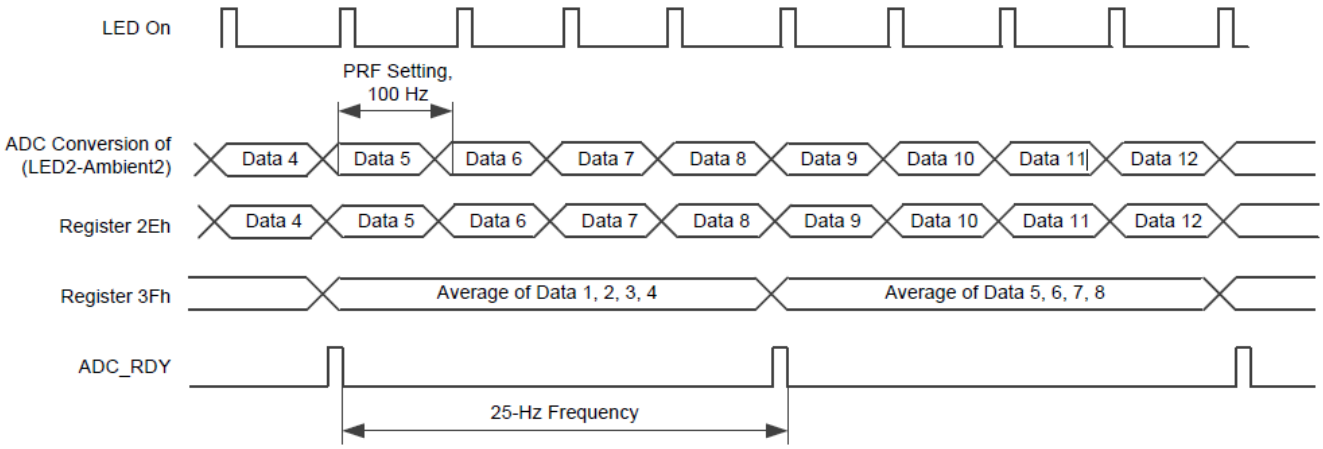


Figure 16. Decimation mode enabled timing diagram
(Decimation factor =4, PRF = 100 Hz)

3.3.6.1 Decimation Mode Power and Performance

The main advantage of the decimation mode is that this mode can be used to reduce the readout rate of the MCU because the data rate reduces by the decimation factor. Normally, reducing the data rate leads to SNR loss. However, with decimation mode, there is no SNR loss regardless of the lower data rate because of the averaging of consecutive samples. Table 16 compares different modes of operation.

Table 16. Different modes of operation

Mode	Rate of device samples and conversions	Rate of MCU data reads	Relative performance
No decimation, 100Hz PRF	100 Hz	100 Hz	Reference
No decimation, 25Hz PRF	25Hz	25 Hz	SNR is approximately 6dB lower than reference
4X decimation mode, 100Hz PRF	100 Hz	25 Hz	SNR is comparable to reference

3.4 Register Map

Register Address (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h																					SW_RESET		TM_COUNT_RST	REG_READ
01h	LED2STC																							
02h	LED2ENDC																							
03h	LED1LEDSTC																							
04h	LED1LEDENDC																							
05h	ALED2STC																							
06h	ALED2ENDC																							
07h	LED1STC																							
08h	LED1ENDC																							
09h	LED2LEDSTC																							
0Ah	LED2LEDENDC																							
0Bh	ALED1STC																							
0Ch	ALED1ENDC																							
0Dh	LED2CONVST																							
0Eh	LED2CONVEND																							
0Fh	ALED2CONVST																							
10h	ALED2CONVEND																							
11h	LED1CONVST																							
12h	LED1CONVEND																							
13h	ALED1CONVST																							
14h	ALED1CONVEND																							
15h	ADCRSTSTCT0																							
16h	ADCRSTENDCT0																							
17h	ADCRSTSTCT1																							
18h	ADCRSTENDCT1																							
19h	ADCRSTSTCT2																							
1Ah	ADCRSTENDCT2																							
1Bh	ADCRSTSTCT3																							
1Ch	ADCRSTENDCT3																							
1Dh	PRPCT																							
1Eh																TIMEREN					NUMAV			
20h									ENSEPGAIN										TIA_CF_SEP			TIA_GAIN_SEP		

Register Map(continued)

Register Address (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21h																PROG_TG_EN			TIA_CF			TIA_GAIN		
22h							ILED3						ILED2						ILED1					
23h				DYNAMIC1			ILED_SHIFT			DYNAMIC2					OSC_ENABLE					DYNAMIC3	DYNAMIC4		PDNRX	PDNAFE
28h																								
29h															ENABLE_CLKOUT					CLKDIV_CLKOUT				
2Ah	LED2VAL																							
2Bh	ALED2VAL																							
2Ch	LED1VAL																							
2Dh	ALED1VAL																							
2Eh	LED2-ALED2VAL(1)																							
2Fh	LED1-ALED1VAL																							
31h																			ENABLE_INPUT_SHORT			CLKDIV_EXTMODE		
32h									PDNCYCLESTC															
33h									PDNCYCLEENDC															
34h									PROG_TG_STC															
35h									PROG_TG_ENDC															
36h									LED3LEDSTC															
37h									LED3LEDENDC															
39h																						CLKDIV_PRF		
3Ah					POL_OFFDAC_LED1	I_OFFDAC_LED1				POL_OFFDAC_AMB1	I_OFFDAC_AMB1				POL_OFFDAC_AMB2	I_OFFDAC_AMB2				POL_OFFDAC_LED2	I_OFFDAC_LED2		
3Dh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEC_EN	0	DEC_FACTOR			0
3Fh	AVG_LED2 – ALED2VAL																							
40h	AVG_LED1 – ALED1VAL																							

(1)Ignore the content of this register when LED3 is used.

3.4.1 Register 0h(offset = 0h) [reset = 0h]

Figure 16. Register 0h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	SW_RESET	0	TM_COUNT_RST	REG_READ

Table 17. Register 0h Field Descriptions

Bit	Field	Type	Reset	Descriptions
3	SW_RESET	W	0h	Self clearing reset bit. For Software reset, write '1'.
1	TM_COUNT_RST	W	0h	Used to suspend the count and keep the counter in reset state
0	REG_READ	W	0h	Register readout enable for 'Write' registers (not needed for ADC output 0 REG_READ W 0h registers) 0: Register Write mode 1: Enable the readout of write registers

3.4.2 Register 1h(offset = 1h) [reset = 0h]

Figure 17. Register 1h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2STC							
7	6	5	4	3	2	1	0
LED2STC							

Table 18. Register 1h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2STC	W/R	0h	Sample LED2 start

3.4.3 Register 2h(offset = 2h) [reset = 0h]

Figure 18. Register 2h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2ENDC							
7	6	5	4	3	2	1	0
LED2ENDC							

Table 19. Register 2h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2ENDC	W/R	0h	Sample LED2 end

3.4.4 Register 3h(offset = 3h) [reset = 0h]

Figure 19. Register 3h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1LEDSTC							
7	6	5	4	3	2	1	0
LED1LEDSTC							

Table 20. Register 3h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1LEDSTC	W/R	0h	LED1 start

3.4.5 Register 4h(offset = 4h) [reset = 0h]

Figure 20. Register 4h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1LEDENDC							
7	6	5	4	3	2	1	0
LED1LEDENDC							

Table 21. Register 4h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1LEDENDC	W/R	0h	LED1 end

3.4.6 Register 5h(offset = 5h) [reset = 0h]

Figure 21. Register 5h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED2STC/LED3STC							
7	6	5	4	3	2	1	0
ALED2STC/LED3STC							

Table 22. Register 5h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED2STC/ LED3STC	W/R	0h	Sample Ambient 2 (or Sample LED3) start

3.4.7 Register 6h(offset = 6h) [reset = 0h]

Figure 22. Register 6h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED2ENDC/LED3ENDC							
7	6	5	4	3	2	1	0
ALED2ENDC/LED3ENDC							

Table 23. Register 6h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED2ENDC/ LED3ENDC	W/R	0h	Sample Ambient 2 (or Sample LED3 end

3.4.8 Register 7h(offset = 7h) [reset = 0h]

Figure 23. Register 7h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1STC							
7	6	5	4	3	2	1	0
LED1STC							

Table 24. Register 7h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1STC	W/R	0h	Sample LED1 start

3.4.9 Register 8h(offset = 8h) [reset = 0h]

Figure 24. Register 8h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1ENDC							
7	6	5	4	3	2	1	0
LED1ENDC							

Table 25. Register 8h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1ENDC	W/R	0h	Sample LED1 end

3.4.10 Register 9h(offset = 9h) [reset = 0h]

Figure 25. Register 9h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2LEDSTC							
7	6	5	4	3	2	1	0
LED2LEDSTC							

Table 26. Register 9h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2LEDSTC	W/R	0h	LED2 start

3.4.11 Register Ah(offset = Ah) [reset = 0h]

Figure 26. Register Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2LEDENDC							
7	6	5	4	3	2	1	0
LED2LEDENDC							

Table 27. Register Ah Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2LEDENDC	W/R	0h	LED2 end

3.4.12 Register Bh(offset = Bh) [reset = 0h]

Figure 27. Register Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED1STC							
7	6	5	4	3	2	1	0
ALED1STC							

Table 28. Register Bh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED1STC	W/R	0h	Sample Ambient 1 start

3.4.13 Register Ch(offset = Ch) [reset = 0h]

Figure 28. Register Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED1ENDC							
7	6	5	4	3	2	1	0
ALED1ENDC							

Table 29. Register Ch Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED1ENDC	W/R	0h	Sample Ambient 1 end

3.4.14 Register Dh(offset = Dh) [reset = 0h]

Figure 29. Register Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2CONVST							
7	6	5	4	3	2	1	0
LED2CONVST							

Table 30. Register Dh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2CONVST	W/R	0h	LED2 convert phase start

3.4.15 Register Eh(offset = Eh) [reset = 0h]

Figure 30. Register Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED2CONVEND							
7	6	5	4	3	2	1	0
LED2CONVEND							

Table 31. Register Eh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED2CONVEND	W/R	0h	LED2 convert phase end

3.4.16 Register Fh(offset = Fh) [reset = 0h]

Figure 31. Register Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED2CONVST/LED3CONVST							
7	6	5	4	3	2	1	0
ALED2CONVST/LED3CONVST							

Table 32. Register Fh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED2CONVST /LED3CONVST	W/R	0h	Ambient 2(or LED3) convert phase start

3.4.17 Register 10h(offset = 10h) [reset = 0h]

Figure 32. Register 10h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED2CONVEND/LED3CONVEND							
7	6	5	4	3	2	1	0
ALED2CONVEND/LED3CONVEND							

Table 33. Register 10h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED2CONVEND/ LED3CONVEND	W/R	0h	Ambient 2(or LED3) convert phase end

3.4.18 Register 11h(offset = 11h) [reset = 0h]

Figure 33. Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1CONVST							
7	6	5	4	3	2	1	0
LED1CONVST							

Table 34. Register 11h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1CONVST	W/R	0h	LED1 convert phase start

3.4.19 Register 12h(offset = 12h) [reset = 0h]

Figure 34. Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED1CONVEND							
7	6	5	4	3	2	1	0
LED1CONVEND							

Table 35. Register 12h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED1CONVEND	W/R	0h	LED1 convert phase end

3.4.20 Register 13h(offset = 13h) [reset = 0h]

Figure 35. Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED1CONVST							
7	6	5	4	3	2	1	0
ALED1CONVST							

Table 36. Register 13h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED1CONVST	W/R	0h	Ambient 1 convert phase start

3.4.21Register 14h(offset = 14h) [reset = 0h]

Figure 36. Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ALED1CONVEND							
7	6	5	4	3	2	1	0
ALED1CONVEND							

Table 37. Register 14h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ALED1CONVEND	W/R	0h	Ambient 1 convert phase end

3.4.22 Register 15h(offset = 15h) [reset = 0h]

Figure 37. Register 15h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTSTCT0							
7	6	5	4	3	2	1	0
ADCRSTSTCT0							

Table 38. Register 15h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTSTCT0	W/R	0h	ADC Reset phase 0 start

3.4.23 Register 16h(offset = 16h) [reset = 0h]

Figure 38. Register 16h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTENDCT0							
7	6	5	4	3	2	1	0
ADCRSTENDCT0							

Table 39. Register 16h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTENDCT0	W/R	0h	ADC Reset phase 0 end

3.4.24 Register 17h(offset = 17h) [reset = 0h]

Figure 39. Register 17h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTSTCT1							
7	6	5	4	3	2	1	0
ADCRSTSTCT1							

Table 40. Register 17h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTSTCT1	W/R	0h	ADC Reset phase 1 start

3.4.25 Register 18h(offset = 18h) [reset = 0h]

Figure 40. Register 18h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTENDCT1							
7	6	5	4	3	2	1	0
ADCRSTENDCT1							

Table 41. Register 15h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTENDCT1	W/R	0h	ADC Reset phase 1 end

3.4.26 Register 19h(offset = 19h) [reset = 0h]

Figure 41. Register 19h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTSTCT2							
7	6	5	4	3	2	1	0
ADCRSTSTCT2							

Table 42. Register 19h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTSTCT2	W/R	0h	ADC Reset phase 2 start

3.4.27 Register 1Ah(offset = 1Ah) [reset = 0h]

Figure 42. Register 1Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTENDCT2							
7	6	5	4	3	2	1	0
ADCRSTENDCT2							

Table 43. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTENDCT2	W/R	0h	ADC Reset phase 2 end

3.4.28 Register 1Bh(offset = 1Bh) [reset = 0h]

Figure 43. Register 1Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTSTCT3							
7	6	5	4	3	2	1	0
ADCRSTSTCT3							

Table 44. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTSTCT3	W/R	0h	ADC Reset phase 3 start

3.4.29 Register 1Ch(offset = 1Ch) [reset = 0h]

Figure 44. Register 1Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ADCRSTENDCT3							
7	6	5	4	3	2	1	0
ADCRSTENDCT3							

Table 45. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	ADCRSTENDCT3	W/R	0h	ADC Reset phase 3 end

3.4.30 Register 1Dh(offset = 1Dh) [reset = 0h]

Figure 45. Register 1Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PRPCT							
7	6	5	4	3	2	1	0
PRPCT							

Table 46. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	PRPCT	W/R	0h	Count value for the counter that sets the PRF. The counter automatically counts till PRPCT and returns back to 0 to start the next count.

3.4.31 Register 1Eh(offset = 1Eh) [reset = 0h]

Figure 46. Register 1Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	TIMEREN
7	6	5	4	3	2	1	0
0	0	0	0	NUMAV			

Table 47. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Descriptions
8	TIMEREN	W/R	0h	0: Timer module disabled. 1: Enables Timer module. This enables the timing engine which can be programmed to generate all the clock phases for synchronized transmit drive, receive sampling and data conversion.
[3:0]	NUMAV	W/R	0h	Number of ADC averages. By programming a higher ADC conversion time, the ADC can be set to do multiple conversions and average these multiple conversions to achieve lower noise. This is set using the bit control NUMAV. The number of samples that are averaged is represented by the decimal equivalent of NUMAV+1. For example, NUMAV=0 represents no averaging, NUMAV=2 represents averaging of 3 samples, and NUMAV = 15 represents averaging of 16 Samples.

3.4.32 Register 20h(offset = 20h) [reset = 0h]

Figure 47. Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
ENSEPGAIN	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	TIA_CF_SEP			TIA_GAIN_SEP		

Table 48. Register 20h Field Descriptions

Bit	Field	Type	Reset	Descriptions
15	ENSEPGAIN	W/R	0h	0: Single TIA Gain for all phases 1: Enables two separate sets of TIA gains
[5:3]	TIA_CF_SEP	W/R	0h	When ENSEPGAIN=1, then TIA_CF_SEP is the control for C_{f2} setting
[2:0]	TIA_GAIN_SEP	W/R	0h	When ENSEPGAIN=1, then TIA_GAIN_SEP is the control for R_{f2} setting

3.4.33 Register 21h(offset = 21h) [reset = 0h]

Figure 48. Register 21h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	PROG_TG_EN
7	6	5	4	3	2	1	0
0	0	TIA_CF			TIA_GAIN		

Table 49. Register 21h Field Descriptions

Bit	Field	Type	Reset	Descriptions
8	PROG_TG_EN	W	0h	Replaces the ADC_RDY output with a fully programmable signal from the timing engine. The start and end points of this signal are set using controls PROG_TG_STC and PROG_TG_ENDC
[5:3]	TIA_CF	W/R	0h	When ENSEPGAIN=0, then control for C_f setting(both C_{f1} and C_{f2}). For detail see table 51. When ENSEPGAIN=1, then control for C_{f1} setting
[2:0]	TIA_GAIN	W/R	0h	When ENSEPGAIN=0, then control for R_f setting(both R_{f1} and R_{f2}). For detail see table 50. When ENSEPGAIN=1, then control for R_{f1} setting

Table 50. Register settings for TIA_GAIN

TIA_GAIN / TIA_GAIN_SEP Register Value	R_f
0	500kΩ
1	250kΩ
2	100kΩ
3	50kΩ
4	25kΩ
5	10kΩ
6	1MΩ
7	2MΩ

Table 51. Register settings for TIA_CF

TIA_GAIN / TIA_GAIN_SEP Register Value	R_f
0	5pF
1	2.5pF
2	10pF
3	7.5pF
4	20pF
5	17.5pF
6	25pF
7	22,5pF

3.4.34 Register 22h(offset = 22h) [reset = 0h]

Figure 49. Register 22h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	ILED3	
15	14	13	12	11	10	9	8
ILED3				ILED2			
7	6	5	4	3	2	1	0
ILED2		ILED1					

Table 52. Register 22h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[17:12]	ILED3	W/R	0h	LED3 current control
{11:6}	ILED2	W/R	0h	LED2 current control
[5:0]	ILED1	W/R	0h	LED1 current control Incrementing of LED1 current is Listed in Table 53

Table 53. Register settings for ILED1

ILED1 / ILED2 / ILED3 register Values	LED current setting (mA)
0	0
1	0.8
2	1.6
3	2.4
……	……
63	50

3.4.35 Register 23h(offset = 23h) [reset = 0h]

Figure 50. Register 23h

23	22	21	20	19	18	17	16
0	0	0	DYNAMIC1	0	0	ILED_SHIFT	0
15	14	13	12	11	10	9	8
0	DYNAMIC2	0	0	0	0	OSC_ ENABLE	0
7	6	5	4	3	2	1	0
0	0	0	DYNAMIC3	DYNAMIC4	0	PDNRX	PDNAFE

Table 54. Register 23h Field Descriptions

Bit	Field	Type	Reset	Descriptions
20	DYNAMIC1	W/R	0h	0: Transmitter not powered down 1: Transmitter powered down in Dynamic powerdown mode
17	ILED_SHIFT	W/R	0h	0: Maximum current 50mA Each increment of the 6-bit code of ILED1 causes the LED1 current setting to increment by roughly 0.8 mA 1: Maximum current 100mA
14	DYNAMIC2	W/R	0h	0: ADC not powered down 1: ADC powered down in Dynamic powerdown mode

Table 55. Register 23h Field Descriptions(continued)

Bit	Field	Type	Reset	Descriptions
9	OSC_ENABLE	W/R	0h	0: External clock mode(Default). In this mode, the CLK pin functions as an input pin where the external clock can be input. 1: Enable Oscillator mode. In this mode, 4 MHz internal oscillator gets enabled.
4	DYNAMIC3	W/R	0h	0: TIA not powered down 1: TIA power down in Dynamic powerdown
3	DYNAMIC4	W/R	0h	0: Rest of ADC not powered down 1: Rest of ADC powered down in Dynamic powerdown
1	PDNRX	W/R	0h	0: Normal mode 1: RX portion of the AFE is powered down
0	PDNAFE	W/R	0h	0: Normal mode 1: Entire AFE is powered down

3.4.37 Register 29h(offset = 29h) [reset = 0h]

Figure 52. Register 29h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	ENABLE_CLKOUT	0
7	6	5	4	3	2	1	0
0	0	0	CLKDIV_CLKOUT				0

Table 56. Register 29h Field Descriptions

Bit	Field	Type	Reset	Descriptions
9	ENABLE_CLKOUT	W/R	0h	In the internal clock mode, the internally generated clock can be output on theCLK pin. 0: Disable Clock output. 1: Enables CLKOUT generation and buffering on to CLK pin. The frequency of the clock output on the CLK pin (in the internal clock mode) can be set using a programmable divider controlled by register bit CLKDIV_CLKOUT
[4:1]	CLKDIV_CLKOUT	W/R	0h	Set the frequency of the clock output On the CLK pin(in the internal clock mode). For detail see Table 57

Table 57. Register setting for CLKDLV_CLKOUT

CLKDIV_CLKOUT Register Settings	Division ratio	Frequency of output clock in MHz
0	1	4
1	2	2
2	4	1
3	8	0.5
4	16	0.25
5	32	0.125
6	64	0.0625
7	128	0.03125
8..15	Do not use	Do not use

3.4.38 Register 2Ah(offset = 2Ah) [reset = 0h]

Figure 53. Register 2Ah

23	22	21	20	19	18	17	16
LED2VAL							
15	14	13	12	11	10	9	8
LED2VAL							
7	6	5	4	3	2	1	0
LED2VAL							

Table 58. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	LED2VAL	R	0h	LED2 output code in 24-bit Twos complement formats.

3.4.39 Register 2Bh(offset = 2Bh) [reset = 0h]

Figure 54. Register 2Bh

23	22	21	20	19	18	17	16
ALED2VAL / LED3VAL							
15	14	13	12	11	10	9	8
ALED2VAL / LED3VAL							
7	6	5	4	3	2	1	0
ALED2VAL / LED3VAL							

Table 59. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	ALED2VAL / LED3VAL	R	0h	Ambient 2 or LED3 output code in 24-bit Twos complement formats.

3.4.40 Register 2Ch(offset = 2Ch) [reset = 0h]

Figure 55. Register 2Ch

23	22	21	20	19	18	17	16
LED1VAL							
15	14	13	12	11	10	9	8
LED1VAL							
7	6	5	4	3	2	1	0
LED1VAL							

Table 60. Register 2Ch Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	LED1VAL	R	0h	LED1output code in 24-bit Twos complement formats.

3.4.41 Register 2Dh(offset = 2Dh) [reset = 0h]

Figure 56. Register 2Dh

23	22	21	20	19	18	17	16
ALED1VAL							
15	14	13	12	11	10	9	8
ALED1VAL							
7	6	5	4	3	2	1	0
ALED1VAL							

Table 61. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	ALED1VAL	R	0h	Ambient 1 output code in 24-bit Twos complement formats.

3.4.42 Register 2Eh(offset = 2Eh) [reset = 0h]

Figure 57. Register 2Eh

23	22	21	20	19	18	17	16
LED2-ALED2VAL							
15	14	13	12	11	10	9	8
LED2-ALED2VAL							
7	6	5	4	3	2	1	0
LED2-ALED2VAL							

Table 62. Register 2Eh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	LED2-ALED2VAL(1)	R	0h	LED2-Ambient2 output code in 24-bit Twos complement formats.

(1) Ignore the content of this register when LED3 is used.

3.4.43 Register 2Fh(offset = 2Fh) [reset = 0h]

Figure 58. Register 2Fh

23	22	21	20	19	18	17	16
LED1-ALED1VAL							
15	14	13	12	11	10	9	8
LED1-ALED1VAL							
7	6	5	4	3	2	1	0
LED1-ALED1VAL							

Table 63. Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Descriptions
[23:0]	LED1-ALED1VAL	R	0h	LED1-Ambient1 output code in 24-bit Twos complement formats.

3.4.44 Register 31h(offset = 31h) [reset = 0h]

Figure 59. Register 31h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	ENABLE_INPUT_SHORT	0	0	CLKDIV_EXTMODE		

Table 64. Register 31h Field Descriptions

Bit	Field	Type	Reset	Descriptions
5	ENABLE_INPUT_SHORT	W/R	0h	INP/INN shorted to VCM whenever the TIA is powerdown
[2:0]	CLKDIV_EXTMODE	W/R	0h	Used to set division ratio to allow flexible clocking in the external clock mode. For details see Table 65

Table 65. Register settings for CLKDLV_EXTMODE

CLKDIV_CLKOUT Register Settings	Division ratio	Frequency of output clock in MHz
0	2	8-12
1	8	32-48
2	Do not use	
3	12	48-60
4	4	16-24
5	1	4-6
6	6	24-36
7	Do not use	

3.4.45 Register 32h(offset = 32h) [reset = 0h]

Figure 60. Register 32h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PDNCYCLESTC							
7	6	5	4	3	2	1	0
PDNCYCLESTC							

Table 66. Register 32h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	PDNCYCLESTC	W/R	0h	PDN_CYCLE start

3.4.46 Register 33h(offset = 33h) [reset = 0h]

Figure 61. Register 33h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PDNCYCLEENDC							
7	6	5	4	3	2	1	0
PDNCYCLEENDC							

Table 67. Register 33h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	PDNCYCLEENDC	W/R	0h	PDN_CYCLE end

3.4.47 Register 34h(offset = 34h) [reset = 0h]

Figure 62. Register 34h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PROG_TG_STC							
7	6	5	4	3	2	1	0
PROG_TG_STC							

Table 68. Register 34h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	PROG_TG_STC	W	0h	Defines the start time for the programmable timing engine signal that can replace ADC_RDY

3.4.48 Register 35h(offset = 35h) [reset = 0h]

Figure 63. Register 35h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PROG_TG_ENDC							
7	6	5	4	3	2	1	0
PROG_TG_ENDC							

Table 69. Register 35h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	PROG_TG_ENDC	W	0h	Defines the end time for the programmable timing engine signal that can replace ADC_RDY

3.4.49 Register 36h(offset = 36h) [reset = 0h]

Figure 64. Register 36h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED3LEDSTC							
7	6	5	4	3	2	1	0
LED3LEDSTC							

Table 70. Register 36h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED3LEDSTC	W/R	0h	LED3 start If LED3 is not used, leave it as '0'.

3.4.50 Register 37h(offset = 37h) [reset = 0h]

Figure 65. Register 37h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
LED3LEDENDC							
7	6	5	4	3	2	1	0
LED3LEDENDC							

Table 71. Register 37h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[15:0]	LED3LEDENDC	W/R	0h	LED3 end If LED3 is not used, leave it as '0'.

3.4.51 Register 39h(offset = 39h) [reset = 0h]

Figure 66. Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	CLKDIV_PRF		

Table 71. Register 39h Field Descriptions

Bit	Field	Type	Reset	Descriptions
[2:0]	CLKDIV_PRF	W/R	0h	Clock division ratio for clock to timing engine. For details see Table 71

Table 72. Register 39h Field Descriptions

CLKDIV_CLKOUT Register Settings	Division ratio	Frequency of the Timing clock (when the ADC clock is 4 MHz)	Lowest PRF setting in Hz(1)
0	1	4	61
1	Do not use		
2	Do not use		
3	Do not use		
4	2	2	31
5	4	1	15
6	8	0.5	8
7	16	0.25	4

(1) Limit to 10 Hz

3.4.52 Register 3Ah(offset = 3Ah) [reset = 0h]

Figure 67. Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	0	POL_OFFDAC_LED2	I_OFFDAC_LED2		
15	14	13	12	11	10	9	8
I_OFFDAC_LED2	POL_OFFDAC_AMB1	I_OFFDAC_AMB1				POL_OFFDAC_LED1	I_OFFDAC_LED1
7	6	5	4	3	2	1	0
I_OFFDAC_LED1			POL_OFFDAC_AMB2/ POL_OFFDAC_LED3	I_OFFDAC_AMB2/ I_OFFDAC_LED3			

Table 73. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Descriptions
19	POL_OFFDAC_LED2	W/R	0h	Ambient DAC polarity for LED2
[18:15]	I_OFFDAC_LED2	W/R	0h	Ambient DAC setting for LED2
14	POL_OFFDAC_AMB1	W/R	0h	Ambient DAC polarity for Ambient 1
[13:10]	I_OFFDAC_AMB1	W/R	0h	Ambient DAC setting for Ambient 1
9	POL_OFFDAC_LED1	W/R	0h	Ambient DAC polarity for LED1
[8:5]	I_OFFDAC_LED1	W/R	0h	Ambient DAC setting for LED1
4	POL_OFFDAC_AMB2 /POL_OFFDAC_LED3	W/R	0h	Ambient DAC polarity for Ambient 2 (or LED3)
[3:0]	I_OFFDAC_AMB2 /I_OFFDAC_LED3	W/R	0h	Ambient DAC setting for Ambient 2 (or LED3)

Table 74. Register settings for I_OFFDAC

I_OFFDAC Register Settings	Ambient DAC current magnitude with POL_OFFDAC=0	Ambient DAC current magnitude with POL_OFFDAC=1
0	0 uA	0 uA
1	0.47 uA	-0.47 uA
2	0.93 uA	-0.93 uA
3	1.4 uA	-1.4 uA
4	1.87 uA	-1.87 uA
5	2.33 uA	-2.33 uA
6	2.8 uA	-2.8 uA
7	2.27 uA	-2.27 uA
8	3.73 uA	-3.73 uA
9	4.2 uA	-4.2 uA
10	4.67 uA	-4.67 uA
11	5.13 uA	-5.13 uA
12	5.6 uA	-5.6 uA
13	6.07 uA	-6.07 uA
14	6.53 uA	-6.53 uA
15	7 uA	-7 uA

3.4.53 Register 3Dh(offset = 3Dh) [reset = 0h]

Figure 68. Register 3Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	DEC_EN	0	DEC_FACTOR			0

Table 75. Register 3Dh Field Descriptions

Bit	Field	Type	Reset	Descriptions
23-6	0	W	0h	Must write 0
5	DEC_EN	R/W	0h	0= Decimation mode disabled 1= Decimation mode enabled
4	0	W	0h	Must write 0
3-1	DEC_FACTOR	R/W	0h	Decimation factor (how many samples Are to be averaged);see table 76 for details
0	0	W	0h	

Table 76. DEC_FACTOR Register Settings

DEC_FACTOR REGISTER SETTINGS	DECIMATION FACTOR
0	1
1	2
2	4
3	8
4	16
5-8	Do not use

3.4.54 Register 3Fh(offset = 3Fh) [reset = 0h]

Figure 69. Register 3Fh

23	22	21	20	19	18	17	16
AVG_LED2-ALED2VAL							
15	14	13	12	11	10	9	8
AVG_LED2-ALED2VAL							
7	6	5	4	3	2	1	0
AVG_LED2-ALED2VAL							

Table 76. Register 3Fh Field Descriptions

Bit	Field	Type	Reset	Descriptions
23-0	AVG_LED2-ALED2VAL	R	0h	These bits are the 24-bit averaged output code for (LED2-Ambient2) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

3.4.55 Register 40h(offset = 40h) [reset = 0h]

Figure 70. Register 40h

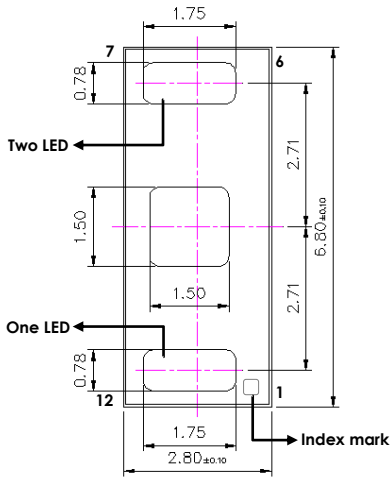
23	22	21	20	19	18	17	16
AVG_LED1-ALED1VAL							
15	14	13	12	11	10	9	8
AVG_LED1-ALED1VAL							
7	6	5	4	3	2	1	0
AVG_LED1-ALED1VAL							

Table 76. Register 40h Field Descriptions

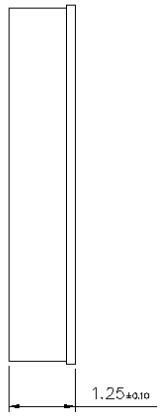
Bit	Field	Type	Reset	Descriptions
23-0	AVG_LED1-ALED1VAL	R	0h	These bits are the 24-bit averaged output code for (LED1-Ambient1) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

4. Mechanical Design

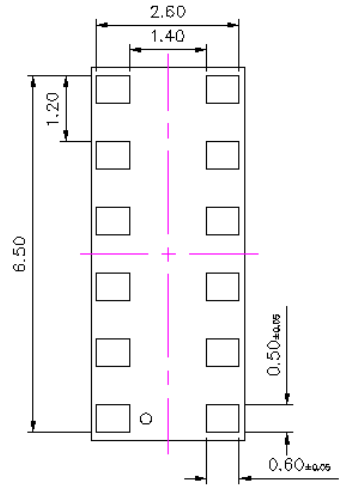
4.1 Mechanical data(unit : mm)



Top View



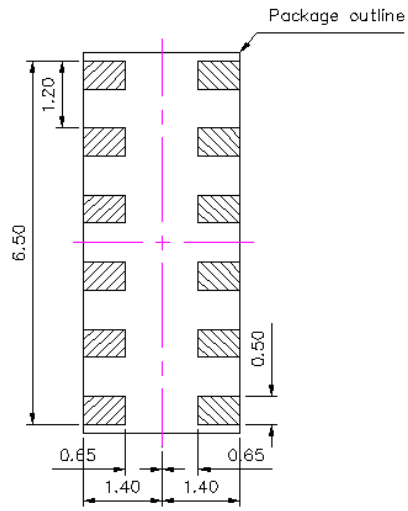
Side View



Bottom View

Pin No.	Function	Pin No.	Function
1	RX_SUP	7	TX_SUP
2	ADC_RDY	8	N.C
3	CLK	9	GND
4	RESETZ	10	N.C
5	SDA	11	N.C
6	SCL	12	IO_SUP

4.2 PCB Layout Footprint (unit : mm)



5. Application Information

5.1 Brief Application Note

Figure 68, 69 shows the typical connection of PPS964A. The following points are to be noted:

1. Use decoupling capacitors (1 uF or higher) placed close to the PPS964A to filter the noise on RX_SUP and TX_SUP.
2. The voltage level used for IO_SUP should be the same as I/O voltage level for the MCU.
3. The pull up resistors of two line serial bus are recommended to be 2.2 KΩ.

1) External clock mode

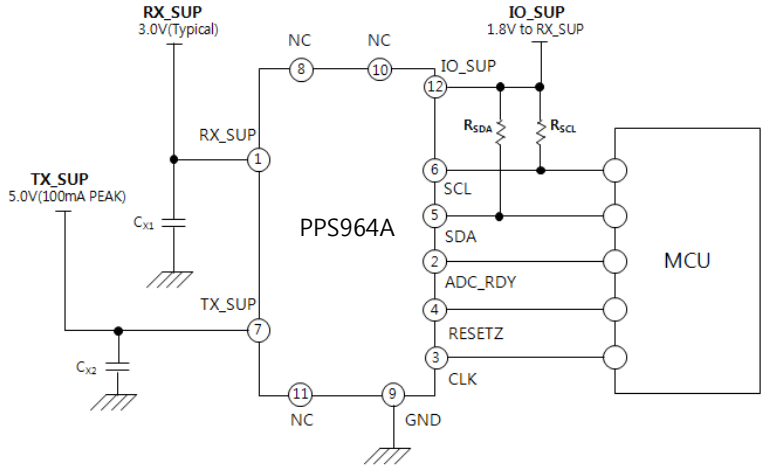


Figure 68. Hardware pin connection diagram in external clock mode

2) Internal oscillator mode

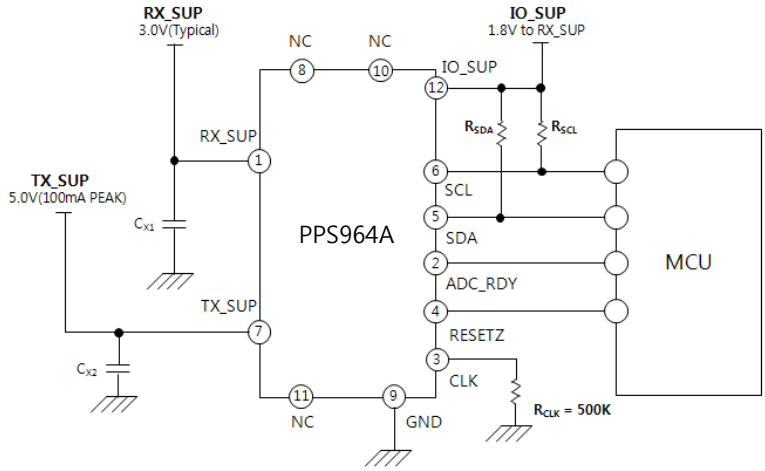


Figure 69. Hardware pin connection diagram in internal oscillator mode

6. Power Supply Recommendations

The guidelines for Power supply sequencing and Device initialization are shown in Figure 67 and Figure 68.

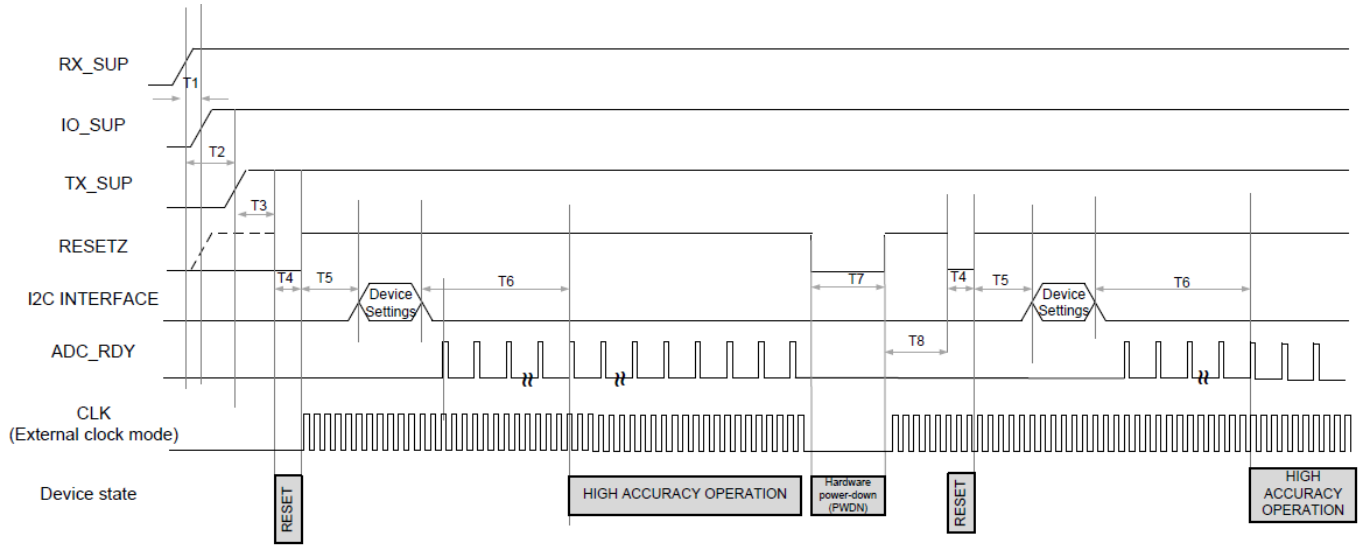


Figure 67. Power Supply Sequencing, Device Initialization, and Hardware Powerdown Timing

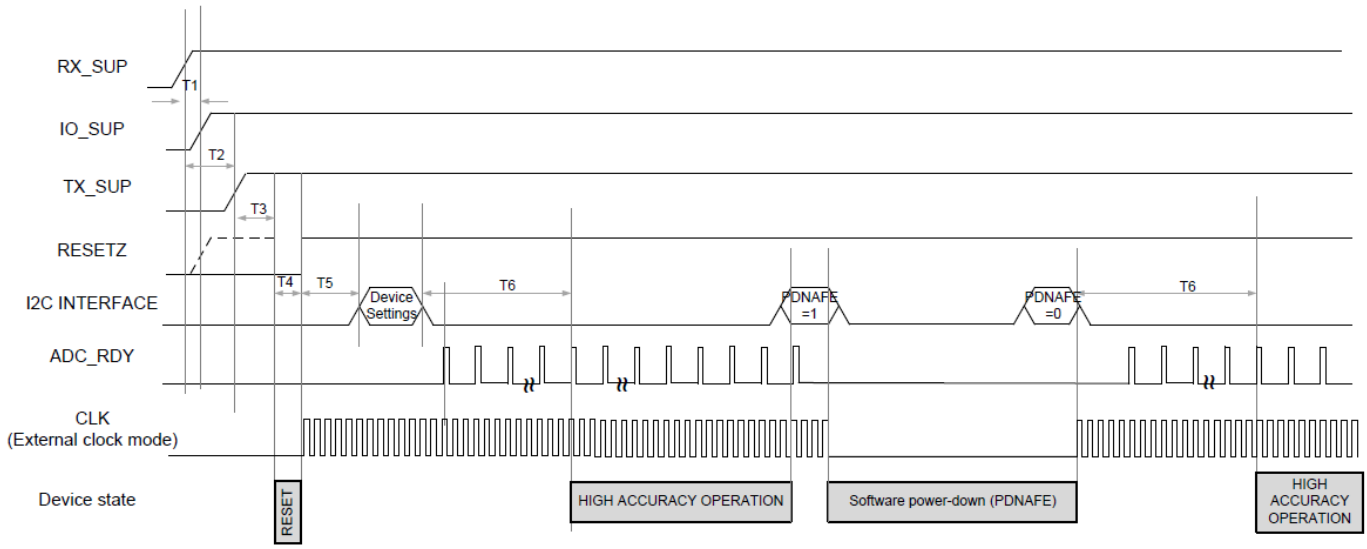


Figure 68. Power Supply Sequencing, Device Initialization, and Software Powerdown Timing

Table 74. Timing Parameter for power Supply Sequencing, Device Initialization, and Powerdown Timing

Timing	Description	Value
T1	Time between RX_SUP and IO_SUP ramping up	Ramp up RX_SUP before or at the same time as IO_SUP. Keep T1 as small as possible. Eg.10 ms
T2	Time between RX_SUP and TX_SUP ramping up	Keep as small as possible. Eg.+/-10 ms
T3	Time between all supplies stabilizing and start of RESETZ low going pulse	> 10 ms
T4	RESETZ pulse width for the device to get reset	Between 25 us and 50 us
T5	Time between resetting the device and issue of I2C commands	> 1 ms
T6	Time between I2C commands and the ADC_RDY pulse which corresponds to valid data	$T_{CHANNEL}$ (1)
T7	Width of RESETZ pulse for the device to enter into PWDN (power-down) mode	> 200 us
T8	Time from exiting power-down mode and subsequently resetting the device	> 10 ms

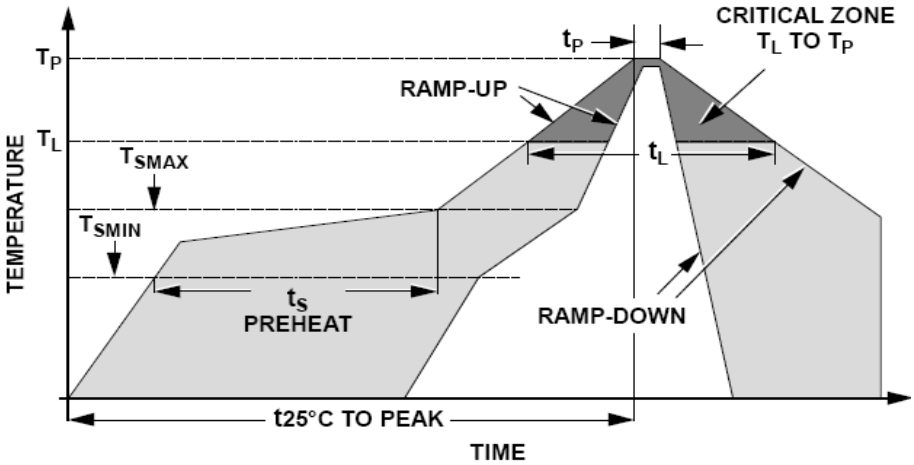
(1) Parameter $T_{CHANNEL}$ specified in electrical characteristics

7. Reflow Profile

***Standard Reflow soldering condition**

Reference	J-STD-020-C, J-STD-033		
Maximum Peak Temperature	260℃		
Moisture Sensitivity Level	MSL 3		
Bake Condition		Exposure Time > 72 hours	Exposure Time < 72 hours
	Bake @ 125℃	9 hours	7 hours
	Bake @ 90℃, < 5% RH	33 hours	23 hours
	Bake @ 40℃, < 5% RH	13 days	9 days

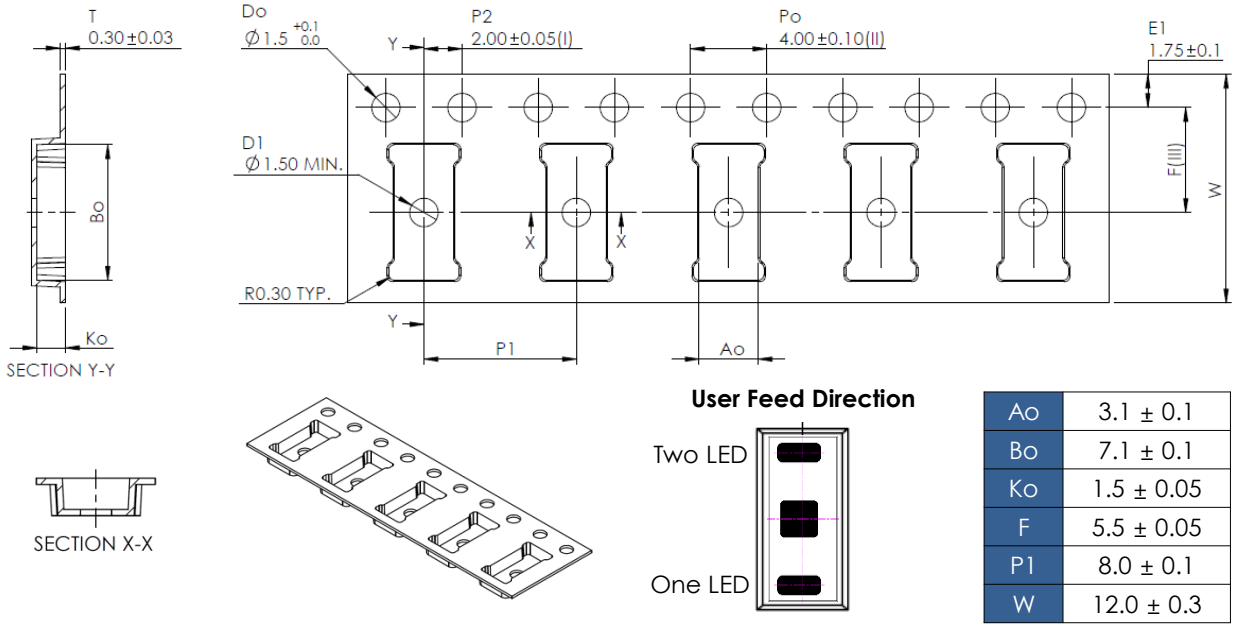
- Recommended Solder Reflow



Profile Feature	Pb-Free Assembly
Average ramp-up rate(T_{SMAX} to T_P)	3℃/second max.
Preheat - Temperature Min.(T_{SMIN}) - Temperature Max.(T_{SMAX}) - Time(T_{SMIN} to T_{SMAX}) (T_S)	150℃ 200℃ 60 ~ 180 seconds
Time maintained above : - Temperature(T_L) - Time(t_L)	217℃ 60 ~ 150 seconds
Peak temperature(T_P)	260℃
Time within 5℃ of actual peak temperature(T_P)^2	20 ~ 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

8. Package Specifications

8.1 Carrier Tape Information I[Unit : mm]

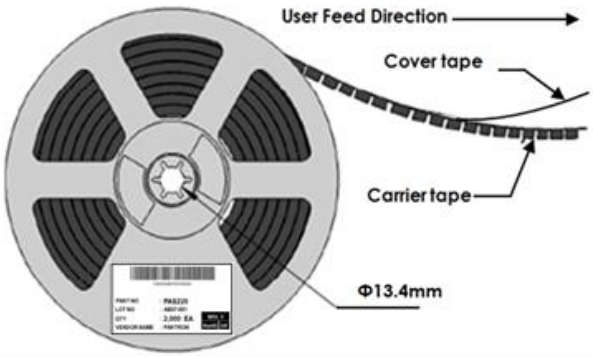


User Feed Direction

Ao	3.1 ± 0.1
Bo	7.1 ± 0.1
Ko	1.5 ± 0.05
F	5.5 ± 0.05
P1	8.0 ± 0.1
W	12.0 ± 0.3

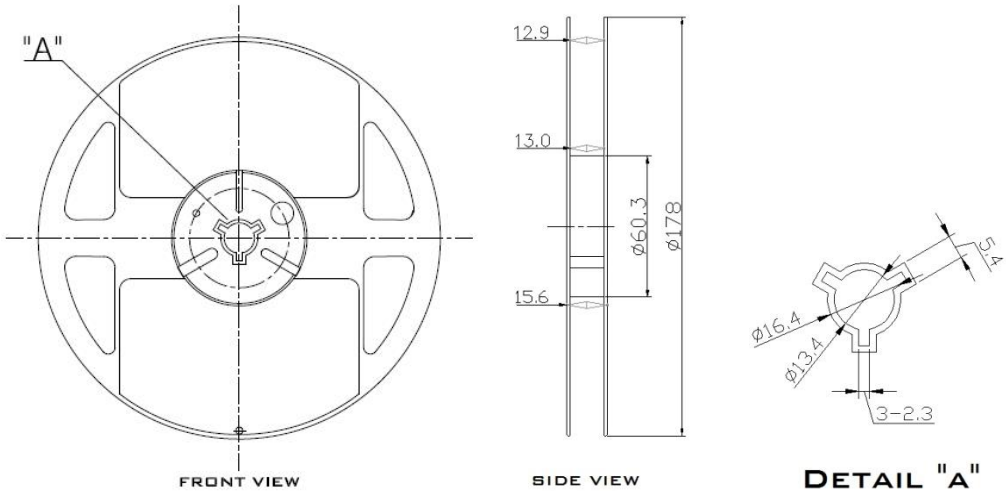
※ Note
1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ±0.20mm.
3. Measured from centerline of sprocket hole to centerline of pocket.

8.2. Carrier tape Information II(unit : mm)



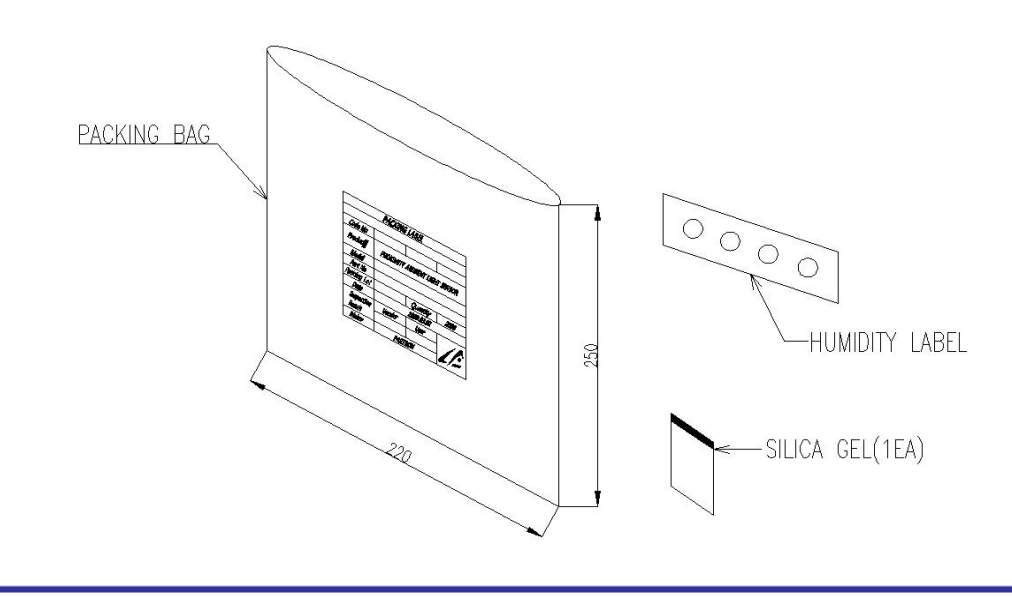
※ Note
1. Reel Diameter : 330±1 mm
2. Quantity Per Reel : 5,000EA
3. Label : external package & reel

8.3. Reel Information (unit : mm)



8.4. Aluminum Bag Information(Unit : mm)

(1) Material: Aluminum + Nylon + LDPE
(2) Quantity: 5,000ea / 1pcs
(3) Put Silica gel and humidity indicator into package and attach the Label



9. Conditions of product storage and baking

Please use this product within 6 months after receipt.

- The product shall be stored without opening the packing under the ambient temperature from 5 to 35℃(Celsius) and humidity from 20 to 70% RH.
  (Packing materials, in particular, may be deformed at the temperature over 40℃ (Celsius)).

- The product left more than 6 months after receipt, it needs to be confirmed the solderbility before used.

- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_X, etc.).

- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

  This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020).

- After the packing opened, the product shall be stored at <30℃(Celsius) / <60% RH and the product shall be used within 168 hours.

- When the color of the indicator in the packing changed, the product shall be baked before soldering.

- Baking condition : 125±5℃(Celsius), 9 hours, 1 time

- The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant

10. Reliability Specifications

No.	Test item	Test condition
1	**Preconditioning Test**	Bake + Soak(MSL3 or above) + 3X reflow [Test was performed after a lapse of two hours.]
2	**High Temperature & Humidity Resistance**	+85℃/85% R.H., 120 hours, [Test was performed after a lapse of two hours.]
3	**Temperature Cycle**	-40±2℃(30 min.) → +85℃±2℃(30 min.), 300 cycles [Test was performed after a lapse of two hours.]
4	**Low Temperature Resistance**	-20℃, 1000 hours [Test was performed after a lapse of two hours.]
5	**High Temperature Resistance**	+125℃, 1000 hours [Test was performed after a lapse of two hours.]
6	**High Temperature Operating Life**	125℃ / Max V_{CC} / Dynamic, 1000 hours
7	**Low Temperature Operating Life**	-20℃ / Max V_{CC} / Dynamic, 1000 hours
8	**Unbiased HAST**	130℃ / 85% / 33.3psi, 96 hours [Test was performed after a lapse of two hours.]
9	**Temperature Humidity with Bias(THB)**	85℃,85% RH / Max V_{DD} / 1000 hours
10	**ESD**	HBM : 2kV, MM : 200V CDM : 1kV, Latch up : ±100mA/3.6V
11	**Vibration**	Frequency: 0 ~ 500Hz, Amplitude : 1.52 mm(duration of 1 minute) 2 hours, 3 axis (X, Y, Z direction) [Test was performed after a lapse of two hours.]
12	**Drop**	1.5 m, Steel plate, 12 times
13	**Reflow**	3 reflow cycles [Test was performed after a lapse of two hours.]
14	**Solder heat**	+350℃, 5 sec., each pad(4-point) respectively
15	**EMI**	1kV/m, 60Hz