Data sheet

Rev. 0.3

PPSI262

Integrated Module for Heart rate monitors and pulse oximeters

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Specification Revisions

- Revision history.

Rev	Date	Revision history
0.1	2017.02.22	Initial Release
0.2	2017.08.30	Changed photodiode characteristics
0.3	2018.01.31	Removed RED LED Characteristics

PPSI262

Integrated Module for Heart rate monitors and pulse oximeters

1. Overview

1.1 Brief Description

The PPSI262 is an integrated module for optical bio-sensing applications, such as heart-rate monitoring (HRM) and saturation of peripheral capillary oxygen (SpO2). The device supports up to four switching light-emitting diodes (LEDs) and up to three photodiodes. The current from the photodiode is converted into voltage by the transimpedance amplifier (TIA) and digitized using an analog-to-digital converter (ADC). The ADC code can be stored in a 128-sample First in, First out (FIFO) block with programmable depth. The FIFO depth can be partitioned to accommodate the phases that must be stored. The FIFO can be read out using either an I2C or a SPI interface. The PPSI262 also has a fully-integrated LED driver with an 8-bit current control. The device has a high dynamic range transmit-and-receive circuitry that helps with the sensing of very small signal levels.

Features

- Flexible Pulse Sequencing and Timing Control
- Clocking using an external clock or internal oscillator
- FIFO with 128-sample Depth:
  – Programmable Partitioning Across Phases
- I2C, SPI™ Interfaces: Selectable by Pin

Transmitter :

- Supports Common Anode LED Configuration
- 8-Bit Programmable LED Current up to 200 mA
- Mode to fire two LEDs in parallel
- Programmable LED On-Time
- Simultaneous Support of 3 LEDs for Optimized SpO2, HRM, or Multi-Wavelength HRM

Receiver:

- Supports 3 Time-Multiplexed Photodiode Inputs
- 24-Bit Representation of the Current Input from the Photodiode in Twos Complement Format
- Individual DC Offset Subtraction DAC (Up to ±126-µA Range) at TIA Input for Each LED, Ambient
- Digital Ambient Subtraction at ADC Output
- Noise filtering with programmable bandwidth
- Transimpedance Gain: 10 kΩ to 2 MΩ

Physical Characteristics

- Operating Temperature Range: –30°C to +85°C
- Supply voltage:
  Rx : 1.8~1.9V(LDO bypass)
  2.0~3.6V(LDO Enable)
  Tx : 3~5.25V
  IO : 1.7~3.6V
- Small size package : 7.0 x 3.0 x 1.35mm, 20-LGA
- Dual green/IR LED PKG

1.2. Block Diagram

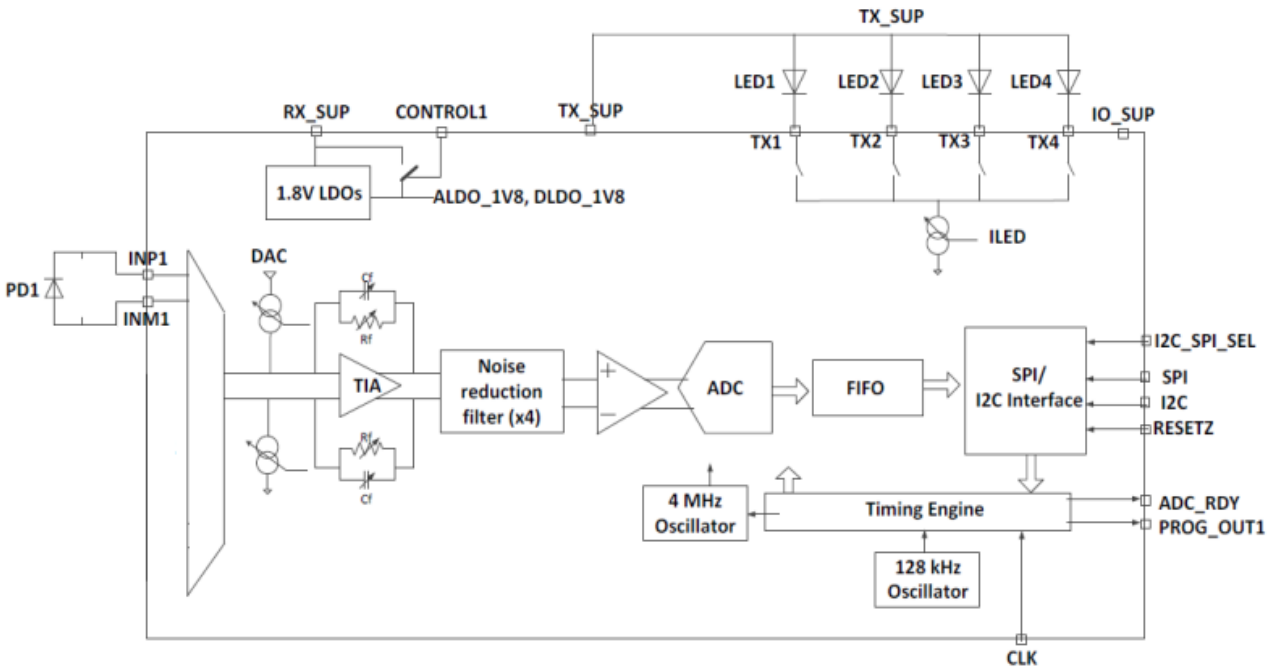


Figure 1. Block Diagram.

1.3 Applications

- Optical Heart-Rate Monitoring (HRM) for Wearables, Hearables
- Heart-Rate Variability (HRV)
- Pulse Oximetry (SpO2) Measurements
- Maximum Oxygen Consumption (VO2 Max)
- Calorie Expenditure

1.4 Pin Configurations

• 20 -LGA (PPSI262)

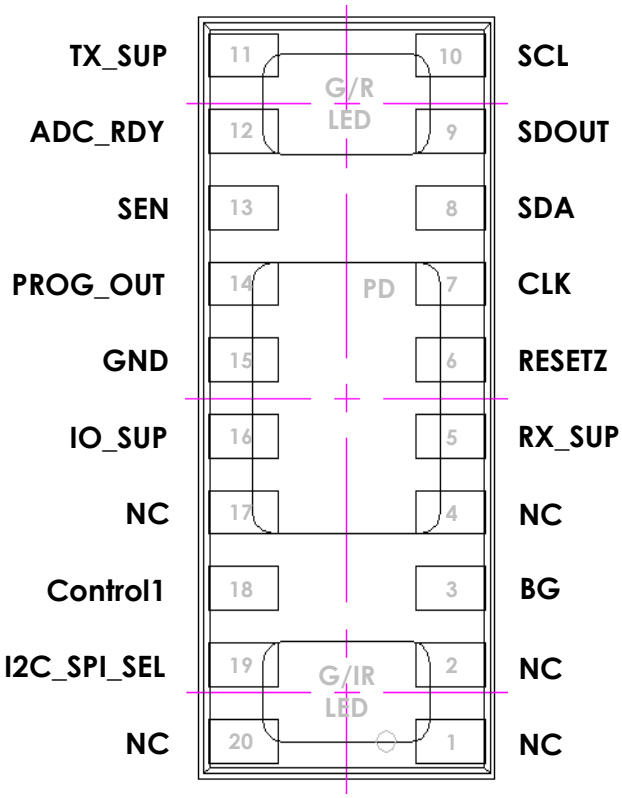


Figure 2. PKG Diagram.

(Top View)

1.5 Pin Description

Table 1. Pin Description.

PIN No.	PIN Name	Description
1	NC	Not connected
2	NC	Not connected
3	BG	Bandgap voltage output; 0.1uF decoupling capacitor can be used.(1)
4	NC	Not connected
5	RX_SUP	Receiver supply; 1-µF decapacitor to GND. 1.8 V to 1.9 V (when LDO is bypassed with CONTROL1='1') 2.0 V to 3.6 V (when LDO is enabled with CONTROL1='0')
6	RESETZ	This pin is either RESETZ or PWDN. Functionality is based on the (active low) duration of RESETZ. A 25-µs to 50-µs duration means that RESETZ is active and the device is reset. A > 200-µs duration means that PWDN is active. Levels = 0 V to IO_SUP. Do not leave floating. While enabling PWDN, pull CONTROL1 and I2C_SPI_SEL also to '0'
7	CLK	Clock Input pin. Levels = 0 V to IO_SUP. The lowest frequency clock with which the device could be made to work is 32 kHz. Using a higher clock frequency enables finer timing control resolution for the timing signals (eg. SAMP, LED ON, etc) in the Active phase.
8	SDA	I^2C mode : I^2C data, external resistor to IO_SUP (Eg. 10kΩ). SPI mode : Serial data input Levels = 0V to IO_SUP.
9	SDOUT	I^2C mode : Programmable interrupt (output). SPI mode : Serial data output for SPI Levels = 0V to IO_SUP.
10	SCL	I^2C mode : I^2C data, external resistor to IO_SUP (Eg. 10kΩ). SPI mode : Serial clock input Levels = 0V to IO_SUP.
11	TX_SUP	Transmitter supply; 1uF decapacitor to GND
12	ADC_RDY	Programmable interrupt (output)
13	SEN	I^2C mode: Invert of LSB of I^2C slave address; SPI mode: Chip select for SPI (Active low).
14	PROG_OUT	Programmable interrupt (output).(2) Levels = 0 V to IO_SUP. Connect to MCU input pin.
15	GND	Common ground
16	IO_SUP	Provides a separate supply for the digital I/O. From 1.7 to a max value equal to RX_SUP
17	NC	Not connected
18	Control1	When RX_SUP is 2.0V or higher: Connect CONTROL1 to ground (0V) to operate with internal LDOs enabled. When RX_SUP is 1.8-1.9V: Connect CONTROL1 to an MCU I/O pin. Pull to '1' during normal operation (with LDO bypassed) and to '0' during Hardware power-down mode.
19	I2C_SPI_SEL	This pin enables selection between the I^2C and SPI interfaces. 0: To enable I^2C interface and to save power in Hardware Powerdown mode 1: To enable SPI interface Connect to an output pin of the MCU for dynamic control. I^2C_SPI_SEL is internally referred to RX_SUP. If RX_SUP and IO_SUP differ by more than 0.3V, a level shifter will be needed for the connection.
20	NC	Not connected (FVDD)

(1) Using a 0.1-µF capacitor on BG improves the AFE noise but results in a higher recovery time from a software and hardware power- down.
(2) To enable the PROG_OUT1 pin as an output pin, set the EN_PROG_OUT1 bit to '1'.

2. IC Characteristics

2.1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter	Conditions	Min.	Max.	Units
Supply voltage range	RX_SUP to GND : LDO bypassed	-0.3	2.1	V
	RX_SUP to GND : LDO enabled(2)	-0.3	4	V
	IO_SUP to GND	-0.3	Min[4, (RX_SUP+0.3)]	V
	TX_SUP to GND	-0.3	6	V
Voltage applied to Analog inputs		Max[-0.3, (RX_GND-0.3)]	Min[4, (RX_SUP+0.3)]	V
Voltage applied to Digital inputs		Max[-0.3, (RX_GND-0.3)]	Min[4, (IO_SUP+0.3)]	V
Max duty cycle(Cumulative): Sum of all LED phase durations as a fraction of total period	50mA LED current mode		10	%
	100mA LED current mode		3	%
	200-mA LED current mode		TBD	%
Storage temperature, T_{stg}		-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages higher than 2.1V can be applied on RX_SUP only when CONTROL1 pin is at '0'.

2.2. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter			Min.	Typ	Max.	Units
RX_SUP	Receiver supply : LDO bypass mode		1.8		1.9	V
	Receiver supply : LDO enabled mode		2.0		3.6	V
IO_SUP			1.7		RX_SUP	V
TX_SUP		50-mA LED current mode	[3.0 or (0.32 + V_{LED})(1) whichever is greater]		5.25	V
Digital Inputs (except CONTROL1, I2C_SPI_SEL)			0		IO_SUP	V
Analog inputs (and CONTROL1, I2C_SPI_SEL)			0		RX_SUP	V
Operating temperature range			-30		85	°C

(1) VLED refers to the maximum voltage drop across the external LED (at maximum LED current). This value is usually governed by the forward drop voltage(V_{FB}) of the LED.

2.3 Electrical characteristics

Typical specifications are at T_A = 25°C; TX_SUP = 5 V, RX_SUP = 1.8V (with CONTROL1=1.8V to bypass internal LDOs), IO_SUP = 1.8 V, external clock mode with 32 kHz clock on CLK pin (period = t_{TE} = 31.25µs),

1-kHz sampling rate, SAMP width of 3xt_{TE}, LED ON width of 4xt_{TE}, Cf chosen such that there are 7-8 TIA time constants within the SAMP width, NUMAV=1 (2 ADC averages), Noise Reduction Filter bandwidth set to 2.5 kHz, C_{IN} = 100 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD)

Parameter	Conditions	Min.	Typ.	Max.	Unit
PRF(1) – Pulse repetition frequency		25		1000	SPS
Receiver					
Offset cancellation DAC current range	Default range	-15.75		15.75	uA
	2X range	-31.5		31.5	
	4X range	-63		63	
	8X range	-126		126	
Offset cancellation DAC current step	Default (–15.75 uA to 15.75 uA) range		0.125		uA
TIA gain setting		10K		2M	Ω
C_f setting		2.5		25	pF
Switched RC filter bandwidth(2)			2.5, 5, 10		kHz
ADC averages	Set as (NUMAV+1)	1		16	
Detector capacitance	Differential capacitance between INP, INN	10		200	pF
PPG Transmitter					
LED current range	50mA mode	0		50	mA
	100mA mode	0		100	
	200mA mode	0		200	
LED current resolution			8		Bits
PPG PERFORMANCE					
Receiver-only noise	Receiver inputs open, Rf=500-kΩ, Cf=7.5 pF		40		µV(3)
Transmitter + Receiver noise	50 mA LED current looped back electrically to the receiver inputs through an external op-amp to create an output voltage of 0.4V (Rf=500kΩ, Cf=7.5 pF)		60		µV(3)

(1) PRF refers to the rate at which samples from each of the four phases are output from the AFE.
(2) Lower filter bandwidth setting gives lower effective bandwidth for both signal and noise
(3) Output noise over the full Nyquist bandwidth calculated from the standard deviation of the output code.

Electrical Characteristics (continued)

Typical specifications are at T_A = 25°C; TX_SUP = 5 V, RX_SUP = 1.8V (with CONTROL1=1.8V to bypass internal LDOs), IO_SUP = 1.8 V, external clock mode with 32 kHz clock on CLK pin (period = t_{TE} = 31.25µs), 1-kHz sampling rate, SAMP width of 3xt_{TE}, LED ON width of 4xt_{TE}, Cf chosen such that there are 7-8 TIA time constants within the SAMP width, NUMAV=1 (2 ADC averages), Noise Reduction Filter bandwidth set to 2.5 kHz, C_{IN} = 100 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD)

Parameter	Conditions	Min.	Typ.	Max.	Unit
EXTERNAL CLOCK(When external clock mode)					
Frequency of external clock		32		4000	kHz
Input clock high level			IO_SUP		V
Input clock low level			0		V
Input capacitance of CLK pin	Capacitance to ground		<4		pF
INTERNAL OSCILLATOR FOR TIMING ENGINE (When using internal oscillator mode)					
Frequency			128		kHz
Accuracy	Room temperature		±1%		
Frequency drift with temperature	Full temperature range		±1%		
Jitter(RMS)			12		ns
FIFO					
FIFO depth				128	Samples
I²C INTERFACE					
Maximum clock speed			400		kHz
I²C slave address	SEN=1		5A		Hex
	SEN=0		5B		Hex
SPI INTERFACE					
Maximum clock speed			4		MHz
Current consumption					
RX_SUP current excluding switching current from I²C or SPI readout(4)	PPG signal acquisition(5)		50		uA
	Hardware power-down (PWDN) mode(6)		<1		
	Software power-down (PDNAFE) mode(6)		15		
RX_SUP current resulting from switching current at I²C readout	At PRF of 100 Hz, readout with FIFO enabled with FIFO_PERIOD=60, FIFO_NPHASE=4(7)		12		
	Power-down mode		0		
IO_SUP current(5)	PPG signal acquisition(5)		1		uA
	Hardware power-down (PWDN) mode(6)		<1		
	Software power-down (PDNAFE) mode(6)		<1		
TX_SUP current	PPG signal acquisition(5)		4		uA
	Hardware power-down (PWDN) mode(6)(8)		<1		
	Software power-down (PDNAFE) mode(6)(8)		<1		
Digital Inputs					
V_{IH} High-level input voltage	Digital inputs except CONTROL1, I2C_SPI_SEL	0.9*IO_SUP	IO_SUP		V
	CONTROL1 and I2C_SPI_SEL(9)	0.85*RX_SUP	RX_SUP		V
V_{IL} Low-level input voltage	Digital inputs except CONTROL1, I2C_SPI_SEL		0	0.1*IO_SUP	V
	CONTROL1 and I2C_SPI_SEL(9)			0.1*RX_SUP	V
Digital Outputs					
V_{OH} High-level input voltage			IO_SUP		V
V_{OL} Low-level input voltage			0		V

(4) The additional current for FIFO readout is negligible when operating in the SPI interface mode.
(5) Acquisition of 4 phases of signal in PPG mode at 50 Hz PRF
(6) External clock switched off.
(7) This current depends on the percentage of time for which the I2C_CLK is low; and scales with FIFO_NPHASE and PRF. This extra component of current is negligible when operating in the SPI interface mode.
(8) With LED currents set to 0 mA.
(9) CONTROL1 and I2C_SPI_SEL can also be driven directly by the MCU (with IO_SUP levels) if the VIH, VIL levels are satisfied.

2.4 Timing Requirements

2.4.1 Interrupts Timing

		Min.	Typ.	Max..	Unit
$t_{DATA\_RDY\_RISE}$	DATA_RDY rise time (10% to 90%) with a 15-pF capacitive load to ground(1)		12		ns
$t_{DATA\_RDY\_FALL}$	DATA_RDY fail time (90% to 10%) with a 15-pF capacitive load to ground(1)		12		ns

(1) Same timing applies to other interrupts also

2.4.2 I²C Interface Timing

		Min.	Typ.	Max..	Unit
t_{I2C_RISE}(1)	I²C data rise time with a 10-kΩ pullup resistor with a 20-pF load from I²C data to GND		1200		ns
t_{I2C_FALL}	I²C data fall time (when the data line is pulled down by the AFE) with a 20-pF load from I²C data to GND		28		ns

(1) Maximum achievable speed of the I²C interface could be limited by this parameter if the load on the I²C lines are high.

2.4.3 SPI Interface Timing

	PARAMETER	Min.	Typ.	Max..	Unit
t_{SPICLK}	Serial shift clockperiod	125			ns
t_{STECLK}	Serial data enable low to serial clock rising edge, setup time	15			ns
$t_{CLKSTEH,L}$	Serial clock transition to serial data enable high or low	15			ns
t_{SIMOSU}	Serial data input to serial clock rising edge, setup time	15			ns
t_{SIMOHD}	Valid serial data input after SCLK rising edge, hold time	15			ns
t_{SOMIPD}	Serial clock falling edge to valid serial data output			15	ns
t_{SOMIHD}	Serial clock rising edge to invalid serial data output		0.5		t_{SPICLK}

(1) The values in this table refer to the timings of these logic signals internal to the AFE. Additional timing margins may need to be accounted for based on the external delays and rise and fall times of these signals.

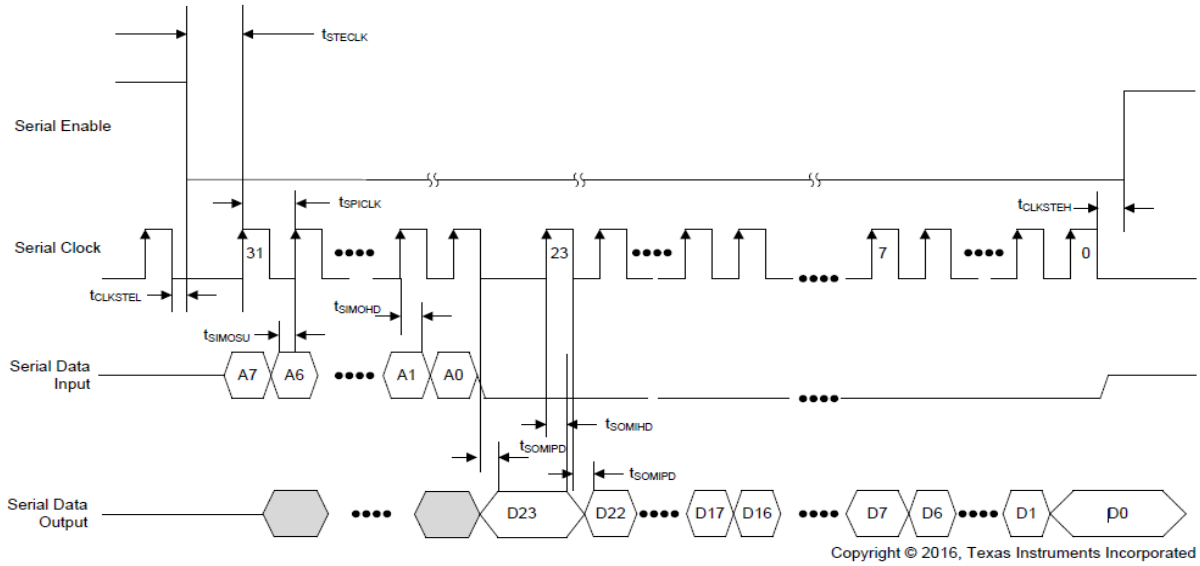


Figure 1. Serial Interface Timing Diagram, Read Operation

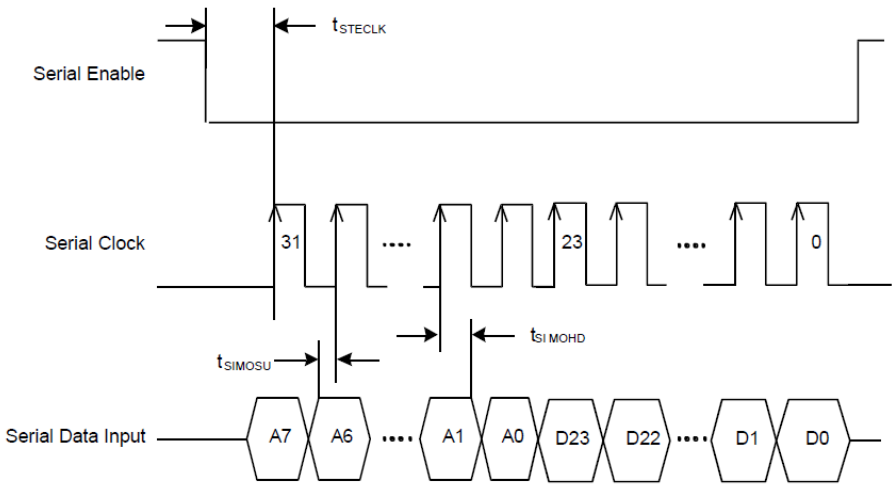


Figure 2. Serial Interface Timing Diagram, Write Operation

2.5 LED Characteristics

Table 2. Green LED(LED1) Characteristics. T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Limits			Unit	Remark
		Min	Typ	Max		
V_F	Forward Voltage	3.2	3.7	4.2	V	IF=150mA
V_R	Reverse Voltage			5	V	
P_o	Radiant Power	40		60	mW	IF=150mA
Λ_p	Peak Wavelength		527		nm	IF=150mA
Δλ	Spectrum Width, Half Power		35		nm	IF=150mA

Table 3. IR LED(LED2) Characteristics. T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Limits			Unit	Remark
		Min	Typ	Max		
V_F	Forward Voltage	1.4		1.5	V	IF=100mA
I_R	Reverse Current			5	uA	Vr=10V
P_o	Radiant Power	18		23	mW	IF=100mA
Λ_p	Peak Wavelength		945		nm	IF=100mA
Δλ	Spectrum Width, Half Power		30		nm	IF=100mA

2.6 Photo diode Characteristics

Table 4. Photo diode Characteristics. T_A=25±5℃(unless otherwise specified)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
I_D	Reverse dark current	V_R=10V, E_e=0mW/cm^2			20	nA
$V_{(BR)R}$	Reverse breakdown voltage	I_R=100uA, E_e=0mW/cm^2	33			V
C_t	Total capacitance	V_R=5V, E_e=0mW/cm^2, F=1MHZ		36		pF
t_{on}/t_{off}	Turn-on/Turn-off Time	V_R=5V, R_L=50Ω, λ=850nm		50/50		ns
S	Sensitivity	V_R=3V, 527nm		0.41		A/W
		V_R=3V, 660nm		0.5		A/W
		V_R=3V, 945nm		0.53		A/W
λ	Sensitivity wavelength range	-	300		1100	nm
λ_p	Peak sensitivity wavelength	-		850		nm

3. Detailed Description

3.1 Overview

The PPSI262 has an integrated transmitter and receiver for optical heart-rate monitoring and pulse oximetery applications. The system is characterized by a parameter termed the pulse repetition frequency (PRF) that determines the repetition periodicity of a sequence of operations. Every cycle of a PRF results in four 24-bit digital samples at the output of the AFE, each of which is stored in a separate register. An optional first in, first out (FIFO) can be used to store samples across multiple periods. The FIFO depth can be programmed to store the analog-to-digital converter (ADC) data from the different phases over a certain number of periods. When the FIFO is enabled, the ADC_RDY pin can be configured to serve as a FIFO_RDY interrupt and its periodicity changes based on the number of periods over which the programmed FIFO depth is filled.

The receiver input pins (INP, INM) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a trans-impedance amplifier (TIA). The TIA gain is set by its feedback resistor (RF) and can be programmed from 10 kΩ to 2 MΩ. The trans-impedance gain between the input current and output differential voltage of the TIA is equal to 2 × RF. At the output of the TIA is a programmable switched RC filter which serves as a Noise Bandwidth reduction filter. There are four parallel RC filters that are each connected to the TIA output signal during one of the four sampling phases. The output of each filter at the end of the sampling phase is stored on a capacitor, buffered and converted by an ADC. The ADC output in each phase can be stored in the FIFO and read out using the SPI or I2C interface. An Offset Cancellation DAC at the input of the receiver can be programmed to subtract a DC current from the incident current signal from the Photodiode. By removing some or all of the DC current, a higher TIA gain can be applied to maximize the Signal to Noise ratio at the output of the AFE. The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on the power supplies.

The transmitter comprises of an LED current driver which can be routed to a different LED in each phase. The current setting of the LED driver can be independently programmed in each phase. The operation of the LEDs turning on can be fully synchronized with the sampling of the signal from the photodiode by the receiver. The synchronization is made possible using a fully programmable timing engine.

The PPSI262 has two internal LDOs, ALDO and DLDO which can be used for driving the Analog and Digital sections of the receiver. When CONTROL1 is connected to RX_SUP, the LDOs are powered down with their output tristate, and the internal nodes ALDO_1V8 and DLDO_1V8 are connected through switches to RX_SUP. When CONTROL1 is 0V, two Internal LDOs are enabled and they drive ALDO_1V8 and DLDO_1V8 to 1.8V. When operating in the internal LDO mode, the LDOs can be made to enter a low power state during the Deep sleep phase so as to limit the power impact.

3.2 Sequence of receiver operations

The PPSI262 has four sampling phases within the active phase of each PRF cycle. In the PPG mode, the four sampling phases can correspond to either of the following signal state sequences received by the photodiode. The recommended sequence is shown below:

1. 2-LED mode: LED2 → Ambient phase 2 → LED1 → Ambient phase 1
2. 3-LED mode: LED2 → LED3 → LED1 → Ambient

The sequence of the signals Within the active phase of the pulse repetition cycle is shown in Figure 3.

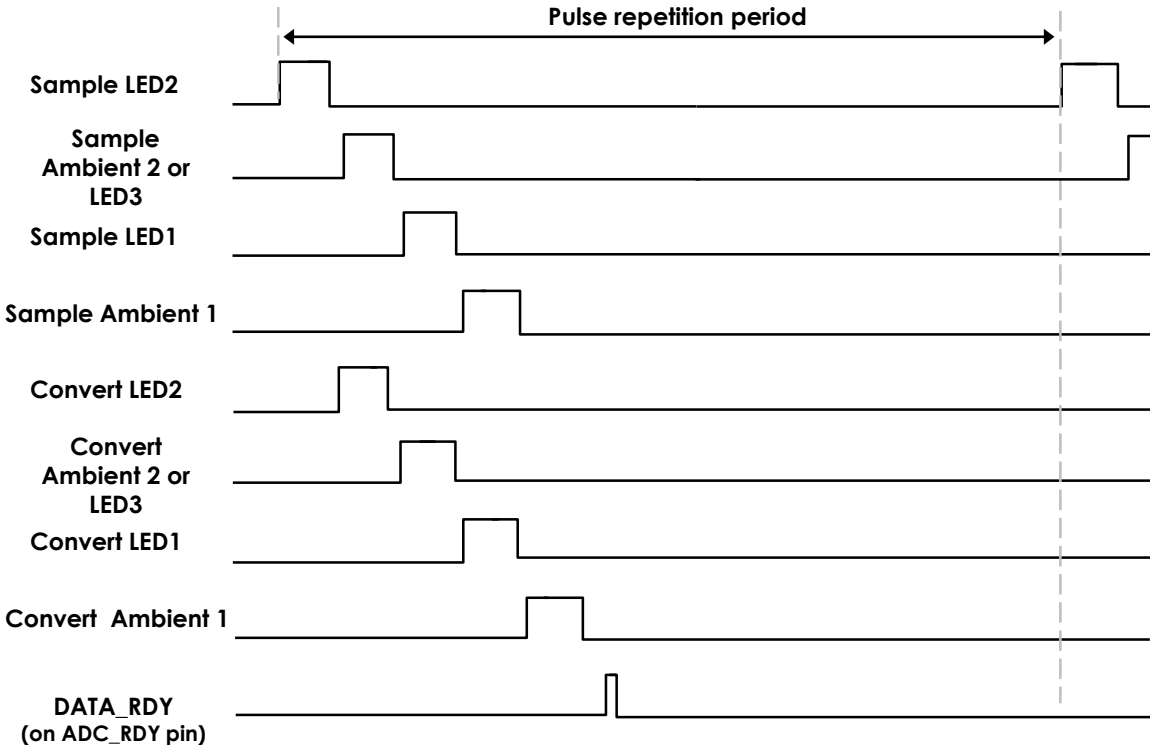


Figure 3. Sequence of Four Sampling and Conversion Phases

In 2-LED mode, LED1 and LED2 are pulsed around the corresponding sampling phases. In 3-LED mode, LED1, LED2, and LED3 are pulsed around the corresponding sampling phases. The TIA gain (RF) and feedback capacitor (CF) can be programmed differently between the four phases. If RF and CF must be independently programmed for the first and second phases, then the LED3 ON signal must be programmed even if LED3 is not used. If independent programmability of RF and CF is required for the third and fourth phases, an LED4 ON signal must be programmed. A 4th LED can be optionally connected on the TX4 pin and can be turned on in the Ambient phase 1. However, operation with all 4 LEDs turned on in the same PRF cycle is not recommended because such operation would not allow acquisition of the ambient signal (which requires the LEDs to be OFF). When LED4 is turned on, then one of the other three phases should be used as the Ambient phase. An interrupt termed *DATA_RDY* can be programmed by setting a start and end count and can be output on the ADC_RDY pin. This signal can serve as an interrupt to the MCU to read data from the AFE every PRF cycle. This interrupt is applicable when the FIFO is not used.
If any of the four conversion phases are not needed, then the phase durations can be set to 0 (by setting the phase start and end counts greater than PRPCT). The DATA_RDY interrupt can be positioned after the last conversion phase is completed. The DATA_RDY pulse is defined using the start and end counts in registers DATA_RDY_STC and DATA_RDY_ENDC.

3.3 TIA Gain and Bandwidth controls

The TIA gain is set by programming the value of R_F (the feedback resistor of the TIA). The R_F setting is controlled using the TIA_GAIN* and TIA_GAIN_SEP* register controls.

The TIA feedback capacitance is set by programming the value of C_F. The product of R_F and C_F determines the time constant of the TIA and must be set to approximately 1/5th (or less) of the sampling pulse durations. This choice of time constant allows the TIA to pass the incoming pulses from the photodiode, and for its output to settle close to the steady-state value.

By default, the TIA_GAIN and TIA_CF register controls determine the R_F and C_F applied for all four phases of the receiver. Separate values can be set for the phases by setting either the ENSEPGAIN or ENSEPGAIN4 bits, as shown in Table 6.

Phase	Default		ENSEPGAIN=1		ENSEPGAIN4=1	
	R_f	C_f	R_f	C_f	R_f	R_f
LED2	TIA_GAIN	TIA_CF	TIA_GAIN_SEP	TIA_CF_SEP	TIA_GAIN_SEP	TIA_CF_SEP
LED3/Ambient 2	TIA_GAIN	TIA_CF	TIA_GAIN_SEP	TIA_CF_SEP	TIA_GAIN_SEP2	TIA_CF_SEP2
LED1	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF
Ambient 1	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF	TIA_GAIN_SEP3	TIA_CF_SEP3

Table 6. Mapping of register controls to the R_f and C_f controls in the various phases

When ENSEPGAIN4 = 1, the transition points of the four R_F and C_F settings are defined by the start of the corresponding LED phase, as shown in Figure 4. Thus, program the LED3 start and end counts even if LED3 is not used and program the LED4 start and end counts even though LED4 does not physically exist.

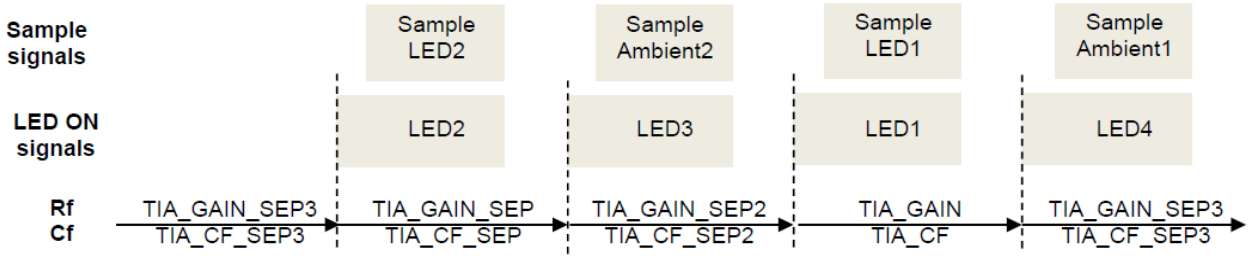


Figure 4. TIA R_F, C_F transitions within a period for ENSEPGAIN4=1

The TIA gain controls are 4-bit controls using the register bits shown in Table 7. The settings for RF and CF are shown in Table 8 and Table 9, respectively

4-bit control	D3	D2	D1	D0
TIA_GAIN	TIA_GAIN_MSB	TIA_GAIN_LSB		
TIA_GAIN_SEP	TIA_GAIN_SEP_MSB	TIA_GAIN_SEP_LSB		
TIA_GAIN_SEP2	TIA_GAIN_SEP2_MSB	TIA_GAIN_SEP3_LSB		
TIA_GAIN_SEP3	TIA_GAIN_SEP3_MSB	TIA_GAIN_SEP3_LSB		

Table 7. Mapping of register controls to the 4-bit TIA gain control

The TIA setting for R_f are shown in Table 8.

TIA_GAIN, TIA_GAIN_SEP* REGISTER CONTROL	R_f
0	500kΩ
1	250kΩ
2	100kΩ
3	50kΩ
4	25kΩ
5	10kΩ
6	1MΩ
7	2MΩ
8	1.5MΩ
Other settings	Do not use

Table 8. TIA_GAIN Register Settings

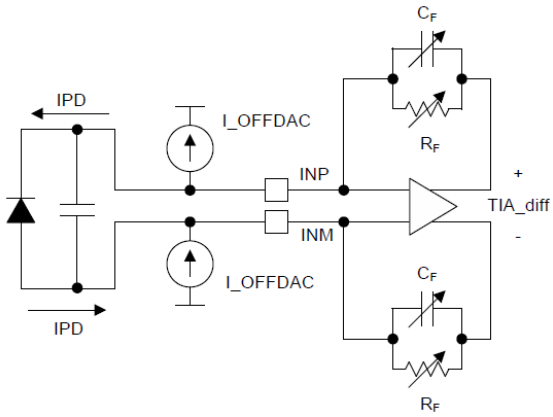
The TIA settings for C_f are shown in Table 9.

TIA_CF, TIA_CF_SEP* REGISTER VALUE	C_f
0	5 pF
1	2.5 pF
2	10pF
3	7.5 pF
4	20pF
5	17.5pF
6	25pF
7	22.5pF

Table 9. TIA_CF Register Settings

3.4 Offset cancellation DAC

A typical optical heart-rate signal has a dc component and an ac component. Although a higher TIA gain maximizes the ac signal at the PPSI262 output, the magnitude of the dc component limits the maximum gain possible in the TIA. In order to decouple the affect of the dc level on the allowed ac signal gain, a current digital-to-analog converter (DAC) is placed at the input of the device. By setting a programmable cancellation current (based on the dc current signal level), the effective signal that is gained up by the TIA can be reduced.
This reduction in the effective signal current into the TIA results in the ability to set a higher TIA gain than what is otherwise possible without enabling the offset correction. In each of the four phases of operation, a separate programmable current value can be set by programming four different sets of register bits. These cancellation currents are automatically presented to the input of the TIA in the appropriate phase. The ability to set a different cancellation current in each of the four phases can be used to cancel out the ambient current in the ambient phase. In the LED on phase, this ability can be used to cancel out the sum of the ambient current and dc current of the heart-rate signal. The polarities of the signal current and offset cancellation current is illustrated in Figure 5. The polarity of the offset cancellation current can be reversed by programming the POL_OFFDAC bits.



With zero input current and zero current in the offset cancellation DAC, the output of the PPSI262 will be close To zero. Based on the channel offset, the output voltage for zero input current could be a small positive or negative value, usually in the range of several mV. With the photodiode connected as shown in Figure 6 and a signal current coming from the photodiode, the output code of the device is expected to be positive with the offset cancellation DAC set to zero (I_{offset} = 0). With I_{offset} set negative (POL_OFFFAC = 1), a dc offset can be subtracted from the signal and the ac signal can be amplified with a higher gain than what is otherwise possible.

Figure 5. Offset Cancellation Current Polarity Diagram

A breakdown of the signal current and voltage levels is provided in Table 10 for a variety of signal levels. In Table 10, the current transfer ratio (CTR) is used to describe the relationship between the set LED current and the resulting photodiode current (IPD). CTR is the ratio of the photodiode current for a given LED current and is a function of the optical and mechanical parameters as well as human physiology.

PHASE	ILED(mA)	CTR (uA/mA)	I_{sig} (uA)	I_{amb} (uA)	IPD (uA)	I_OFFDAC (uA)	I_{eff} (uA)	R_F (MΩ)	TIA_diff (V)
LED2	25	0.025	0.625	1	1.625	-1.5	0.125	1	0.25
LED3	50	0.025	1.25	1	2.25	-2	0.25	0.5	0.25
LED1	12.5	0.025	0.3125	1	1.3125	-1	0.3125	0.5	0.3125
AMB1	0	0.025	0	1	1	-1	0	2	0

Table 10. Signal Current and Voltage Levels for a Hypothetical Use Case(1)

(1) ILED is the set LED current; CTR is the current transfer ratio (in =A / mA); I_{sig} is the photodiode signal current resulting from LED pulsing (I_{sig} = ILED × CTR); I_{amb} is the current in the photodiode resulting from ambient light (that is present in all phases and adds to I_{sig}); IPD is the total input current (I_{sig} + I_{amb}); I_OFFDAC is the current setting of the offset cancellation DAC; I_{eff} is the effective current after offset cancellation (I_{sig} + I_OFFDAC); R_f is the TIA gain setting; and TIA_diff is the output differential signal of the TIA (note that this signal must be within the range of ±1 V).

The I_OFFDAC* bits control the magnitude of the current subtracted (or added) at the TIA input. The POL_OFFDAC bits determine whether the current is subtracted from or added to the input. The mapping of the register controls to the 6-bit control for I_OFFDAC is shown in Table 11. By default, the full-scale current range of the Offset Cancellation DAC is ±15.75 uA. This range can be extended by using the IFS_OFFDAC register control as shown in Table 12. The offset DAC value as a function of the I_OFFDAC* and IFS_OFFDAC is shown in Table 13.

7-bit control	D6	D5	D4	D3	D2	D1	D0
I_OFFDAC_LED1	I_OFFDAC_LED1_MSB	I_OFFDAC_LED1_MID				I_OFFDAC_LED1_LSB	I_OFFDAC_LED1_LSB_EXT
I_OFFDAC_LED2	I_OFFDAC_LED2_MSB	I_OFFDAC_LED2_MID				I_OFFDAC_LED2_LSB	I_OFFDAC_LED2_LSB_EXT
I_OFFDAC_LED3	I_OFFDAC_LED3_MSB	I_OFFDAC_LED3_MID				I_OFFDAC_LED3_LSB	I_OFFDAC_LED3_LSB_EXT
I_OFFDAC_AMB1	I_OFFDAC_AMB1_MSB	I_OFFDAC_AMB1_MID				I_OFFDAC_AMB1_LSB	I_OFFDAC_AMB1_LSB_EXT

Table 11. Mapping of register controls to the 6-bit control of I_OFFDAC*

IFS_OFFDAC value (binary)	Full scale current
000	±15.75 uA
011	±31.5 uA
101	±63 uA
111	±126 uA
Other setting	Do not use

Table 12. Full-scale current control of the Offset Cancellation DAC using IFS_OFFDAC control

DECIMAL EQUIVALENT OF 7-BIT I_OFFDAC*	OFFSET CANCELLATION DAC CURRENT (µA) for different IFS_OFFDAC (binary setting)			
	IFS_OFFDAC='000'	IFS_OFFDAC='011'	IFS_OFFDAC='101'	IFS_OFFDAC='111'
0	0	0	0	0
1	0.125	0.25	0.5	1
2	0.25	0.5	1	2
..	..	..	..	..
127	15.75	31.5	63	126

Table 13. Mapping of the offset DAC setting to the 6-bit I_OFFDAC* control[1], [2]

(1) The offset cancellation DAC is not trimmed at production and, therefore, the value of the full-scale current can vary across units by ±20%.

(2) Above table corresponds to POL_OFFDAC*=0. With POL_OFFDAC*=1, the above currents become negative

With respect to Table 13, the following points should be noted. The I_OFFDAC_LED*_LSB_EXT bit extends the resolution of the Offset DAC control. However, the relative accuracy of the current control from this bit is worse than the accuracy of the other bits. Additionally, the absolute accuracy of the Offset DAC current setting becomes worse at higher settings of IFS_OFFDAC. The noise contribution from the Offset DAC also increases for higher current settings. As a result, using the higher Offset Cancellation currents could result in diminishing returns on the SNR.

By default, the Offset Cancellation DAC transitions as shown in Figure 6. The Offset DAC transitions to the value set for a given phase at the start of SAMP phase and returns to the value set for the Ambient1 phase (I_OFFDAC_AMB1) between SAMP phases.

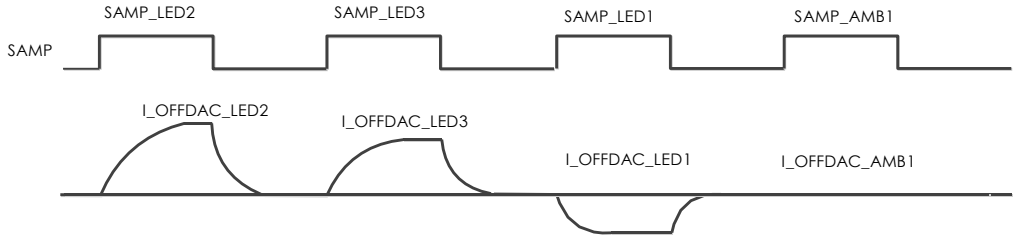


Figure 6. Transitions of the offset DAC at the SAMP phases

By programming the register control EARLY_OFFSET_DAC, the transition of the Offset DAC can be advanced to happen at the start of the LED ON signal as shown in Figure 7. Refer section Sampling width considerations for more details.

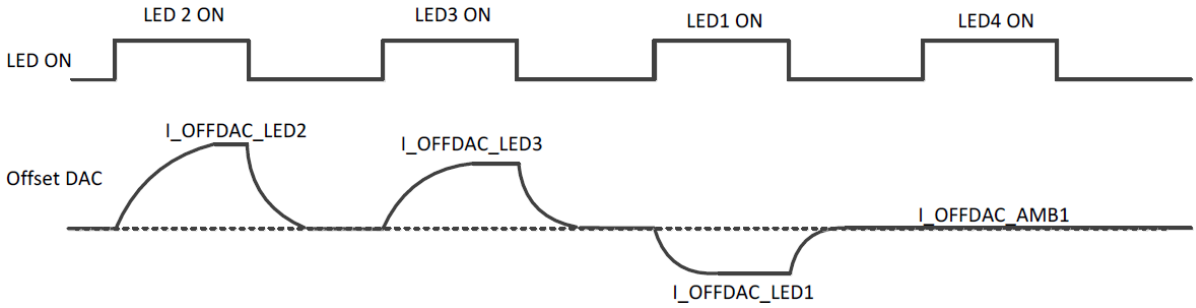


Figure 7. Transitions of the offset DAC when EARLY_OFFSET_DAC is set to '1'

3.5 Noise reduction filter

The PPSI262 has a programmable noise bandwidth filter which is connected to the output of the TIA during the SAMP phase. There are 4 filters, one dedicated for each phase. Each filter is meant to 'see' the settled voltage of the TIA output corresponding to that phase, which corresponds to the steady-state envelope of the signal for that phase. For simplicity, the scheme with the four parallel filters is shown in Figure 8 for a single-ended representation of the signal chain. The effective bandwidth for both the signal as well as the noise is determined by the RC time constant of the switched RC filter and the sampling pulse duty cycle. The RC time constant of the filter is programmable. The filter provides noise bandwidth reduction. However, it also limits the effective signal bandwidth at low sampling duty cycles to a value roughly equal to (Sampling duty cycle)*f_{RC} kHz where f_{RC} is the physical 3-dB bandwidth of the filter as determined by its R-C product.

An ADCRST signal is generated automatically by the AFE at the start of the CONV phases, and is used to reset the input capacitance of the ADC buffer prior to each ADC conversion phase. This resetting of the input capacitance of the buffer helps erase the memory from previous conversions.

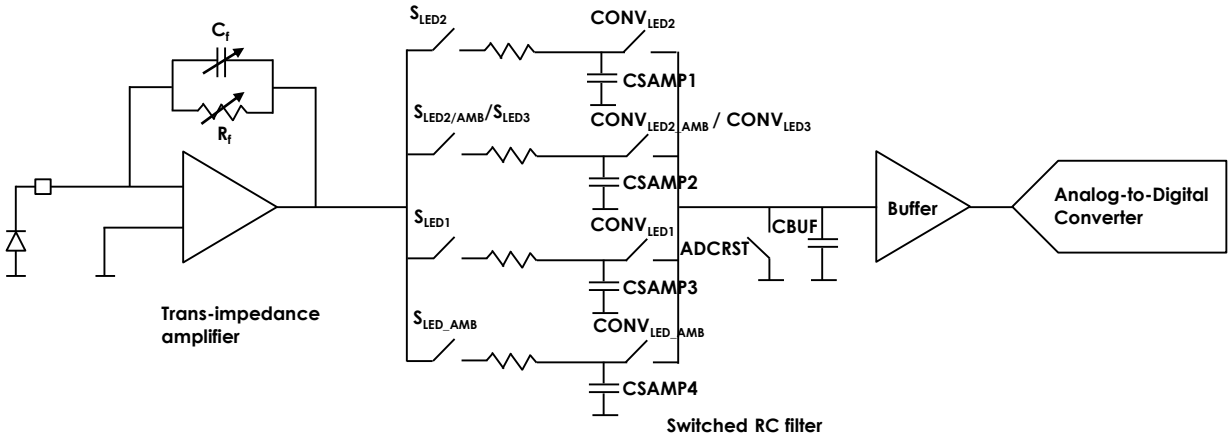


Figure 8. Illustration of the noise reduction filter

The filter bandwidth has a default typical value of 2.5 kHz. The bandwidth for the 4 filters can also be programmed between a typical value of 2.5 kHz (default), 5 kHz or 10 kHz using the FILTER_BW(1) and FILTER_BW(0) register controls as shown in Table 14.

FILTER_BW<1>	FILTER_BW<0>	Typical f_{RC} (kHz)
0	0	2.5
0	1	5
1	0	10
1	1	Do not use

Table 14. Filter bandwidth set by FILTER_BW<1:0> control

3.6 Analog-to-Digital Converter (ADC)

The PPSI262 has an ADC that provides a 22-bit representation of the current from the photodiode. The ADC codes corresponding to the various sampling phases can be read out from 24-bit registers in twos complement format. The ADC full-scale input range (±FS) is nominally ±1.2 V and spans bits 21 to 0. The mapping of the ADC input voltage to the ADC code is shown in Table 15.

Differential Input Voltage at ADC Input	24-bit ADC Output Code
-FS	111000000000000000000000
$(-FS/2^{21})V$	111111111111111111111111
0	000000000000000000000000
$(+FS/2^{21})V$	000000000000000000000001
+FS	000111111111111111111111

Table 15. Mapping of ADC Input Voltage to ADC code

When the input exceeds the full scale levels, the output code saturates. The exact saturation value depends on the NUMAV setting. For different NUMAV settings, the saturation value on the positive side is between 1FFF19h and 1FFFFFh, and the saturation value on the negative side is between E080E7h and E00000h. This kind of saturation behavior is applicable to the register data corresponding to and individual conversion phase (for eg. data in the LED2 phase register). The behavior of the (LED-Ambient) register data is different from the one outlined above. For the (LED-Ambient) register data, the two MSBs of the 24-bit word serve as sign-extension bits to the 22-bit ADC code. and are equal to the MSB of the 22-bit ADC code when the input to the ADC is within its full-scale range, as shown in Table 16.

Bits 23-21	INPUT STATUS
000	Positive and Lower than positive full scale (Within full scale range)
111	Negative and Higher than negative full scale (Within full scale range)
001	Positive and Higher than positive full scale (Outside full scale range)
110	Negative and Lower than negative full scale (Outside full scale range)

Table 16. Sign-Extension Bits in the (LED-Ambient) register data

Noted that the TIA has an operating range of ±1 V even though the ADC input full-scale range is ±1.2 V, as shown in Figure 9. When setting the TIA gain, ensure that the signal at the TIA output does not exceed ±1 V.

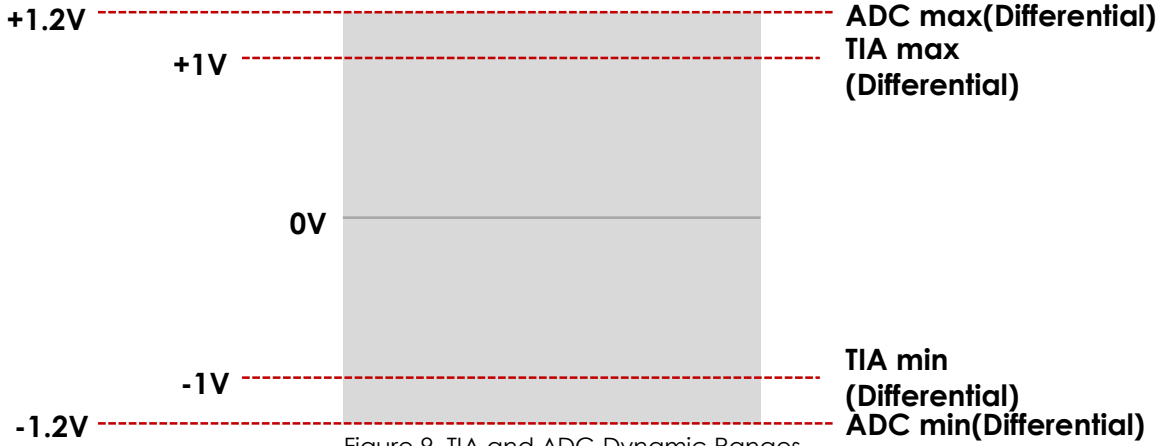


Figure 9. TIA and ADC Dynamic Ranges

To reduce the noise, the input to the ADC (sampled on the CSAMPx capacitors) can be converted by the ADC multiple times and averaged. The number of averages is set using the NUMAV register control as:
Number of Averages = (NUMAV + 1)
By default, NUMAV = 0. Therefore, the default mode corresponds to when the ADC converts its input one time in each of the four phases and stores the content in the register corresponding to that phase.

When NUMAV is programmed (for example, if NUMAV = 3), the ADC converts its input four times in each phase, averages the four conversions, and stores the averaged value in the register corresponding to that phase.

Averaging only helps in reducing ADC noise and not the front-end noise because the input to the ADC is the same sampled voltage across all ADC conversions used to generate the average (this voltage corresponds to the voltage sampled on the CSAMPx capacitors). The number of samples that can be averaged ranges from 1 to 16 (when NUMAV is programmed from 0 to 15). A higher number of averages results in larger conversion times.

Averaging is implemented in the following manner:
The number of ADC samples corresponding to the number of averages (NUMAV + 1) are accumulated, as shown below.

$$\text{SUMADC} = \sum_{i=1}^{(NUMAV+1)} (ADCi)$$

where

- ADCi = the i^{th} sample converted by the ADC.

The accumulator output (SUMADC) is then divided by a factor *D* that is obtained by D = 128 ÷ X , with X being an integer.

The averaged output is calculated as:
ADCOUT = SUMADC ÷ D

Where

- D = 128 ÷ X, with X being an integer.

This implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from ideal values for other settings, as shown in Table 17.

NUMAV	Number of averages	X	Division factor, D
0	1	128	1.0
1	2	64	2.0
2	3	43	2.97
3	4	32	4.0
4	5	26	4.92
5	6	21	6.10
6	7	18	7.11
7	8	16	8.0
8	9	14	9.14
9	10	13	9.85
10	11	12	10.67
11	12	11	11.64
12	13	10	12.8
13	14	9	14.22
14	15	9	14.22
15	16	8	16.0

Table 17. Averaging Mode Settings

3.7 LED current driver

The PPSI262 generates the drive current for the LEDs using an internally generated reference voltage called TX_REF. A voltage-to-current conversion circuit is used to convert the TX_REF voltage to the programmed LED current. Switches, controlled by the LED_ON signals are used to route the LED driver current into the appropriate TX pin as shown in Figure 10. The PPSI262 has two identical LED drivers. By default, only LED driver 1 is active.

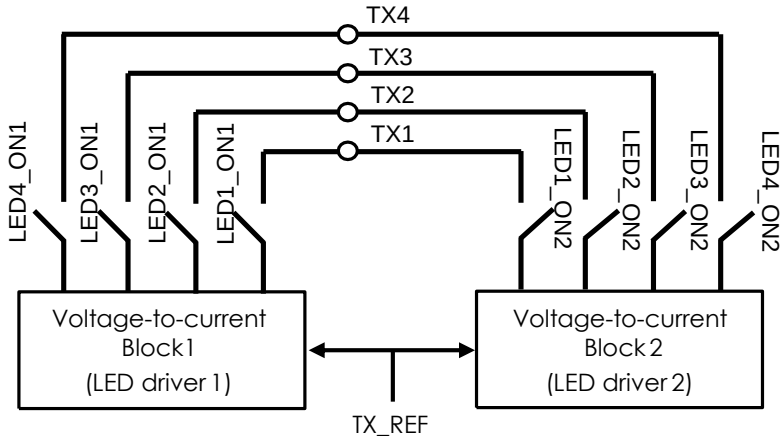


Figure 10. Support of parallel LED drive

The default LED current range is from 0 mA to 50 mA. The individual currents of each of the three LEDs can be controlled independently, each with a separate 8-bit control.
The 8-bit LED control is split into two sets of register controls as shown in Table 18.

8-bit control	D7	D6	D5	D4	D3	D2	D1	D0
ILED1	ILED1_MSB						ILED1_LSB	
ILED2	ILED2_MSB						ILED2_LSB	
ILED3	ILED3_MSB						ILED3_LSB	
ILED4	ILED4_MSB						ILED4_LSB	

Table 18. Mapping of register controls to the 8-bit LED current control

Taken as a decimal number, the 8-bit setting provides 255 steps between 0 mA and 50 mA. Each increment of the ILED 8-bit code causes the LED current setting to increment by approximately 0.2 mA. The LED current range can be programmed using the ILED_FS register control. This register control changes the full-scale LED driver current by changing the voltage on TX_REF as shown in Table 19.

ILED_FS register control	Full-scale LED driver current	TX_REF voltage
0	50 mA	0.15V
1	100 mA	0.3V

Table 19. Registers for Full-scale LED current control

The mapping of the register control to the LED current in the 50/100/200mA current modes is shown in Table 20.

ILED1, ILED2, ILED3, ILED4 REGISTER VALUES (Decimal Equivalent of 8-Bit Code)	NOMINAL LED CURRENT SETTING (mA)		
	50 mA mode	100 mA mode	200 mA mode
0	0	0	0
1	0.196	0.392	0.784
2	0.392	0.784	1.568
...	...	…	…
255	50	100	200

Table 20. LED Current Setting versus ILED Values as Set by the Registers

The control signals for the switches connected to each driver are derived from the LED*_ON signals generated by the Timing engine as defined by the start and end counts. The control signals connected to each driver can be masked in a programmable manner. By default, only LED driver 1 is active and the control signals for the switches connected to LED driver 1 (LED*_ON1) are set using the LED_ON signals. The control signals for LED driver 1 and LED driver 2 can be modified using the register controls DIS_DRV1_LEDx and EN_DRV2_LEDx respectively as shown in Table 21.

Register control (1)	Mapping of LED driver control (1) signal to LED_ON signal
DIS_DRV1_LEDx	LEDx_ON1 = LEDx_ON. DIS_DRV1_LEDx
EN_DRV2_LEDx	LEDx_ON2 = LEDx_ON. EN_DRV2_LEDx

Table 21. Register for controlling the control signals of LED driver 1 and LED driver2

(1) x refers to LED number(LED1, LED2, LED3, LED4)

The DIS_DRV1_LEDx and EN_DRV2_LEDx controls can be used to turn on two LEDs simultaneously. For example, to turn on LED1 and LED2 simultaneously, the following settings can be used:

- Program LED1_ON and LED2_ON to be identical (coincident) signals
- Program the LED current settings ILED1 and ILED2 to be the same value
- Route current of only LED driver 1 into TX1 during LED1_ON by setting DIS_DRV1_LED1='0', EN_DRV2_LED1='0'
- Route current of only LED driver 2 into TX2 during LED2_ON by setting DIS_DRV1_LED2='1', EN_DRV2_LED2='1'

The DIS_DRV1_LEDx and EN_DRV2_LEDx controls can also be used to route the current from both the LED drivers into the same LED.
The full-scale LED current and headroom voltages are listed for various use cases in Table 22.

ILED_FS register control	1 LED driver ON		2 LED drivers ON, both through 1 LED		2 LED drivers ON, 2 LEDs	
	Full scale current(1)	VHR(2)	Full scale current(1)	VHR(2)	Full scale current(1)	VHR(2)
0	50 mA	320 mV	100 mA	370 mV	50 mA	345 mV
1	100 mA	600 mV	200 mA	650 mV	100 mA	625 mV

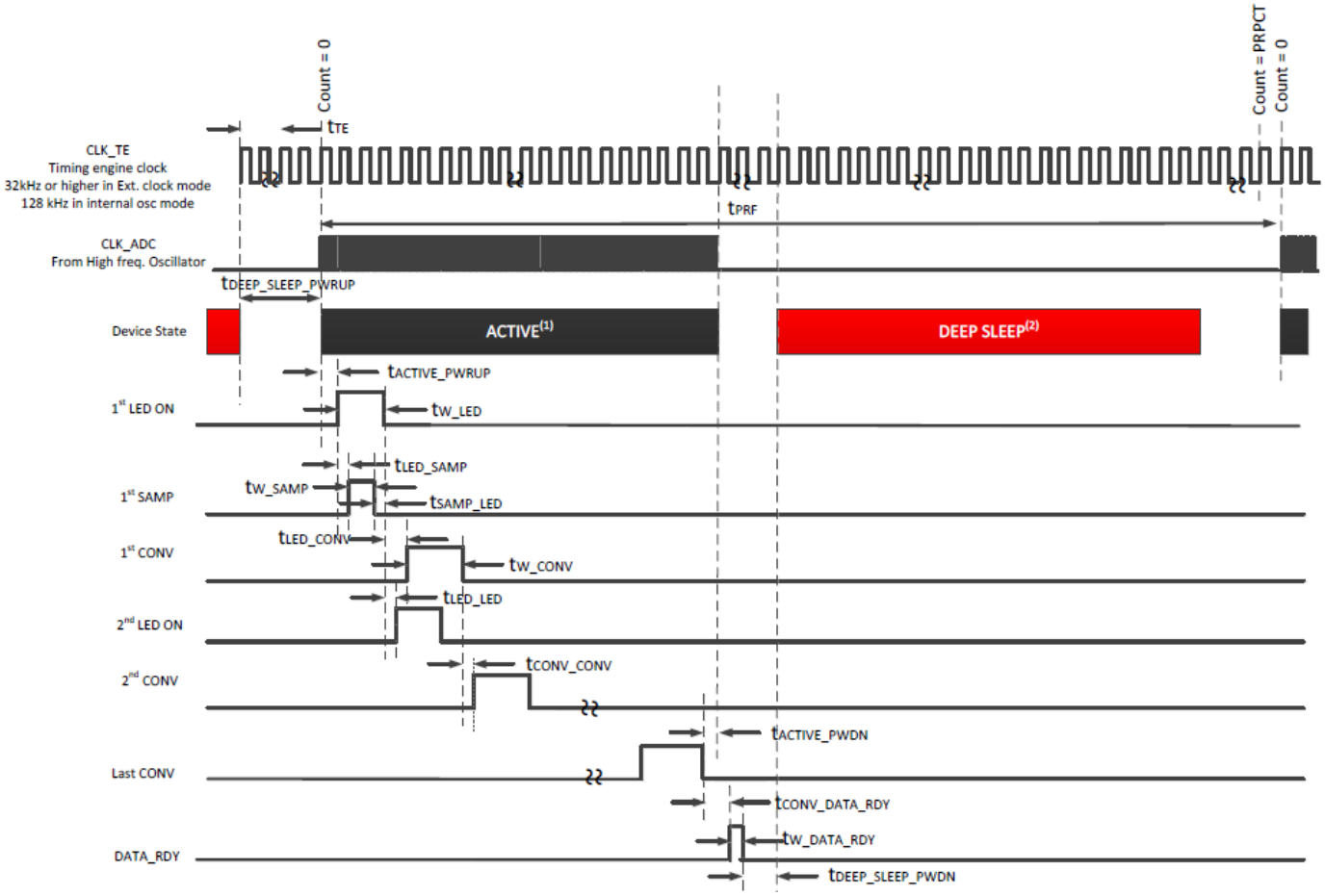
Table 22. Full-scale LED current and headroom voltage

(1) Full scale current per LED
(2) Typical voltage headroom needed for the LED driver

The parameter VHR mentioned in Table 22 refers to the typical voltage headroom needed for the LED driver when operating at a LED code corresponding to the full scale current for the ILED_FS setting. If the battery is directly used to drive TX_SUP, then the VHR can be interpreted as the voltage which when added to the forward voltage of the battery signifies the lowest voltage to which the battery can discharge before the LED driver current starts to fall.
If using a boost converter to drive TX_SUP, the boost converter's output voltage can be chosen as the sum of VHR and the maximum forward voltage of the LED, with an additional ~300 mV added for extra margin.

3.8 Timing Engine

The PPSI262 has an internal programmable timing engine that generates a repetitive pattern of signals at a rate referred to as the PRF (pulse repetition frequency). The timing engine can be configured to either run off an external clock provided on the CLK pin, or using an internally generated clock from a 128 kHz oscillator. The PRF is determined by the PRPCT register control. The high-frequency oscillator needed by the ADC for conversion can be turned on during the Active phase. The usage of the various clocking signals can be visualized from Figure 11.



(1) Set CONTROL_DYN_TIA=1, CONTROL_DYN_ADC=1 to power up the TIA and ADC in the ACTIVE phase. Set timing counts for DYN_CLK, DYN_TIA and DYN_ADC to coincide with the ACTIVE phase.

(2) Set CONTROL_DYN_BIAS=1, CONTROL_DYN_TX(1)=1, CONTROL_DYN_TX(0)=1, CONTROL_DYN_BG=1, CONTROL_DYN_VCM=1, to power down the TX, Bandgap references, and VCM buffer in the Deep sleep phase. **In LDO Enable mode**: Additionally set CONTROL_DYN_ALDO=1, CONTROL_DYN_DLDO=1 and SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP=1.

Figure 11. Timing scheme governing a PRF cycle in external clock mode

The PPSI262 has two main regions of operation, Active phase and the Deep Sleep phase. Both the Active and Deep Sleep phase can be programmed by setting start and end counts using timing registers. In the Deep sleep phase, the entire PPSI262 is put in an extremely low power state. In the Active phase, all the blocks in the Transmitter and Receiver are active. The Active phase contains all the LED ON, Sampling and CONV signals.

Figure 12 shows the clocking scheme. The device can be operated either using an external clock (in the External clock mode) or using the internal 128 kHz oscillator (in the Internal oscillator mode set by OSC_ENABLE='1').
The internal oscillator has poor frequency accuracy and for this reason, the external clock mode is preferred.
The frequency of the external clock determines the timing resolution of the timing counts. Using a clock frequency of 32 kHz results in a timing resolution of 31.25us. It is not recommended to operate at a lower clock frequency than this frequency as the timing resolution would worsen.
The timing engine generates the timing signals for the Active phase (LED ON, SAMP, CONV) as well as the dynamic controls to power down the various blocks when in Deep Sleep phase. Figure 12 shows the clocking scheme as well as the clock domains

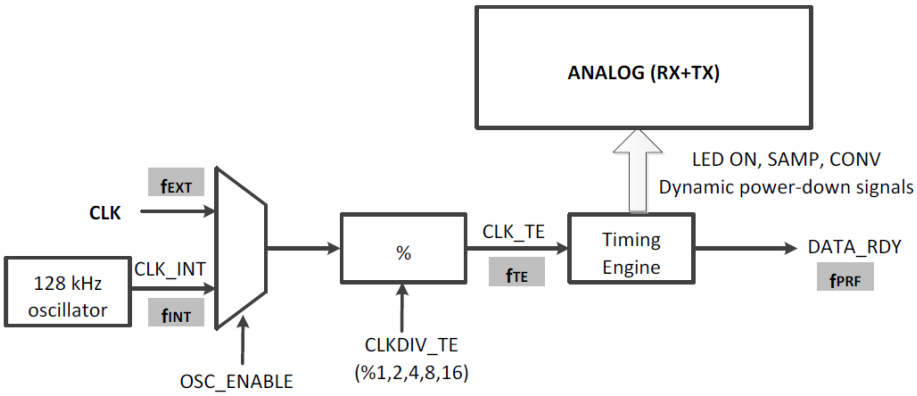


Figure 12. Clocking scheme

A listing of the clock domains is shown in Table 23.

Signal	Frequency	Comment
CLK	32 kHz (f_{EXT})	External Clock input for use in External clock mode (recommended mode of operation). The frequency indicated corresponds to a commonly available system clock. A higher clock frequency can also be provided in case a finer timing resolution is required.
CLK_INT	128 kHz (f_{INT})	Output clock of the 128 kHz oscillator for use in internal oscillator mode (low accuracy, not recommended).
CLK_TE	32 kHz (f_{TE})	All timing signal counts have a step size of 31.25 us (when in external clock mode with CLK frequency of 32 kHz and CLKDIV_TE is set to the default of Divide by 1)
DATA_RDY	50 Hz (f_{PRF})	Interrupt signal when the PRPCOUNT is set to a decimal value corresponding to 640 counts.

Table 23 . Clock domains

The clock input to the timing engine can be divided using the CLKDIV_TE register setting as shown in Table 24. Dividing the clock to the timing engine results in a lower timing resolution for the timing counts.

CLKDIV_TE REGISTER VALUE	DIVISION RATIO
0	1
4	2
5	4
6	8
7	16
Other settings	Do not use

Table 24 . Division of the clock to the timing engine

Table 25 lists the specifications for the timing parameters shown in Figure 11. All these times correspond to the physical timing instants. To map the physical time instants to the counts programmed in the timing registers, refer Table 26.

Parameter	Description	Min	Typ	Max	Unit
$f_{EXT}(1/t_{EXT})$	Frequency of the external clock on the CLK pin	32		4000	kHz
$f_{PRF}(1/t_{PRF})$	Pulse repetition frequency as set by PRPCOUNT register	25		1000	Hz
$t_{DEEP\_SLEEP\_PWRUP}$	Falling edge of CLK pin to the start of Active phase (as determined by DYN_TIA_STC, DYN_ADC_STC, DYN_CLK_STC)	200(1)			us
t_{ACTIVE_PWRUP}	Start of Active phase to the start of the first LED ON signal	300(1)			us
t_{W_LED}	Width of LED ON	55	$3xt_{TE}$(2),(3)		us
t_{LED_SAMP}	LED ON start to SAMP start	25	$1xt_{TE}$(3),(4)		us
t_{W_SAMP}	Width of SAMP phase	30	$2xt_{TE}$(3)		us
t_{SAMP_LED}	SAMP end to LED ON end	0			us
t_{LED_LED}	LED ON end to next LED ON start	$1xt_{TE}$(5)			us
t_{LED_CONV}	LED ON end to corresponding CONV phase start	$1xt_{TE}$			us
t_{W_CONV}	Width of CONV phase – External clock mode	52.3xNUMAV+67(6)			us
	Width of CONV phase – Internal oscillator mode	56.5xNUMAV+72(7)			us
t_{CONV_CONV}	End of CONV phase to start of next CONV phase	$1xt_{TE}$			us
t_{ACTIVE_PWDN}	End of last CONV to end of Active phase (determined by DYN_TIA_ENDC, DYN_ADC_ENDC, DYN_CLK_ENDC)	15	$2xt_{TE}$		us
$t_{CONV\_DATA\_RDY}$	End of last CONV to start of ATA_RDY pulse	$6xt_{TE}$			us
$t_{W\_DATA\_RDY}$	Width of DATA_RDY pulse	$1xt_{TE}$			us
$t_{DEEP\_SLEEP\_PWDN}$	DATA_RDY fall to start of Deep Sleep phase (determined by DEEP_SLEEP_STC)	$5xt_{TE}$			us

Table 25 . Timing parameters associated with the PRF cycle

(1) If the PRF setting is high, then there may not be sufficient time to put the device in Deep sleep and recover in time for the next Active phase. In that case, the Deep sleep phase should be defined to have zero duration – this can be done by setting the start and end counts to a value greater than PRPCT. The Active phase needs to be defined to span the full PRF cycle. In this case, the parameters t_{ACTIVE_PWRUP} and t_{ACTIVE_PWDN} are not applicable and can be considered as having a value of 0.

(2) Throughout this table, t_{TE} refers to one clock period of the 32 kHz clock.

(3) Refer Section titled Sampling width considerations.

(4) Refer Section titled Reducing Sensitivity to Ambient Light Modulation

(5) Assuming that TIA does not saturate in any of the phases. If the TIA saturates in a LED ON phase, then a longer separation might be required to allow the TIA output to settle before entering the next LED ON phase.

(6) To convert to Timing Counts, divide by t_{TE} and round off to the next highest integer. Eg. If NUMAV=1 (2 ADC averages), then t_{W_CONV} = 119.3 us. With external clock of 32 kHz, this would correspond to $4xt_{TE}$. To achieve this Conversion width, the register setting would need to have the relation *CONVEND=*CONVST+3.

(7) While using 128 kHz internal clock, use t_{TE} = 7.8125 us. Eg. If NUMAV=1 (2 ADC averages), then t_{W_CONV} = 128.5 us. This would correspond to $17xt_{TE}$. To achieve this Conversion width, the register setting would need to have the relation *CONVEND=*CONVST+16.

The timing diagram associated with the various programmable phase is shown in Figure 13.

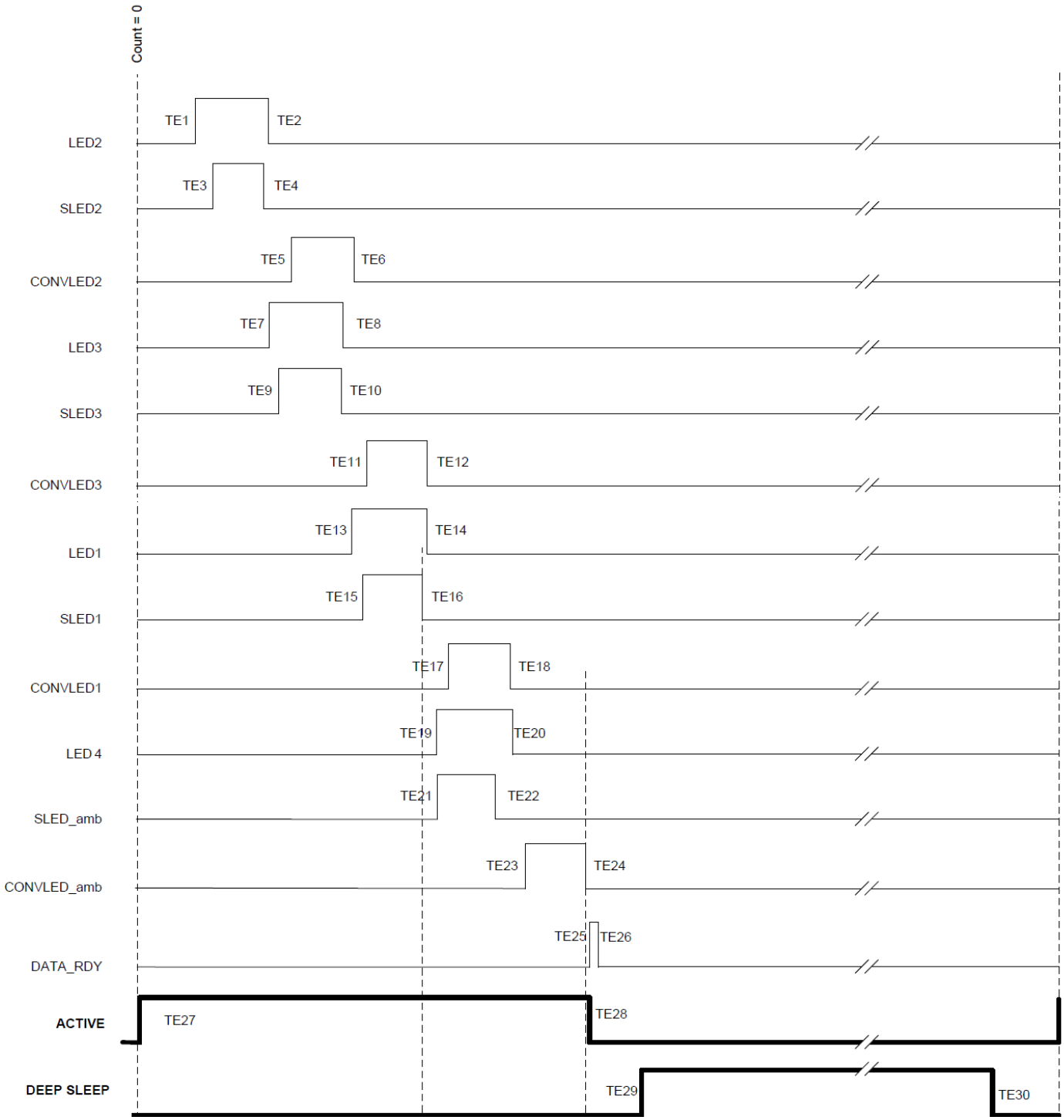


Figure 13. Timing Diagram of various programmable signal phases

The register controls for the signals generated by the timing engine are shown in Table 26.

Timing Signal	Description	REG. ADDR. (Hex)	Timing edge	Relation of time instant of actual event to register vale in decimal(REGVAL)
LED2STC	Sample LED2 start	1h	TE3	REGVAL*t_{TE}
LED2ENDC	Sample LED2 end	2h	TE4	(REGVAL+1)*t_{TE}
LED1LEDSTC	LED1 start	3h	TE13	REGVAL*t_{TE}
LED1LEDENDC	LED1 end	4h	TE14	(REGVAL+1)*t_{TE}
LED3STC	Sample Ambient2 (or sample LED3) start	5h	TE9	REGVAL*t_{TE}
LED3ENDC	Sample Ambient2 (or sample LED3) end	6h	TE10	(REGVAL+1)*t_{TE}
LED1STC	Sample LED1 start	7h	TE15	REGVAL*t_{TE}
LED1ENDC	Sample LED1 end	8h	TE16	(REGVAL+1)*t_{TE}
LED2LEDSTC	LED2 start	9h	TE1	REGVAL*t_{TE}
LED2LEDENDC	LED2 end	Ah	TE2	(REGVAL+1)*t_{TE}
ALED1STC	Sample Ambient1 start	Bh	TE21	REGVAL*t_{TE}
ALED1ENDC	Sample Ambient1 end	Ch	TE22	(REGVAL+1)*t_{TE}
LED2CONVST	LED2 convert phase start	Dh	TE5	REGVAL*t_{TE}
LED2CONVEND	LED2 convert phase end	Eh	TE6	(REGVAL+1)*t_{TE}
LED3CONVST	Ambient2 (or LED3) convert phase start	Fh	TE11	REGVAL*t_{TE}
LED3CONVEND	Ambient2 (or LED3) convert phase end	10h	TE12	(REGVAL+1)*t_{TE}
LED1CONVST	LED1 convert phase start	11h	TE17	REGVAL*t_{TE}
LED1CONVEND	LED1 convert phase end	12h	TE18	(REGVAL+1)*t_{TE}
ALED1CONVST	Ambient1 convert phase start	13h	TE23	REGVAL*t_{TE}
ALED1CONVEND	Ambient1 convert phase end	14h	TE24	(REGVAL+1)*t_{TE}
DATA_RDY_STC	DATA_RDY start	52h	TE25	(REGVAL+*N*)*t_{TE}[1]
DATA_RDY_ENDC	DATA_RDY end	53h	TE26	(REGVAL+*N*+1)*t_{TE}[1]
LED3LEDSTC	LED3 start	36h	TE7	REGVAL*t_{TE}
LED3LEDENDC	LED3 end	37h	TE8	(REGVAL+1)*t_{TE}
LED4LEDSTC	LED4 start[1]	43h	TE19	REGVAL*t_{TE}
LED4LEDENDC	LED4 end[1]	44h	TE20	(REGVAL+1)*t_{TE}
ACTIVE_STC	Active phase start	64h, 66h, 68h[2] [3]	TE27	REGVAL*t_{TE}
ACTIVE_ENDC	Active phase end	65h, 67h, 69h[2]	TE28	(REGVAL+1)*t_{TE}
DEEP_SLEEP_STC	Deep sleep start	6Ah	TE29	REGVAL*t_{TE}
DEEP_SLEEP_ENDC	Deep sleep end	6Bh	TE30	(REGVAL+1)*t_{TE}

Table 26 . Timing register and edge details

[1] Refer Table 37 for the value of N for various interrupts
[2] Write the 3 registers to the same value.
[3] Set these 3 counts to zero so that the Active phase starts at a count of 0.

The cases requiring LED3 and LED4 signals are summarized in table 27.

USAGE CASE	SIGNALS REQUIRED TO BE DEFINED	ADDITIONAL REQUIREMENT
LED3 is used	LED3 ON	ILED3 must be set to the desired value
Separate R_F and C_F must be programmed in the LED2 and Ambient2 phases	LED3 ON	ENSEPGAIN4 =1
Separate R_F and C_F must be programmed in the LED1 and Ambient1 phases	LED3 ON	ENSEPGAIN4 =1
Independent Offset DAC setting in the four phases with the Offset DAC set to transition at LED ON start	LED3 ON, LED4 ON	EARLY_OFFSET_DAC=1

Table 27. Cases requiring the LED3 ON and LED4 signals to be programmed

3.8.1 Differences in the power cycling scheme between the LDO Enabled mode and LDO Bypass mode

When operating with the LDOs bypassed (CONTROL1='1'), the Analog and Digital portions of the receiver are directly driven by the external RX_SUP. When operating with the LDO enabled (CONTROL1=0), the internal LDOs (ALDO and DLDO) are enabled when the DEEP SLEEP signal is low. The following register controls can be used to reduce the power impact from the LDOs while continuing to ensure that the device maintains its programmed operating state when it comes out of the Deep sleep phase and enters the next Active phase.

CONTROL_DYN_ALDO: Powers down the Analog LDO in Deep Sleep phase
CONTROL_DYN_DLDO: Puts the Digital LDO to a low power state in Deep Sleep phase
SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP: Shorts ALDO_1V8 to DLDO_1V8 so that both the LDO outputs are commonly driven by the Digital LDO

3.9 First-In, First-Out (FIFO) Block

3.9.1 FIFO depth and partitioning

The PPSI262 has a 128 sample FIFO which can be used to store the data from the phases of interest. Each sample corresponds to a 3-byte ADC word. The FIFO is enabled by setting the FIFO_EN bit to '1'.

The FIFO can be partitioned to store data from the phases of interest. The ways to partition the FIFO are controlled using the register control FIFO_PARTITION. A register control called REG_FIFO_PERIOD sets the number of periods over which the FIFO gets filled (FIFO_PERIOD) to be (REG_FIFO_PERIOD+1). The different ways to partition the FIFO using the FIFO_PARTITION register control are shown in Table 28.

FIFO_ PARTITION	FIFO_ NPHASE	PHASE1	PHASE2	PHASE3	PHASE4	PHASE5	PHASE6
0000	4	LED2	Ambient2	LED1	Ambient1	—	—
0001	1	(LED1—Ambient1)	—	—	—	—	—
0010	2	LED1	Ambient1	—	—	—	—
0011	1	(LED2—Ambient2)	—	—	—	—	—
0100	2	LED2	Ambient2	—	—	—	—
0101	2	(LED2—Ambient2)	(LED1—Ambient1)	—	—	—	—
0110	3	(LED1—Ambient1)	(LED2—Ambient1)	(Ambient2—Ambient1)	—	—	—
0111	6	LED2	Ambient2	(LED2—Ambient2)	LED1	Ambient1	(LED1—Ambient1)
1000	1	(LED2+Ambient2+ LED1+Ambient1) /4	—	—	—	—	—
Other settings	Do not use						

Table 28. FIFO partitioning across multiple phases[1]

[1]Data marked as AMB2 is replaced by LED3 when the third LED is enabled
[2]When the Decimation mode data is stored in the FIFO, the phases correspond to the corresponding decimation mode outputs

The FIFO depth that is utilized depends on the number of phases of data that are selected to be stored in the FIFO (FIFO_N_PHASE). FIFO_DEPTH is equal to FIFO_PERIOD*FIFO_NPHASE. For example, when only one phase of data is selected to be stored (FIFO_NPHASE=1), then the FIFO_DEPTH is equal to FIFO_PERIOD. However, if 4 phases of data are selected to be stored, then the FIFO_DEPTH is equal to FIFO_PERIOD*4.

Figure 14 illustrates the manner in which the FIFO gets filled when 4 phases of data are selected to be stored.

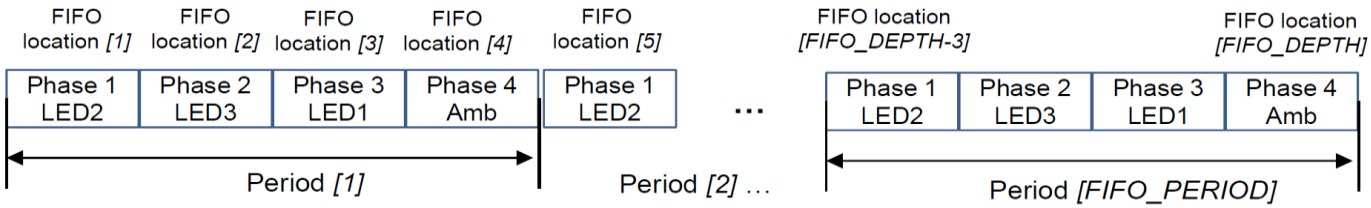


Figure 14. Scheme for FIFO write for the case where 4 phases of data are selected to be stored

3.9.2 FIFO_RDY interrupt generation

The FIFO_RDY interrupt is an indicator of when the FIFO is filled to a depth equal to FIFO_DEPTH and ready for readout by the MCU. The FIFO_RDY interrupt comes with a periodicity equal to (PRF/FIFO_PERIOD). For example, if the PRF is 120 Hz and FIFO_PERIOD is 60 periods, then the periodicity of FIFO_RDY is equal to 2 Hz.

The FIFO_RDY pulse is periodic over FIFO_PERIOD periods. The duration between two consecutive FIFO_RDY pulses constitutes a FIFO write cycle. By default, the pulse width of the FIFO_RDY pulse is the same as the pulse width of DATA_RDY (as set by the registers DATA_RDY_STC and DATA_RDY_ENDC). However, by programming a number using the register control FIFO_EARLY, the start of FIFO_RDY can be advanced by a number of periods equal to FIFO_EARLY. The FIFO_EARLY can be set based on the estimate of how long it will take for the MCU to wake up before it is able to read the FIFO data. For example, the MCU can be set to wake up on the rising edge of FIFO_RDY. The falling edge of FIFO_RDY can be used as an indicator that the FIFO data is ready for readout. Figure 15 shows the scheme of FIFO_RDY generation for two different values of FIFO_EARLY.

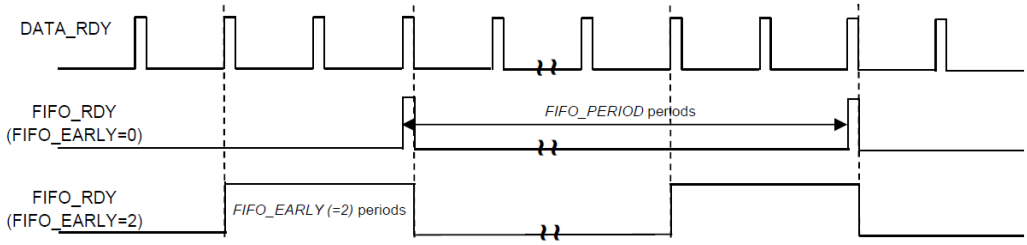


Figure 15. Scheme for FIFO_RDY generation for FIFO_EARLY=0 and FIFO_EARLY=2

The FIFO_RDY can be output on any of the interrupt pins. Refer to the Interrupts section for more details

When the FIFO_RDY interrupt is brought out on the ADC_RDY pin, a FIFO_RDY interrupt event can be registered by reading out a register bit called FIFO_TOGGLE. This register bit toggles between 0 and 1 every time a FIFO_RDY interrupt is issued on the ADC_RDY pin. Reading the FIFO_TOGGLE bit at every FIFO_RDY interrupt can serve as an added check to help ascertain that the MCU has not missed a single FIFO_RDY interrupt. The update of the FIFO_TOGGLE bit is shown in Figure 16.

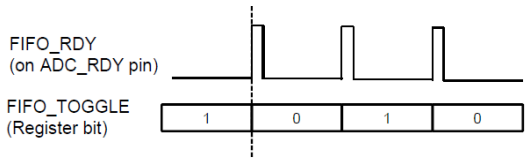


Figure 16. Update of FIFO_TOGGLE register bit

3.9.3 Progression of FIFO read and write pointers

The FIFO write pointer moves automatically in a circular manner as new data gets written into the FIFO. After the ADC conversions are completed in every new PRF cycle, the FIFO write pointer advances by a count equal to FIFO_NPHASE. The FIFO read pointer is a sum of two fields: the read start address and the read offset address. At every FIFO_RDY interrupt, the read start address automatically increments by a number of counts equal to FIFO_DEPTH. There is no mechanism to reverse this increment or to force the read start address. So the data corresponding to a FIFO cycle has to be completely read out before the next FIFO_RDY interrupt. The read offset address is reset to 0 when the chip gets a software or hardware reset and subsequently increments by 1 every time a FIFO word (3-byte) is read out. Under normal circumstances, the read offset address is 0 when the first data corresponding to a FIFO read cycle is read out. As every subsequent FIFO word is read out, the read offset address increments by 1. When the final FIFO word for the cycle is read out, the read offset address has a value equal to (FIFO_DEPTH-1). So at the next FIFO_RDY, the read start address increments by FIFO_DEPTH and the read offset address wraps back to 0. As a result, the FIFO read pointer moves without a break to the first location corresponding to the new FIFO read cycle. To ensure that the read offset pointer starts at 0 at the start of every FIFO read cycle, an exact number of words equal to FIFO_DEPTH should be read out in every FIFO read cycle. An example of a proper and a faulty readout are both illustrated in Figure 17.

The read offset pointer can also be reset to 0 or forced to a programmable value at any time using the register controls FORCE_FIFO_OFFSET and FIFO_OFFSET_TO_FORCE. For example, programming FORCE_FIFO_OFFSET to 1 and FIFO_OFFSET_TO_FORCE to 0 at the start of the FIFO read cycle explicitly forces the read offset address to 0 at the start of every new continuous FIFO read. Subsequent FIFO reads in continuous read mode result in the auto-increment of the read offset pointer. The out-of-sequence FIFO word corresponding to the read pointer (3*FIFO_DEPTH-1) in the faulty case shown in Figure 17 would have been avoided if the read offset address was reset to 0 using the register controls prior to the start of the read. However, there is no way to go back and read the FIFO word corresponding to the read pointer (2*FIFO_DEPTH-1) that was missed in the previous cycle due to an incomplete readout.

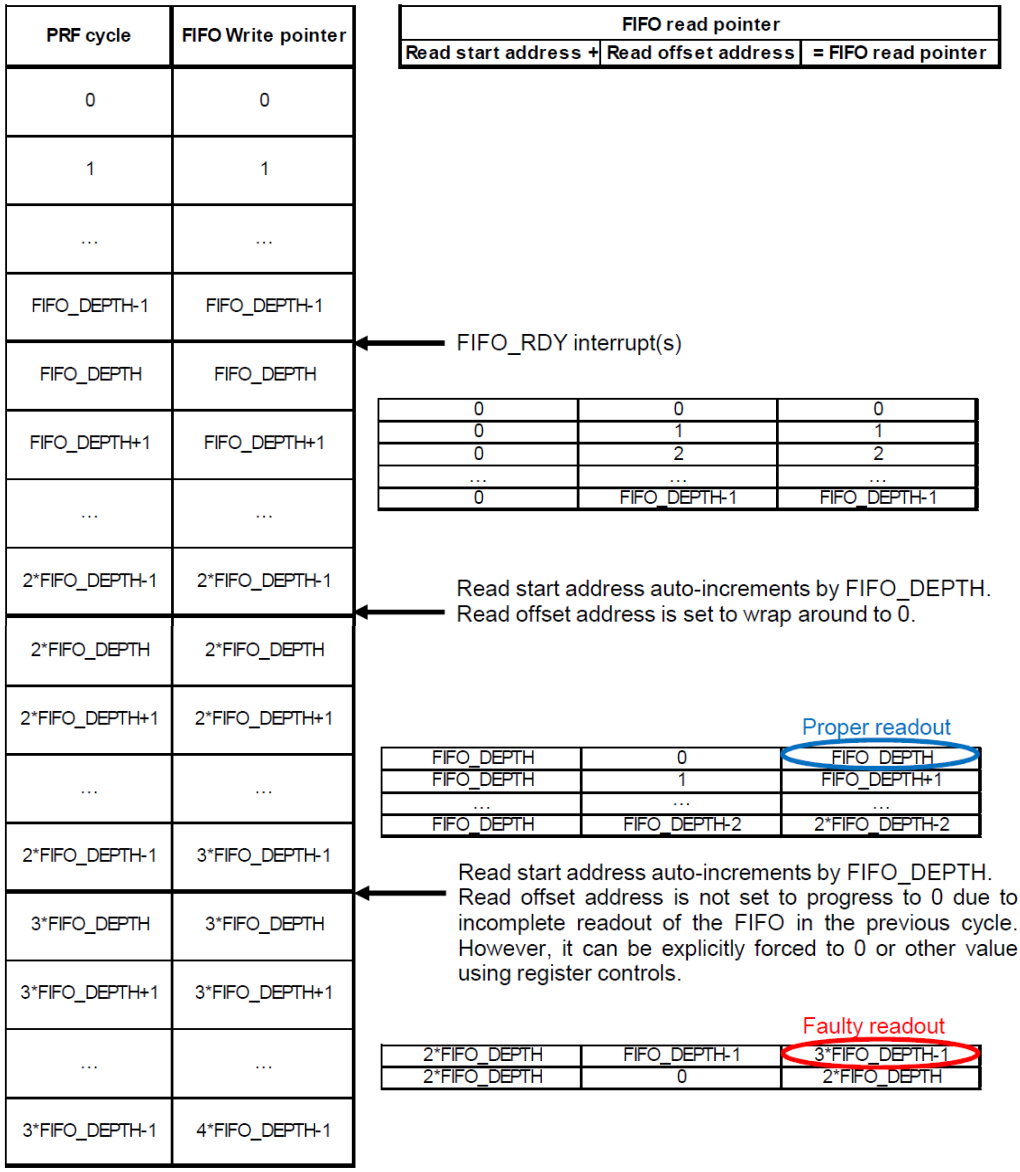


Figure 17. Progression of FIFO read and write pointer

Checking the status of the FIFO_TOGGLE bit and explicitly forcing the FIFO read offset address to 0 at the start of every FIFO read cycle can serve as a mechanism to detect and correct for faults arising from an incorrect FIFO readout.

3.9.4 Considerations When Forcing the FIFO Read Offset

The FIFO read offset address forced through FORCE_FIFO_OFFSET and FIFO_OFFSET_TO_FORCE forces the FIFO offset address at the start of every fresh burst of continuous FIFO readouts. If the FIFO offset force is not removed in a timely manner, duplicate or incorrect data can be read out, as shown in Figure 18.

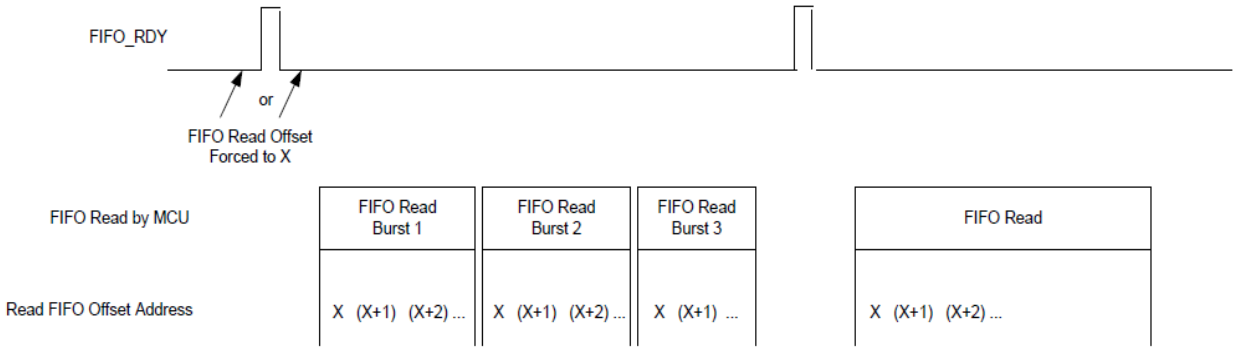


Figure 18. Read Offset Address of the FIFO When FORCE_FIFO_OFFSET is Enabled

The recommended method for proper assertion and deassertion of the FORCE_FIFO_OFFSET feature is illustrated in Figure 19 (for when the entire depth of the FIFO is completed in a single burst) and in Figure 20 (for when the read is br oken up into multiple bursts). Note the requirement for two register writes in register 51h when releasing the FORCE_FIF O_OFFSET mode.

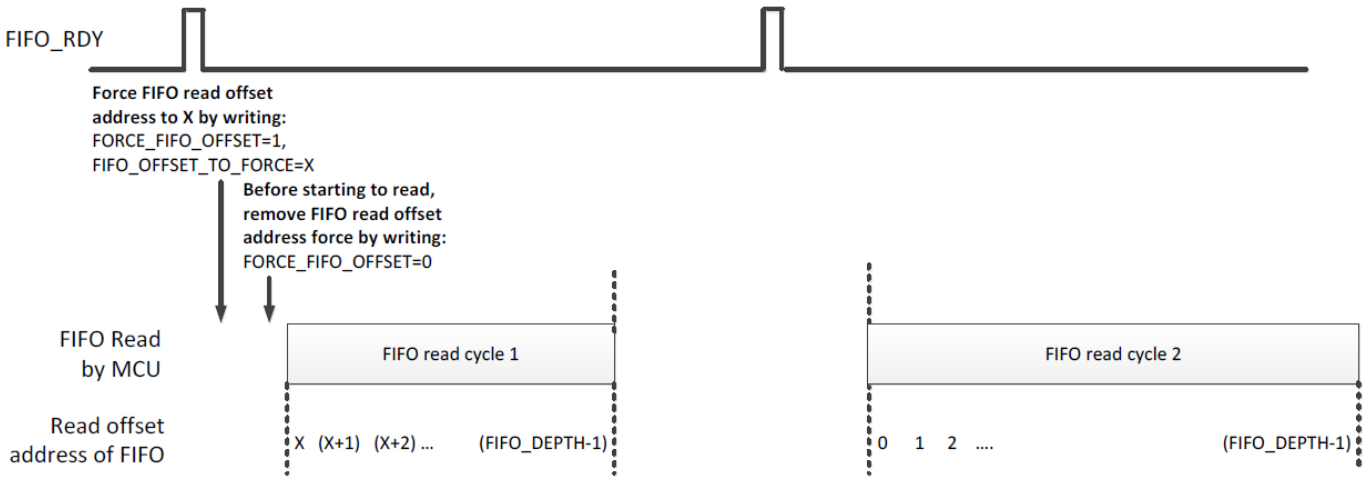


Figure 19. Recommended Method to Deassert FORCE_FIFO_OFFSET When Using a Single Read Burst to Read the FIFO

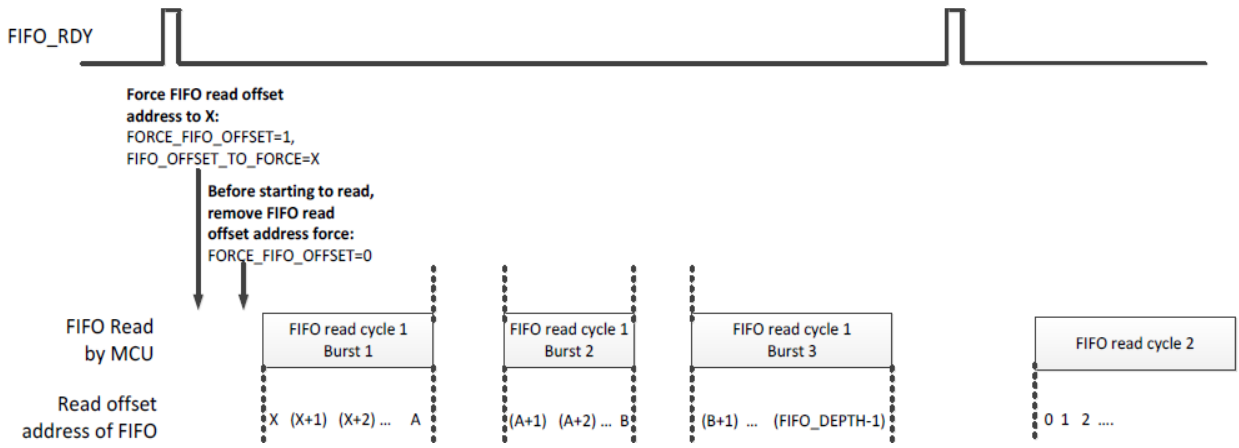


Figure 20. Recommended Method to Deassert FORCE_FIFO_OFFSET When Using Multiple Read Bursts to Read the FIFO

3.9.5 Achieving Deterministic operation while enabling and reading from the FIFO

The FIFO read and write pointers are reset to 0 whenever a hardware or software reset is applied. The FIFO write pointer progresses every period when the timing engine is enabled. This is irrespective of whether the FIFO is enabled or not (FIFO_EN is '0' or '1'). The read start address also progresses irrespective of whether the FIFO is enabled or not. On the other hand, the read offset address increments every time the MCU attempts to read from the FIFO if the FIFO is enabled. With these factors in consideration, the following guidelines are recommended to be followed in order to get deterministic operation from the FIFO:

To enable the FIFO for the first time after powering up the device, follow the below sequence:

1. After powering up the device, apply a reset (software reset or through the RESETZ pin). This resets the FIFO read and write pointers to 0.
2. Configure all the device settings including the timing registers as well as the FIFO settings. Enable the FIFO by setting FIFO_EN=1. Do not attempt to read any data from the FIFO as that will disturb the read offset address.
3. When ready to start operation, set TIMEREN to 1
4. On receiving the first FIFO_RDY (and every subsequent FIFO_RDY), read the full depth of the FIFO before the next FIFO_RDY

The associated timing diagram with the sequence is shown in Figure 21.

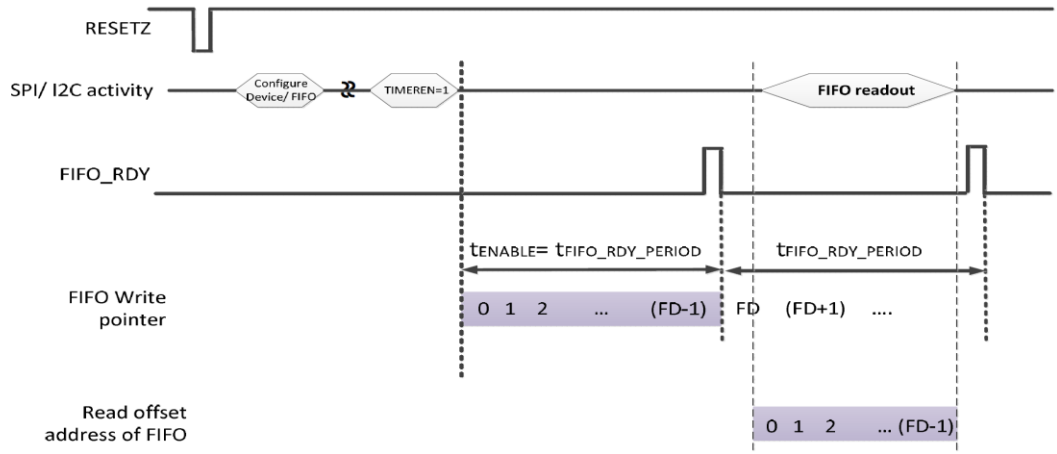


Figure 21. Recommended scheme to enable the FIFO the first time after reset

The FIFO can be disabled in the middle of its operation by setting FIFO_EN=0 and then re-enabled by setting FIFO_EN=1.

3.9.6 FIFO readout timing constraints

The time window in which the MCU can read the data from the FIFO is indicated in Figure 22.

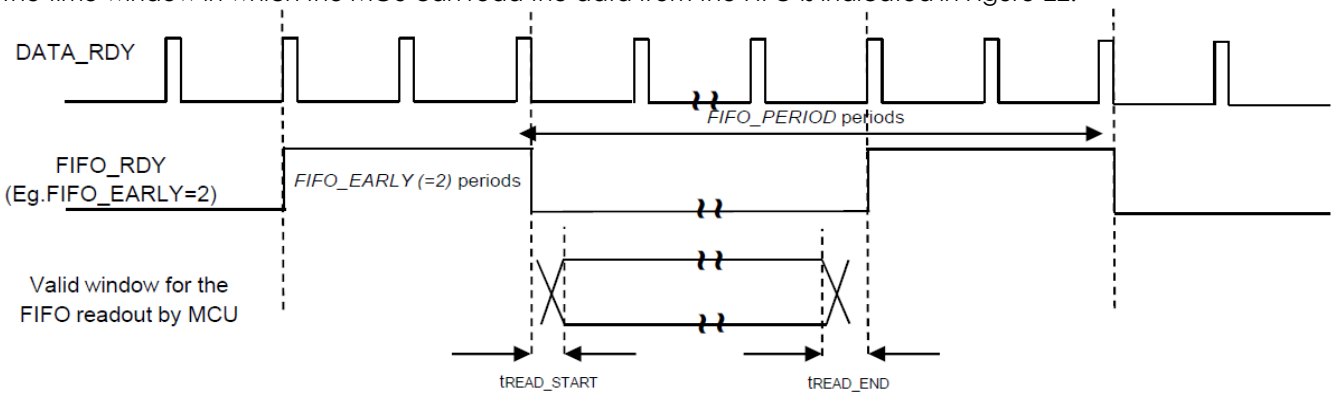


Figure 22. Time window for the MCU to read the FIFO

The timing parameters associated with the start and end of the allowed FIFO read window is as shown in Table 29.

		MIN	TYP	MAX	UNIT
t_{READ_START}	FIFO_RDY falling edge to start of valid FIFO read window	0			µs
t_{READ_END}	Time that the valid FIFO read window ends before the FIFO_RDY rising edge	$10 \times t_{TE}$ (1)			µs

Table 29. Timing parameters associated with the readout window of the FIFO

(1) t_{TE} refers to one clock period of CLK_TE

The FIFO can be read out in continuous readout mode of the I^2C interface or the SPI interface. On receiving a FIFO_RDY interrupt, the MCU should set the readout register address to FFh and continuously read out the data. Starting from the first data of the previous Write cycle, the FIFO outputs each 3-byte data on to the I^2C interface. The MCU should read out the entire depth of the FIFO (FIFO_DEPTH) before the next FIFO_RDY and then stop reading.

3.9.7 Performance considerations related to FIFO readout

The FIFO readout through the I²C interface is a bursty and periodic event with a periodicity of multiple (FIFO_PERIOD) pulse repetition periods. To minimize the noise coupling into the analog portion of the receiver from the readout activity, it is recommended that the FIFO readout not be done during the active part of the pulse repetition period. The first way to achieve this is by reading out the entire FIFO during the dynamic powerdown phase (PDNCYCLE) immediately following the FIFO_RDY pulse. This is shown in Figure 23.

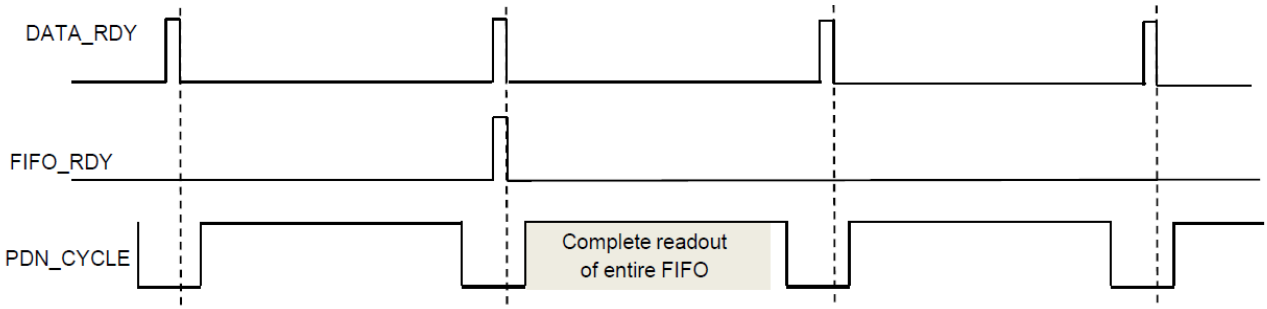


Figure 23. Time window for the MCU to read the FIFO

If the FIFO depth is high or the PRF is high, a scheme as shown in Figure 23 may not be feasible. In that case, the scheme shown in Figure 24 can be used to read out the FIFO. The PDN_CYCLE phase can be identified by the MCU by programming the same timing on one of the spare interrupts (INT_OUT1 or INT_OUT2) and making it output on one of the interrupt outputs (Eg. on PROG_OUT1)

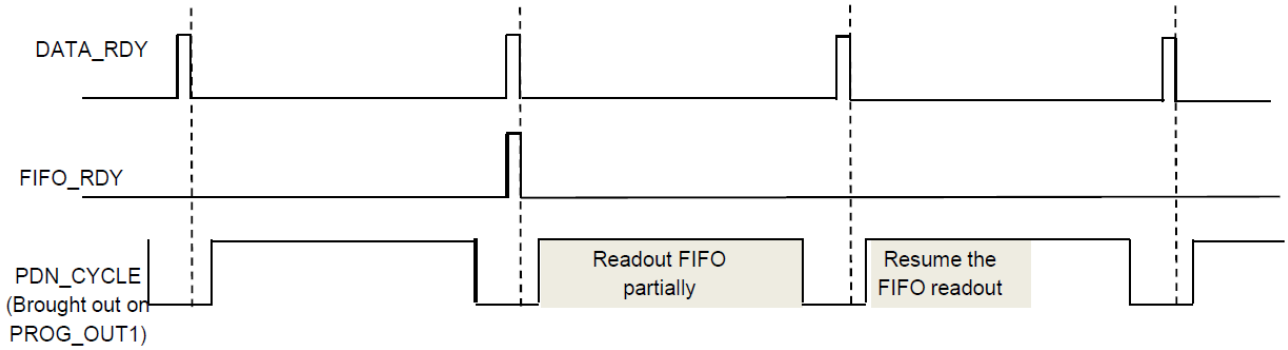


Figure 24. FIFO readout over multiple PDN_CYCLE phases

3.9.8 Watermark FIFO mode

The FIFO mode of operation described thus far is referred to as the ***Normal FIFO mode***. The Normal FIFO mode is one where the FIFO_RDY is generated periodically based on the programmed value of FIFO_PERIOD. The PPSI262 has another FIFO mode where the FIFO_RDY is generated based on a programmed difference between the current locations of the write and read pointers – referred to as the Watermark level.

This FIFO mode, referred to as the ***Watermark FIFO mode*** can be programmed using the WM_MODE register control. In this mode, the FIFO_RDY gets generated when the difference between the Write and Read pointers exceeds a programmed Watermark (WM) level referred to as *WM_FIFO*. The REG_FIFO_PERIOD register control bits used to set FIFO_PERIOD in the Normal FIFO mode are repurposed as the REG_WM_FIFO register control in the Watermark FIFO mode and are used for setting *WM_FIFO*. The REG_WM_FIFO register control sets the Watermark level (WM_FIFO) to be equal to (REG_WM_FIFO + 1). With *WM_FIFO* thus set, the FIFO_RDY interrupt is now an indication to the MCU that a number of samples equal to *WM_FIFO* are ready to be read out. It is to be noted that while the REG_FIFO_PERIOD register control used in the Normal FIFO mode referenced the number of *periods* (with the relation between the number of periods and number of FIFO samples determined by the FIFO_PARTITION setting), the REG_WM_FIFO register control in the Watermark FIFO mode directly references the number of FIFO *samples*. *WM_FIFO* should therefore be chosen to be a multiple of *FIFO_NPHASE*. If the MCU fails to start reading before the completion of the first cycle after FIFO_RDY, then the FIFO_RDY interrupt comes again in the next cycle – this is now an indication that (*WM_FIFO+FIFO_NPHASE*) samples need to be read out

The instantaneous difference between the write and read pointers can be read out through an 8-bit register REG_POINTER_DIFF. The difference between the write and read pointers (*POINTER_DIFF*) is equal to (REG_POINTER_DIFF+1). On receiving a FIFO_RDY, the MCU can read out this register (prior to reading out the FIFO) to confirm that *POINTER_DIFF* is indeed equal to *WM_FIFO*. Figure 25 illustrates the case of how the FIFO_RDY interrupt gets generated in the Watermark FIFO mode for a case where *WM_FIFO* is set to 32. The MCU is shown as reading only 8 samples after receipt of the first FIFO_RDY.

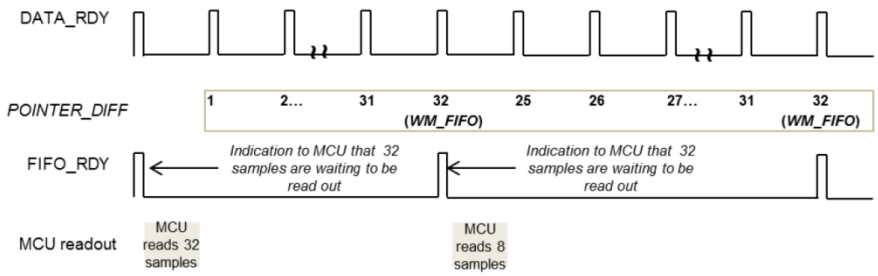


Figure 25. FIFO mode based on programmable watermark level

In addition to the automatic progression of the read pointer (increment with every read), the Read pointer can also be forced relative to Write pointer by setting the FORCE_FIFO_OFFSET to '1', and then programming FIFO_OFFSET_TO_FORCE to set the location of the Read pointer relative to the current location of the Write pointer.

The generation of FIFO_RDY interrupt can be masked using the MASK_FIFO_RDY register control. Such masking may be useful in cases where the MCU is not interested in reading data from the AFE for a period of time but wants to retrieve prior data stored in the FIFO when it starts reading again. The recommended method of achieving this is shown in Figure 26.

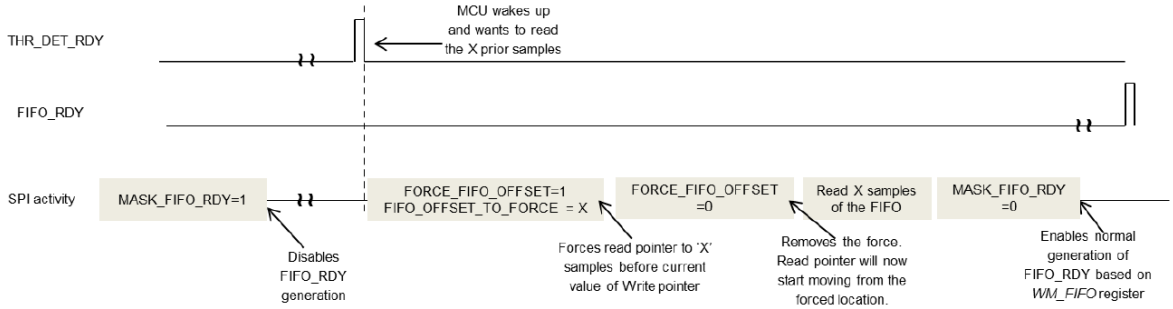


Figure 26. Method of resuming FIFO read following a FIFO_RDY masking phase

4 Device Functional Modes

4.1 Power Modes

The PPS1262 has the following power modes:

1. Normal operation mode: In this mode, the device is in Active mode for at least a fraction of the PRF and may or may not be in a Deep Sleep state for the rest of the PRF cycle. The transition from the Active mode to the Deep sleep mode is automatically controlled by the internal timing engine.
1. Hardware power-down mode (PWDN): this mode is set using the RESETZ and CONTROL1 pins. With the CONTROL 1 pulled low, if the RESETZ pin is pulled low for more than 200 µs, the device enters hardware power-down mode where the power consumption is very low (of a few microamps). In the hardware power- down mode, the conte nts of the registers are erased.
2. Software power-down mode (PDNAFE): This mode is enabled by using a register bit.

It is recommended to shut off the external clock during the powerdown mode. Also, if the SPI interface is used as the interface to the AFE (I2C_SPI_SEL='1'), it is recommended to pull the I2C_SPI_SEL low during hardware power-down mode to cut off the leakage current through the internal pull-down resistor on I2C_SPI_SEL.

4.2 RESET Modes

The PPSI262 has internal registers that must be reset after powering up the supplies and before valid operation.

There are two ways to reset the device:

1. Either through the RESETZ pin (a reset signal can be issued by pulsing the RESETZ pin low for a duration of time between 25 to 50 µs) or
2. A software reset via the SW_RESET register bit. This is a self-clearing bit.

4.3 LDO Modes

The PPSI262 has the following LDO modes:

1. LDO Enable mode: Set by CONTROL1 to 0V
2. LDO Bypass mode: Set by connecting CONTROL1 to RX_SUP

4.4 Decimation Modes

The device has a decimation mode which can be enabled using the register control DEC_EN. In this mode, the device averages the LED output code (after subtracting the corresponding ambient phase)and stores it in the registers AVG_LED2_ALED2VAL and AVG_LED1_ALED1VAL as shown in Table 30. Additionally, by setting the FIFO_EN_DEC register bit, any of the phases of LED or Ambient data from the Decimation mode output can be stored in the FIFO using a mapping similar to the one shown in Table 31. With the FIFO enabled in the Decimation mode, the periodicity (time) of the FIFO_RDY interrupt gets divided by the Decimation factor.

Register	Contents of the register
AVG_LED2_ALED2VAL	Averaged output of LED2 phase code minus Ambient2 phase code
AVG_LED1_ALED1VAL	Averaged output of LED1 phase code minus Ambient1 phase code

Table 30. Contents of AVG_LED2_ALED2VAL and AVG_LED1_ALED1VAL in Decimation mode

(1) Data from decimation mode are not stored in the FIFO. The combination of decimation mode and FIFO enable is not supported.

The averaging is done over multiple PRF cycles. The number of PRF cycles over which the averaging is done can be programmed through the register control DEC_FACTOR as shown in Table 31.

DEC_FACTOR	Number of samples averaged (Decimation factor)
0	1
1	2
2	4
3	8
4	16
5,6,7,8	Do not use

Table 31. Number of cycles of averaging (Decimation factor) as a function of DEC_FACTOR

When the Decimation mode is enabled, the periodicity of the DATA_RDY interrupt automatically scales down by a factor equal to the Decimation Factor. For example, when the decimation factor is set to 4, the periodicity of the DATA_RDY becomes PRF/4. The timing of the Decimation mode for a Decimation factor of 4 is shown in Figure 27. Also, when the FIFO is used to store the Decimation mode data, the periodicity (time) of the FIFO_RDY interrupt gets multiplied by the Decimationfactor.

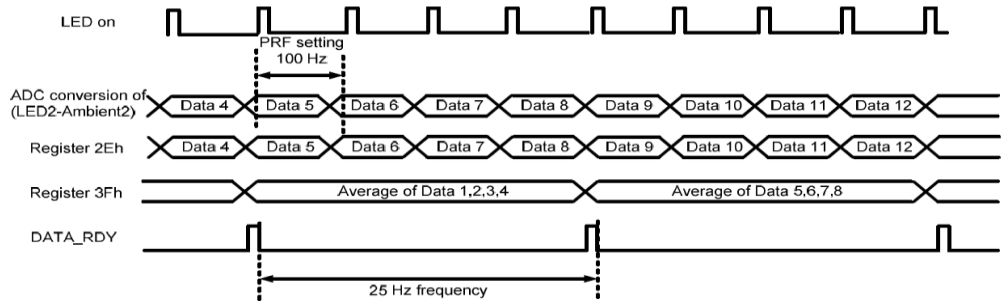


Figure 27. Decimation mode Timing diagram (Decimation factor=4, PRF=100Hz)

The decimation mode retains the SNR advantage of sampling at a high PRF while relaxing the output data rate to a lower rate. This is illustrated in Table 32.

MODE	RATE OF DEVICE SAMPLES AND COVERSIONS	RATE OF MCU DATA READS	RELATIVE PERFORMANCE
No decimation, 100 Hz PRF	100 Hz	100 Hz	Reference
No decimation, 25 Hz PRF	25 Hz	25 Hz	SNR 6 dB lower than reference
4X Decimation mode, 100 Hz PRF	100 Hz	25 Hz	No SNR lowering from reference

Table 32. Different modes of operation

4.5 Threshold Detect Mode

The device has a threshold detect mode that can be enabled using the THR_DET_EN register control. In this mode, the device detects if the averaged output code of a particular phase is within the programmed lower and upper limits. If the output code is within the limits, the THR_DET_RDY interrupt goes high during the corresponding window of the DAT A_RDY pulse. The 24-bit ADC code is compared against lower and upper limits that are set using 24-bit codes THR_DET _LOW_CODE and THR_DET_HIGH_CODE. The mapping of these codes to the register controls is shown in Table33.

24-bit Code used for threshold comparison	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THR_DET_LOW_CODE	THR_DET_LOW_CODE3								THR_DET_LOW_CODE2								THR_DET_LOW_CODE1							
THR_DET_HIGH_CODE	THR_DET_HIGH_CODE3								THR_DET_HIGH_CODE2								THR_DET_HIGH_CODE1							

Table 33. Mapping of the register controls to the Low and High threshold code

The THR_DET_PHASE_SEL register control determines which phase of the output data is compared against the low and high thresholds, as shown in Table34.

THR_DET_PHASE_SEL<8:0> binary setting	OUTPUT PHASE CODE USED FOR THRESHOLD DETECT (1)
XXXXXXXX1	LED2-AMB2
XXXXXXX10	LED2
XXXXXX100	AMB2
XXXXX1000	LED1
XXXX10000	AMB1
XXX100000	LED2-AMB1
XX1000000	AMB2-AMB1
X10000000	LED1-AMB2
100000000	LED1-AMB1

(1)AMB2 corresponds to LED3/SAMP3 and AMB1 corresponds to LED4/SAMP4

Table 34. Output Phase Used for Threshold Detect Based on the THR_DET_PHASE_SEL Value

CHANGE_SEL_LOGIC – Binary setting	Logic for generation of THR_DET_RDY
00	Generated when output code goes IN-RANGE of range set by high and low thresholds
01	Generated when output code goes OUT-OF-RANGE of range set by high and low thresholds
Other setting	Do not use

Table 35. Generation of THR_DET_RDY interrupt based on CHANGE_SEL_LOGIC control

The number of averages of the output code taken to compare against the thresholds depends on the DEC_FACTOR register control, as shown in Table36.

DEC_FACTOR	NUMBER OF SAMPLES AVERAGED BEFORE COMPARISON WITH HIGH AND LOW THRESHOLDS
0	1
1	2
2	4
3	5
4	16
5, 6, 7, 8	Do not use

Table 36. Number of Samples Averaged in Threshold Detect Mode Before Comparison with Thresholds

The THR_DET_RDY interrupt has the same timing as the DATA_RDY interrupt (start and end counts as set by DATA_RDY_ STC and DATA_RDY_ENDC) and a periodicity equal to PRF / (number of samples averaged).

The timing of the THR_DET_RDY interrupt generation is shown in Figure 28 when the number of averages is set to 4.

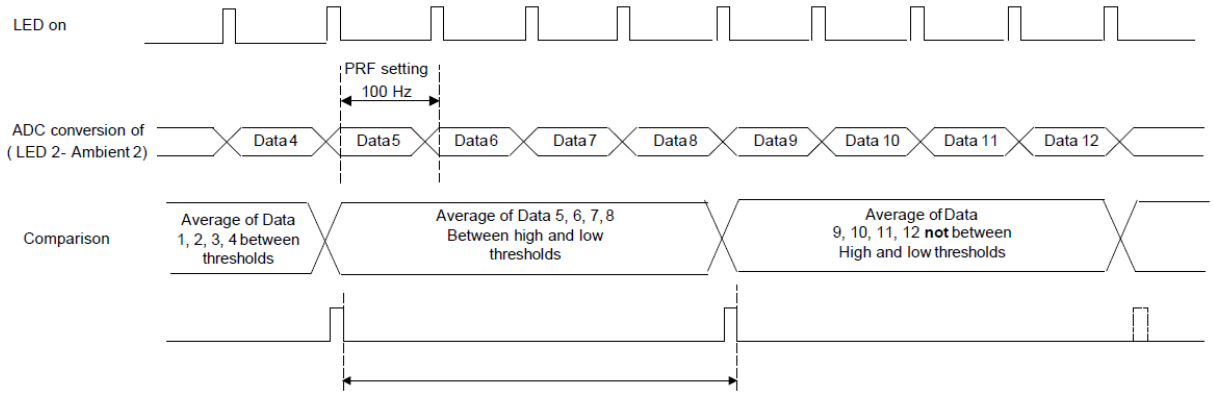


Figure 28. THR_DET_RDY Interrupt Generation Timing Diagram

5. Programming

5.1 I²C Interface

5.1.1 I²C Protocol

The PPSI262 has an I²C interface for communication. The I2C_CLK and I2C_DAT lines require external pullup resistors to IO_SUP. Refer to the I²C protocol standards documents for details of the I²C interface. This section only describes certain key features of the interface. The data on I2C_DAT must be stable during the high level of I2C_CLK and may transition during the low level of I2C_CLK, as shown in Figure 29.

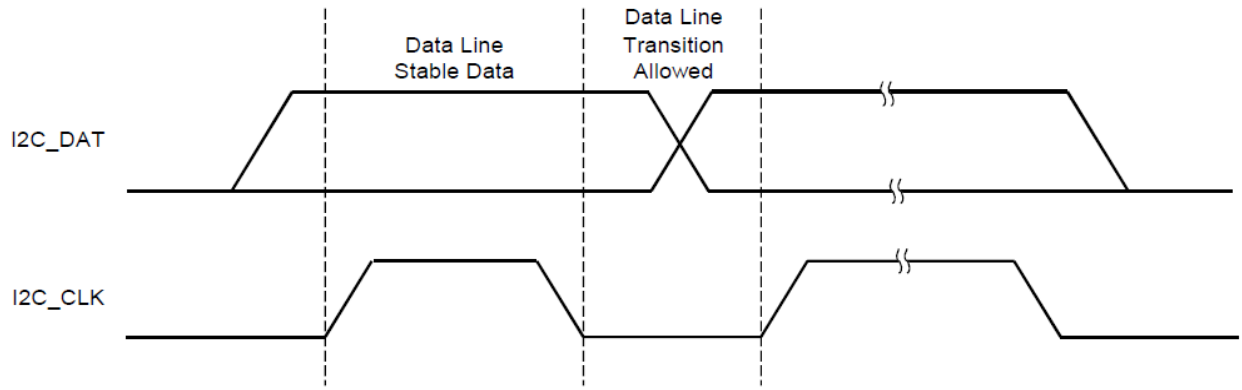


Figure 29. Allowed Transition of I2C_DAT while Transmission of Data Bits

The start condition is indicated by a high-to-low transition of the I2C_DAT line when the I2C_CLK is high. A stop condition is indicated by a low-to-high transition of the I2C_DAT line when the I2C_CLK is high. Figure 30 shows the start and stop conditions.

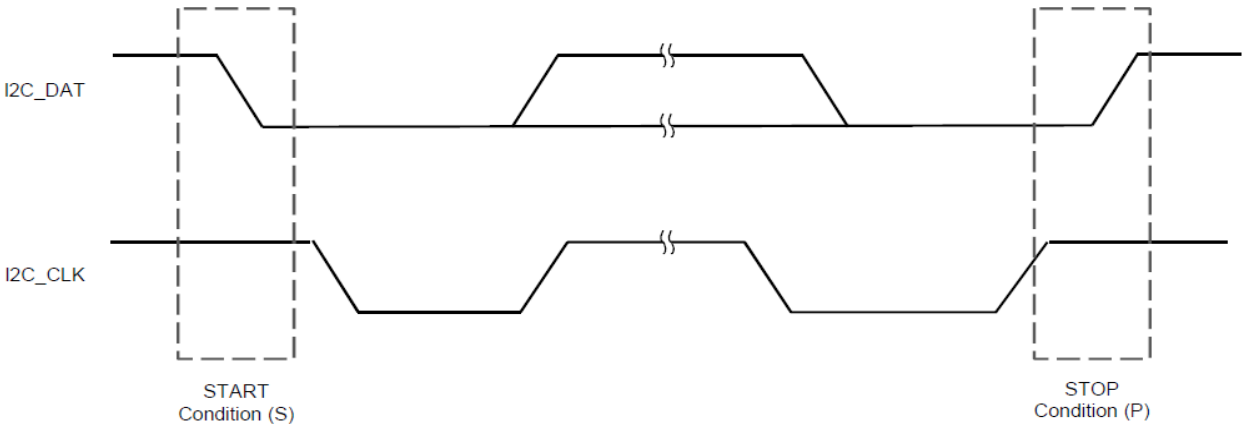
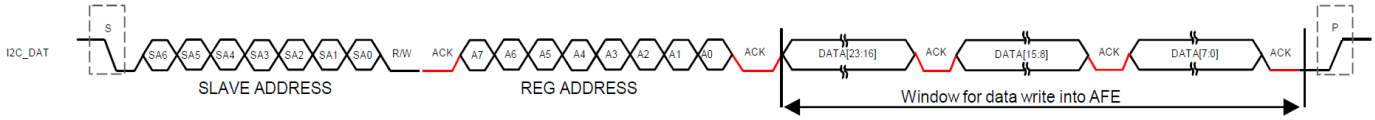


Figure 30. Transition of I2C_DAT during Start and Stop Conditions

5.1.2 I²C write and read

With the previously mentioned protocols for data, start, and stop conditions, the write and read operations are as shown in Figure 31 and Figure 32, respectively. The slave address for the PPSI262 (indicated as SA6 to SA0) is a 7- bit representation of either address 5Ah (when the SEN pin is high) or 5Bh (when the SEN pin is low). The R/W bit is the read/write bit and is set to 1 for reads and 0 for writes. In Figure 31 and Figure 32, the activity performed by the host is shown in black whereas the activity from the PPSI262 is shown in red. Thus, after the host sends the slave address during a write operation, the PPSI262 pulls the I2C_DAT line low (shown as ACK) if the slave address matches 5Ah (when SEN is high) or 5Bh (when SEN is low). Similarly, the host pulls the I2C_DAT line high (shown as NACK) as an acknowledgment of a successfully completed read operation involving three bytes of data.



(1) Activity performed by the host is shown in black whereas the activity from the PPSI262 is shown in red.

Figure 31. I²C Write Option Timing

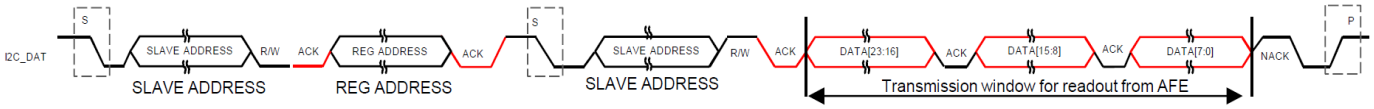


Figure 32. I²C Read Option Timing

5.1.3 Continuous I²C Read/Write mode

Continuous read/write mode is supported by enabling the RW_CONT bit. The FIFO, however, can be read out continuously without setting this bit. The protocol for the continuous write and read modes are shown in Figure 33 and Figure 34, respectively.

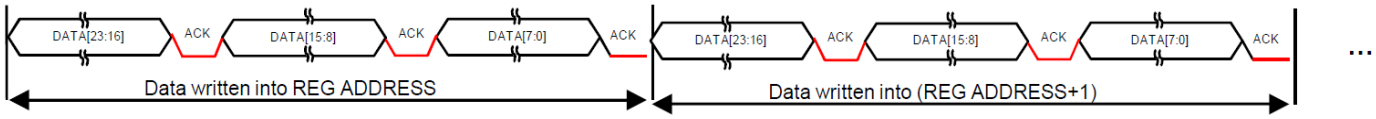


Figure 33. Window for data write into PPSI262 in continuous I²C Write mode (RW_CONT=1)

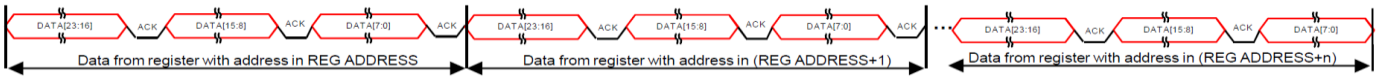


Figure 34. Transmission window for readout from PPSI262 in continuous I²C Read mode (RW_CONT=1)

5.1.4 Data readout from FIFO using a single continuous read operation

When the MCU receives the FIFO_RDY interrupt, the FIFO can be read out through the I²C interface in continuous readout mode, as shown in Figure 35. The REG ADDRESS for reading out the FIFO is FFh. The MCU must read out the full depth of the FIFO before the next FIFO_RDY. Additional restrictions on the FIFO readout timing are mentioned in the FIFO Readout Timing Constraints section.

Figure 35. I²C Readout from FIFO

5.1.5 Data readout from FIFO over multiple read operations

The data from the FIFO can also be read out over multiple read operations with a break in between. A readout over two such read operations as shown in Figure 36 The restrictions on the FIFO readout timing mentioned in the FIFO data readout section continue to apply for this kind of FIFO readout.

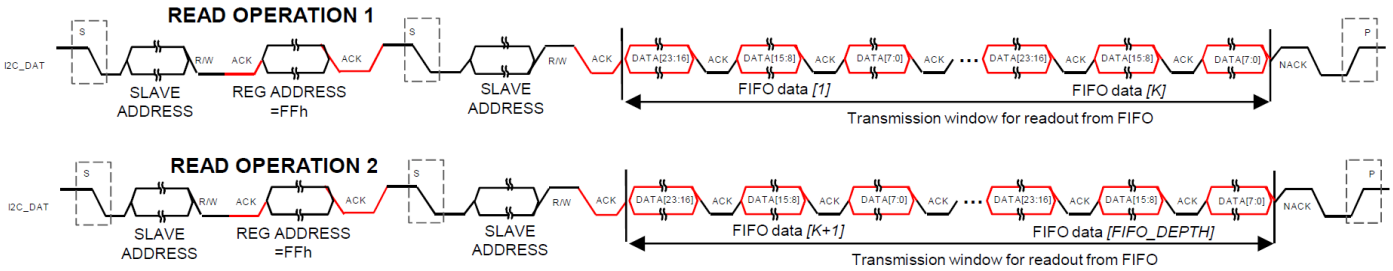


Figure 36. I²C Readout from FIFO over two read operations

5.2 SPI Interface

5.2.1 SPI programming interface

The SPI interface consists of four signals: SCLK (serial clock), SDOUT (serial interface data output), SDIN(serial interface data input), and SEN (serial interface enable).

The SPI interface is enabled by setting the I2C_SPI_SEL pin high. Note that the logic high level of I2C_SPI _SEL corresponds to the RX_SUP voltage level. When operating in SPI interface mode, the pins are reconfigured as shown in Table 37.

PIN		PIN FUNCTION IN SPI INTERFACE MODE
NAME	No.	
I2C_CLK	F3	SCLK : serial clock input
I2C_DAT	F2	SDIN : serial clock data
SEN	E3	SEN : chip select (active low)
SDOUT	E2	SDOUT : serial data output

Table 37. Pin function in SPI interface mode

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on SDOUT. Data are clocked in on SDIN. Even though the input has hysteresis, SCLK is recommended to be kept as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low. The serial interface enable (SEN) enables the serial interface to clock data from SDIN into the device.

5.2.2 Writing data

The SPI_REG_READ register bit must be set to 0 before writing to a register. When SEN is low:
- Serially shifting bits into the device is enabled.
- Serial data (on SDIN) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

The first eight bits form the register address and the remaining 24 bits form the register data. Figure 37 shows an SPI timing diagram for a single write operation.

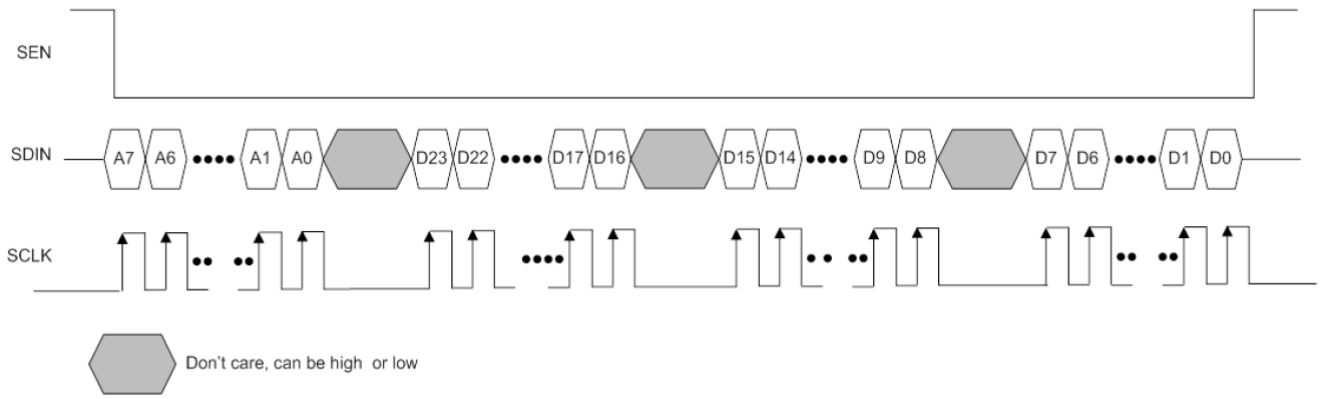
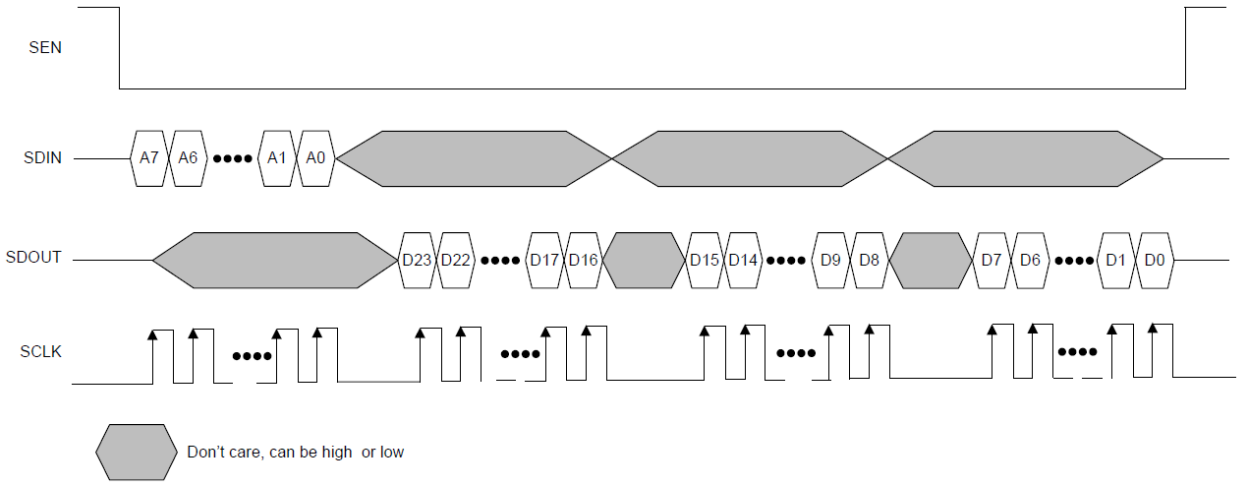


Figure 37. PPSI262 SPI write timing diagram

5.2.3 Reading data

The PPSI262 includes a mode where the contents of the internal registers can be read back on SDOUT. This mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_REG_READ register bit using the SPI write command. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the PPSI262 outputs the contents of the specified register on the SDOUT pin. Figure 38 shows an SPI timing diagram for a single read operation. By default, the SDOUT pin is not tri-state even when SEN is high (inactive).
There are two modes to control the tristate for the SDOUT pin:

(i) Static Tristate mode: In this mode, the SDOUT buffer is forced into tristate always. The Static Tristate mode can be set by programming the SDOUT_TRISTATE bit to 1.
(ii) Dynamic Tristate mode: In this mode, the SDOUT buffer is forced into tristate only whenever SEN is high (inactive). The Dynamic Tristate mode can be set by programming the SDOUT_TRISTATE_D bit to 1.



(1) The SPI_REG_READ register bit must be enabled before attempting a serial readout from the AFE.
(2) Specify the register address of the content that must be read back on bits A[7:0].
(3) The PPSI262 outputs the contents of the specified register on the SDOUT pin.

Figure 38. PPSI262 SPI read timing diagram

5.2.4 Continuous read/write mode in the SPI interface

The SPI interface can be operated in a continuous read or write mode by writing 1 to the RW_CONT bit. In this mode, the address is specified at the start of the read or write cycle. Subsequently, the address of the register being read or written auto-increments until SEN is pulled high. The continuous write and read modes are illustrated in Figure 39 and Figure 40, respectively.

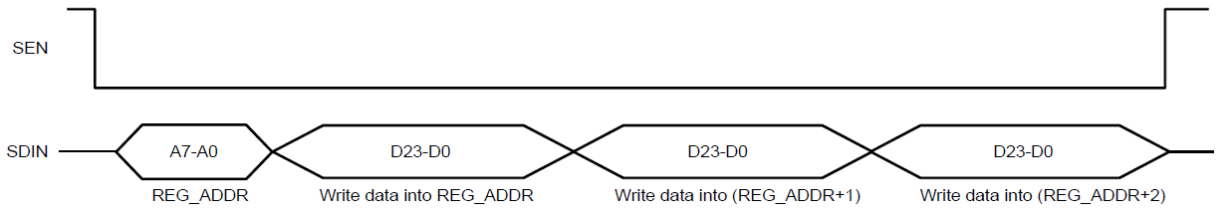


Figure 39. Continuous SPI write (RW_CONT =1)

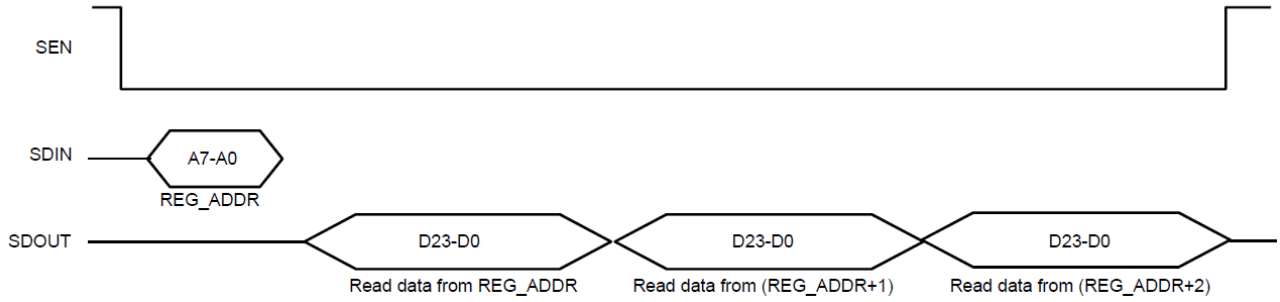


Figure 40. Continuous SPI read (RW_CONT =1, SPI_REG_READ =1)

5.2.5 FIFO readout through the SPI Interface over a single continuous read operation

The contents of the FIFO can be readout in a continuous manner using the SPI interface. The RW_CONT bit is not required to be set to 1 to continuously read out the FIFO. The SPI_REG_READ bit is also not required to be set to 1 when reading out the FIFO. The REG_ADDR used for reading out the FIFO must be set to FFh. The readout method is shown in Figure 41.

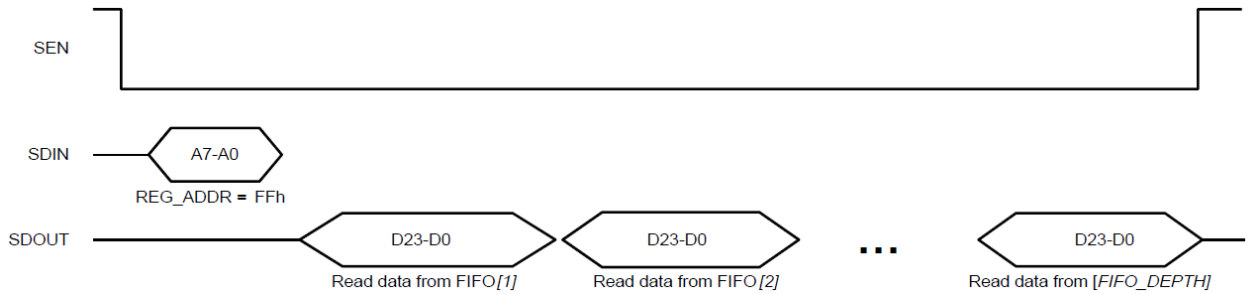


Figure 41. Continuous FIFO readout through the SPI interface

5.2.6 FIFO readout through the SPI Interface over multiple read operation

The FIFO can also be read out over multiple read operations. Figure 42 shows the FIFO being read out over two read operations..

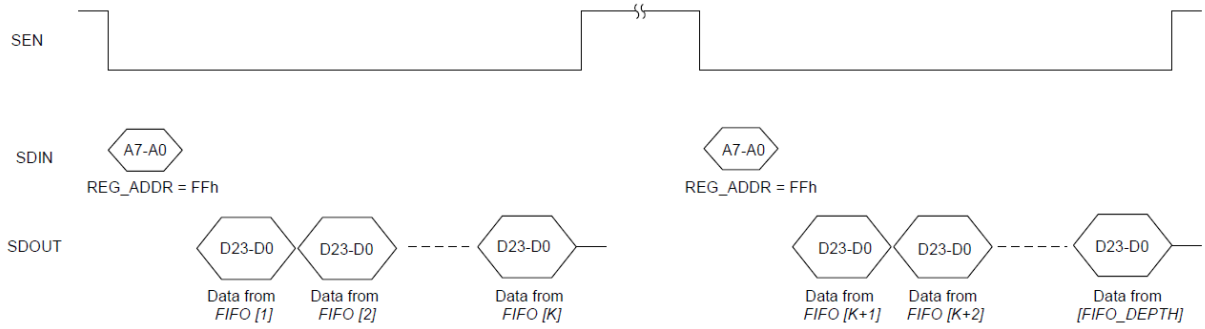


Figure 42. FIFO readout over two read operation

5.3 Interrupts

The device has three output pins, ADC_RDY, PROG_OUT1, and SDOUT, where a variety of interrupts can be output on. The SDOUT is available as an interrupt only in the I2C interface mode. The PROG_OUT1 pin is disabled by default and can be enabled by setting the EN_PROG_OUT1 bit to 1. A variety of interrupts can be multiplexed on the ADC_RDY, PROG_OUT1, and SDOUT pins by using the INT_MUX1, INT_MUX2, and INT_MUX3 controls. The interrupts are described in Table 38.

Interrupt	Description	Effective start count	Value (min)
DATA_ RDY	Interrupt which comes out at the same rate as the output data rate. Rate is equal to PRF when decimation is not enabled and (PRF/DEC_FACTOR) when Decimation is enabled (DEC_EN=1).	DATA_RDY_STC+1	DATA_RDY_ENDC+2
FIFO_RDY	Interrupt which comes once every FIFO Write cycle with a periodicity (in terms of pulse repetition periods) equal to FIFO_PERIOD.	DATA_RDY_STC+2	DATA_RDY_ENDC+3 The end count occurs when the programmed FIFO depth is filled up. The start count is advanced by a number of periods as set by FIFO_EARLY.
THR_DET_ RDY	Threshold detect flag applicable when the device is in Threshold Detect mode - Goes high during the corresponding DATA_RDY window in the periods where the averaged ADC output is between programmed thresholds.	DATA_RDY_STC+2	DATA_RDY_ENDC+3
INT_OUT1	Spare interrupt 1 which is generated as a pulse every period	PROG_INT1_STC	PROG_INT1_ENDC+1
INT_OUT2	Spare interrupt 2 which is generated as a pulse every period	PROG_INT2_STC	PROG_INT1_ENDC+12

Table 38. Description of the various interrupts

The INT_MUX1, INT_MUX2, and INT_MUX3 register controls determine the selection of the interrupts described in Table 33 on the output pins. This selection is shown in Table 39, Table 40, and Table 41.

INT_MUX1	Interrupt output on ADC_RDY pin	Additional controls required
00	DATA_RDY	-
01	THR_DET_RDY	Set THR_DET_EN=1
10	FIFO_RDY	Set FIFO_EN=1
11	Do not use	

Table 39. Selection of interrupts output on ADC_RDY pin

INT_MUX2	Interrupt output on PROG_OUT1 pin	Additional controls required
00	INT_OUT1	EN_PROG_OUT=1
01	DATA_RDY	EN_PROG_OUT=1
10	THR_DET_RDY	EN_PROG_OUT=1, THR_DET_EN=1
11	FIFO_RDY	EN_PROG_OUT=1, FIFO_EN=1

Table 40. Selection of interrupts output on PROG_OUT1 pin

INT_MUX1	Interrupt output on ADC_RDY pin	Additional controls required
00	INT_OUT2	-
01	DATA_RDY	-
10	THR_DET_RDY	Set THR_DET_EN=1
11	FIFO_RDY	Set FIFO_EN=1

Table 41. Selection of interrupts output on SDOUT pin (only in the I^2C interface mode)

5.4 Register Map

ADDR.	REGISTER DATA																						
(Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FIFO_EN	ENABLE_ULP	RW_CONT	SW_RESET	0	TM_COUNT_RST	SPI_REG_READ
01h	0	0	0	0	0	0	0	0	LED2STC															
02h	0	0	0	0	0	0	0	0	LED2ENDC															
03h	0	0	0	0	0	0	0	0	LED1LEDSTC															
04h	0	0	0	0	0	0	0	0	LED1LEDENDC															
05h	0	0	0	0	0	0	0	0	ALED2STC\LED3STC															
06h	0	0	0	0	0	0	0	0	ALED2ENDC\LED3ENDC															
07h	0	0	0	0	0	0	0	0	LED1STC															
08h	0	0	0	0	0	0	0	0	LED1ENDC															
09h	0	0	0	0	0	0	0	0	LED2LEDSTC															
0Ah	0	0	0	0	0	0	0	0	LED2LEDENDC															
0Bh	0	0	0	0	0	0	0	0	ALED1STC															
0Ch	0	0	0	0	0	0	0	0	ALED1ENDC															
0Dh	0	0	0	0	0	0	0	0	LED2CONVST															
0Eh	0	0	0	0	0	0	0	0	LED2CONVEND															
0Fh	0	0	0	0	0	0	0	0	ALED2CONVST\LED3CONVST															
10h	0	0	0	0	0	0	0	0	ALED2CONVEND\LED3CONVEND															
11h	0	0	0	0	0	0	0	0	LED1CONVST															
12h	0	0	0	0	0	0	0	0	LED1CONVEND															
13h	0	0	0	0	0	0	0	0	ALED1CONVST															
14h	0	0	0	0	0	0	0	0	ALED1CONVEND															
1Dh	0	0	0	0	0	0	0	0	PRPCT															

Register Map(continued)

ADDR (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIMEREN	0	0	0	0	NUMAV			
1Fh	0	0	0	0	0	0	0	0	0	TIA_GAIN_SEP3_MSB	TIA_CF_SEP3			TIA_GAIN_ LSB		SEP3_	0	TIA_GAIN_SEP2_MSB	TIA_CF_SEP2			TIA_GAIN_ SEP2_LSB		
20h	0	0	0	0	0	0	0	0	ENSEPGAIN	0	0	0	0	0	0	0	0	TIA_GAIN_SEP_MSB	TIA_CF_SEP			TIA_GAIN_ SEP_LSB		
21h	0	0	0	0	0	0	0	0	0	IFS_OFFDAC			0	0	FILTER_BW(0)	0	0	TIA_GAIN_MSB	TIA_CF			TIA_GAIN_ LSB		
22h	ILED3_ LSB		ILED2_ LSB		ILED1_ LSB		ILED3_MSB						ILED2_MSB						ILED1_MSB					
23h	0	0	0	CONTROL_DYN_TX(0)	0	0	ILED_FS	0	ENSEPGAIN4	CONTROL_DYN_BIAS	0	0	0	0	OSC_ENABLE	0	0	0	0	CONTROL_DYN_TIA	CONTROL_DYN_ADC	0	PDNRX	PDNAFE
24h	0	0	0	0	0	0	0	ILED4_MSB						ILED4_ LSB		0	0	0	0	0	0	0	0	0
28h		FIFO_TOGGLE		DESIGN_ID																				
29h	0	0	0	0	SDOUT_TRISTATE_D	0	0	0	0	0	0	0	0	SDOUT_TRISTATE	0	0	0	0	0	0	0	0	0	0

Register Map(continued)

ADDR (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2Ah	LED2VAL																							
2Bh	ALED2VAL\LED3VAL																							
2Ch	LED1VAL																							
2Dh	ALED1VAL																							
2Eh	LED2-ALED2VAL																							
2Fh	LED1-ALED1VAL																							
31h	FILTER_BW(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	PD_DISCONNECT	0	0	0	0	ENABLE_INPUT_SHORT	0	0	0	0	0
34h	0	0	0	0	0	0	0	0	PROG_INT2_STC															
35h	0	0	0	0	0	0	0	0	PROG_INT2_ENDC															
36h	0	0	0	0	0	0	0	0	LED3LEDSTC															
37h	0	0	0	0	0	0	0	0	LED3LEDENDC															
39h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKDIV_TE		
3Ah	0	0	0	EARLY_OFFSET_DAC	POL_OFFDAC_LED2	I_OFFDAC_LED2_MID				POL_OFFDAC_AMB1	I_OFFDAC_LED2_MID				POL_OFFDAC_LED1	I_OFFDAC_LED2_MID				POL_OFFDAC_AMB2\POL_OFFDAC_LED3	I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID			
3Bh	THR_DET_LOW_CODE																							
3Ch	THR_DET_HIGH_CODE																							
3Dh	0	0	0	0	0	WM_MODE	0	0	0	THR_DET_PHASE_SEL<7>	THR_DET_PHASE_SEL<6>	THR_DET_PHASE_SEL<5>	THR_DET_PHASE_SEL<4>	THR_DET_PHASE_SEL<3>	THR_DET_PHASE_SEL<2>	THR_DET_PHASE_SEL<1>	THR_DET_PHASE_SEL<8>	FIFO_EN_DEC	DEC_EN	THR_DET_EN	DEC_FACTOR			THR_DET_PHASE_SEL<0>

Register Map(continued)

ADDR (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3Eh	0	0	0	0	0	0	0	0	0	0	0	0	I_OFFDAC_LED2_LSB_EXT	I_OFFDAC_AMB1_LSB_EXT	I_OFFDAC_LED1_LSB_EXT	I_OFFDAC_LED3_LSB_EXT	I_OFFDAC_LED2_MSB	I_OFFDAC_LED2_LSB	I_OFFDAC_AMB1_MSB	I_OFFDAC_AMB1_LSB	I_OFFDAC_LED1_MSB	I_OFFDAC_LED1_LSB	I_OFFDAC_LED3_MSB	I_OFFDAC_LED3_LSB
3Fh	AVG_LED2-ALED2VAL																							
40h	AVG_LED1-ALED1VAL																							
42h	INT_ MUX3		INT_ MUX2		0	FIFO_EARLY			REG_FIFO_PERIOD/ REG_WM_FIFO										INT_ MUX1	FIFO_PARTITION				
43h	0	0	0	0	0	0	0	0	LED4LEDSTC															
44h	0	0	0	0	0	0	0	0	LED4LEDENDC															
45h	0	0	0	0	0	0	0	0	TG_PD1STC															
46h	0	0	0	0	0	0	0	0	TG_PD1ENDC															
47h	0	0	0	0	0	0	0	0	TG_PD2STC															
48h	0	0	0	0	0	0	0	0	TG_PD2ENDC															
49h	0	0	0	0	0	0	0	0	TG_PD3STC															
4Ah	0	0	0	0	0	0	0	0	TG_PD3ENDC															
4Bh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_PROG_OUT1	0	0	0	0	CONTROL_DYN_VCM	CONTROL_DYN_DLDO	CONTROL_DYN_ALDO	CONTROL_DYN_BG
4Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TRIPLE_PD_ ENABLE	DUAL_PD_ ENABLE	0	0	0
50h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP	0	CONTROL_DYN_TX(1)	0	0	0

Register Map(continued)

ADDR (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
51h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MASK_FIFO_RDY	FORCE_FIFO_ OFFSET	FIFO_OFFSET_TO_FORCE							
52h	0	0	0	0	0	0	0	0	DATA_RDY_STC															
53h	0	0	0	0	0	0	0	0	DATA_RDY_ENDC															
54h	0	0	0	0	0	0	0	0	0	MASK_PPG			0	0	0	MASK1_PPG			MASK2_PPG			MASK3_PPG		
57h	0	0	0	0	0	0	0	0	PROG_INT1_STC															
58h	0	0	0	0	0	0	0	0	PROG_INT1_ENDC															
60h	0	0	0	0	0	0	0	0	0	0	0	0	EN_AMB_LOOP	CHOOSE_AMB_ PHASE	0	0	0	FREEZE_LOOP	HYST_LOOP		0	0	0	
64h	0	0	0	0	0	0	0	0	DYN_TIA_STC															
65h	0	0	0	0	0	0	0	0	DYN_TIA_ENDC															
66h	0	0	0	0	0	0	0	0	DYN_ADC_STC															
67h	0	0	0	0	0	0	0	0	DYN_ADC_ENDC															
68h	0	0	0	0	0	0	0	0	DYN_CLK_STC															
69h	0	0	0	0	0	0	0	0	DYN_CLK_ENDC															
6Ah	0	0	0	0	0	0	0	0	DEEP_SLEEP_STC															
6Bh	0	0	0	0	0	0	0	0	DEEP_SLEEP_ENDC															
6Dh																	REG_POINTER_DIFF							
72h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_DRV2_LED4	EN_DRV2_LED3	EN_DRV2_LED2	EN_DRV2_LED1	DIS_DRV1_LED4	DIS_DRV1_LED3	DIS_DRV1_LED2	DIS_DRV1_LED1

5.5 Register descriptions

Register 0h(address = 0h) [reset = 0h]

Register 00h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	FIFO_EN	ENABLE_ULP	RW_CONT	SW_RESET	0	TM_COUNT_RST	SPI_REG_READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
23-7	0	W	0h	Must write 0
6	FIFO_EN	W	0h	0 = FIFO disabled 1 = FIFO enabled
5	ENABLE_ULP	W	0h	Enables the ULP mode – Must write to '1'. Note that this bit should be programmed prior to programming registers with address 23h or higher.
4	RW_CONT	W	0h	0 = Read or write only one register at a time 1 = Read or write continuously in both I²C and SPI modes
3	SW_RESET	W	0h	Self-clearing reset bit. For a software reset, write 1.
2	0	W	0h	Must write 0
1	TM_COUNT_RST	W	0h	This bit is used to suspend the count and keep the counter in a reset state.
0	SPI_REG_READ	W	0h	Register readout enable for write registers in SPI mode (not needed in I²C mode or for reading ADC output registers or FIFO in SPI mode). 0 = Register write mode in SPI interface mode 1 = Enables the readout of write registers in SPI interface mode Not required for readout of read-only registers with these addresses: 2Ah, 2Bh, 2Ch, 2Dh, 2Eh, 2Fh, 3Fh, 40h, FFh.

Register 01h (address = 01h) [reset = 0h]

Register 01h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2STC	R/W	0h	Determines sample LED2 start

Register 02h (address = 02h) [reset = 0h]

Register 02h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2ENDC	R/W	0h	Determines sample LED2 end

Register 03h (address = 03h) [reset = 0h]

Register 03h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1LEDSTC	R/W	0h	Determines LED1 start

Register 04h (address = 04h) [reset = 0h]

Register 04h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1LEDENDC	R/W	0h	Determines LED1 end

Register 05h (address = 05h) [reset = 0h]

Register 05h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2STC\LED3STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2STC\LED3STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2STC\LED3STC	R/W	0h	Determines sample Ambient2 (or Determines sample LED3) start

Register 06h (address = 06h) [reset = 0h]

Register 06h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2ENDC\LED3ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2ENDC\LED3ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2ENDC\LED3ENDC	R/W	0h	Determines sample Ambient2 (or Determines sample LED3) end

Register 07h (address = 07h) [reset = 0h]

Register 07h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1STC	R/W	0h	Determines sample LED1 start

Register 08h (address = 08h) [reset = 0h]

Register 08h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1ENDC	R/W	0h	Determines sample LED1 end

Register 09h (address = 09h) [reset = 0h]

Register 09h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2LEDSTC	R/W	0h	Determines LED2 start

Register 0Ah (address = 0Ah) [reset = 0h]

Register 0Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2LEDENDC	R/W	0h	Determines LED2 end

Register 0Bh (address = 0Bh) [reset = 0h]

Register 0Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1STC	R/W	0h	Determines sample Ambient1 start

Register 0Ch (address = 0Ch) [reset = 0h]

Register 0Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1ENDC	R/W	0h	Determines sample Ambient1 end

Register 0Dh (address = 0Dh) [reset = 0h]

Register 0Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2CONVST	R/W	0h	Determines LED2 convert phase start

Register 0Eh (address = 0Eh) [reset = 0h]

Register 0Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2CONVEND	R/W	0h	Determines LED2 convert phase end

Register 0Fh (address = 0Fh) [reset = 0h]

Register 0Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVST\LED3CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVST\LED3CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2CONVST\LED3CONVST	R/W	0h	Determines Ambient2 (or LED3) convert phase start

Register 10h (address = 10h) [reset = 0h]

Register 10h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVEND\LED3CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVEND\LED3CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2CONVEND\LED3CONVEND	R/W	0h	Determines Ambient2 (or LED3) convert phase end

Register 11h (address = 11h) [reset = 0h]

Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1CONVST	R/W	0h	Determines LED1 convert phase start

Register 12h (address = 12h) [reset = 0h]

Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1CONVEND	R/W	0h	Determines LED1 convert phase end

Register 13h (address = 13h) [reset = 0h]

Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1CONVST	R/W	0h	Determines Ambient1 convert phase start

Register 14h (address = 14h) [reset = 0h]

Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1CONVEND	R/W	0h	Determines Ambient1 convert phase end

Register 1Dh (address = 1Dh) [reset = 0h]

Register 1Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PRPCT							
R/W-0h							
7	6	5	4	3	2	1	0
PRPCT							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PRPCT	R/W	0h	These bits are the count value for the counter that sets the PRF. The counter automatically counts until PRPCT and then returns back to 0 to start the next count.

Register 1Dh (address = 1Dh) [reset = 0h]

Register 1Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PRPCT							
R/W-0h							
7	6	5	4	3	2	1	0
PRPCT							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PRPCT	R/W	0h	These bits are the count value for the counter that sets the PRF. The counter automatically counts until PRPCT and then returns back to 0 to start the next count.

Register 1Eh (address = 1Eh) [reset = 0h]

Register 1Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	TIMEREN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	NUMAV			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0
8	TIMEREN	R/W	0h	This bit enables the timing engine that can be programmed to generate all clock phases for the synchronized transmit drive, receive sampling, and data conversion. 0 = Timer module disabled 1 = Enables timer module.
7-4	0	W	0h	Must write 0
3-0	NUMAV	R/W	0h	These bits determine the number of ADC averages. By programming a higher ADC conversion time, the ADC can be set to do multiple conversions and average these multiple conversions to achieve lower noise. This programmability is set with the NUMAV bit control. The number of samples that are averaged is represented by the decimal equivalent of NUMAV + 1. For example, NUMAV = 0 represents no averaging, NUMAV = 2 represents averaging of three samples, and NUMAV = 15 represents averaging of 16 samples.

Register 1Fh (address = 1Fh) [reset = 0h]

Register 1Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	TIA_GAIN_SEP3_MSB	TIA_CF_SEP3			TIA_GAIN_SEP3_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
0	TIA_GAIN_SEP2_MSB	TIA_CF_SEP2			TIA_GAIN_SEP2_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 1Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14	TIA_GAIN_SEP3_MSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP3_MSB is the MSB of the R_F control in the Ambient1 phase.
13-11	TIA_CF_SEP3	R/W	0h	When ENSEPGAIN4 = 1, TIA_CF_SEP3 is the C_F control in the Ambient1 phase.
10-8	TIA_GAIN_SEP3_LSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP3_LSB is the three LSBs of the R_F control in the Ambient1 phase.
7	0	W	0h	Must write 0
6	TIA_GAIN_SEP2_MSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP2_MSB is the MSB of the R_F control in the LED3, Ambient2 phase.
5-3	TIA_CF_SEP2	R/W	0h	When ENSEPGAIN4 = 1, TIA_CF_SEP2 is the C_F control in the LED3, Ambient2 phase.
2-0	TIA_GAIN_SEP2_LSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP2_LSB is the three LSBs of the R_F control in the LED3, Ambient2 phase.

Register 20h (address = 20h) [reset = 0h]

Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ENSEPGAIN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	TIA_GAIN_SEP_MSB	TIA_CF_SEP			TIA_GAIN_SEP_LSB		
W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15	ENSEPGAIN	R/W	0h	Mode to enable independently programmable R_F and C_F values for each of two sets of phases (each set having two phases).
14-7	0	W	0h	Must write 0
6	TIA_GAIN_SEP_MSB	R/W	0h	When ENSEPGAIN = 1, TIA_GAIN_SEP_MSB is the MSB of the R_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_GAIN_SEP_MSB is the MSB of the R_F control in the LED2 phase.
5-3	TIA_CF_SEP_LSB	R/W	0h	When ENSEPGAIN = 1, TIA_CF_SEP is the C_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_CF_SEP is the C_F control in the LED2 phase.
2-0	TIA_GAIN_SEP_LSB	R/W	0h	When ENSEPGAIN = 1, TIA_GAIN_SEP_LSB is the three LSBs of the R_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_GAIN_SEP_LSB is the three LSBs of the R_F control in the LED2 phase.

Register 21h (address = 21h) [reset = 0h]

Register 21h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	IFS_OFFDAC			0	0	FILTER_BW(0)	0
W-0h	R/W-0h			W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	TIA_GAIN_MSB	TIA_CF			TIA_GAIN_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14-12	IFS_OFFDAC	R/W	0h	Programs the full-scale current range of the Offset Cancellation DAC.
11-10	0	W	0h	Must write 0
9	FILTER_BW(0)	R/W	0h	Bit D0 controlling the Bandwidth setting of the Noise reduction filter
8-7	0	W	0h	Must write 0
6	TIA_GAIN_MSB	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_GAIN_MSB is the MSB of the R_F control in all four phases. When ENSEPGAIN = 1, TIA_GAIN_MSB is the MSB of the R_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_GAIN_MSB is the MSB of the R_F control in the LED1 phase.
5-3	TIA_CF	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_CF is the C_F control in all four phases. When ENSEPGAIN = 1, TIA_CF is the C_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_CF is the C_F control in the LED1 phase.
2-0	TIA_GAIN_LSB	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_GAIN_LSB is the three LSBs of the R_F control in all four phases. When ENSEPGAIN = 1, TIA_GAIN_LSB is the three LSBs of the R_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_GAIN_LSB is the three LSBs of the R_F control in the LED1 phase.

Register 22h (address = 22h) [reset = 0h]

Register 22h

23	22	21	20	19	18	17	16
ILED3_LSB		ILED2_LSB		ILED1_LSB		ILED3_MSB	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
ILED3_LSB				ILED2_MSB			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ILED2_MSB		ILED1_MSB					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Register 22h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	ILED3_LSB	R/W	0h	Lower two bits (LSBs) of ILED3 (the LED3 current control)
21-20	ILED2_LSB	R/W	0h	Lower two bits (LSBs) of ILED2 (the LED2 current control)
19-18	ILED1_LSB	R/W	0h	Lower two bits (LSBs) of ILED1 (the LED1 current control)
17-12	ILED3_MSB	R/W	0h	Top six bits (MSBs) of ILED3 (the LED3 current control)
11-6	ILED2_MSB	R/W	0h	Top six bits (MSBs) of ILED2 (the LED2 current control)
5-0	ILED1_MSB	R/W	0h	Top six bits (MSBs) of ILED1 (the LED1 current control)

Register 23h (address = 23h) [reset = 0h]

Register 23h

23	22	21	20	19	18	17	16
0	0	0	CONTROL_DYN_TX(0)	0	0	ILED_FS	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	R/W-0h	W-0h
15	14	13	12	11	10	9	8
ENSEPGAIN4	CONTROL_DYN_BIAS	0	0	0	0	OSC_ENABLE	0
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	CONTROL_DYN_TIA	CONTROL_DYN_ADC	0	PDNRX	PDNAFE
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20	CONTROL_DYN_TX(0)	R/W	0h	One of the bits that powers down LED current bias when the device is in Deep Sleep mode. Always write '1'.
19-18	0	W	0h	Must write 0
17	ILED_FS	R/W	0h	Programs the full scale current range of the LED driver.
16	0	W	0h	Must write 0
15	ENSEPGAIN4	R/W	0h	Mode to enable independently programmable R_F and C_F values in each of the four phases.
14	CONTROL_DYN_BIAS	R/W	0h	Powers down the bias for the Offset Cancellation DAC and ADC when the device is in Deep Sleep mode. Always write '1'.
13-10	0	W	0h	Must write 0
9	OSC_ENABLE	R/W	0h	0 = External clock mode (default). In this mode, the CLK pin functions as an input pin where the external clock can be in put. 1 = Enables oscillator mode. In this mode, the 128-kHz internal oscillator is enabled and used by the timing engine.
8-5	0	W	0h	Must write 0
4	CONTROL_DYN_TIA	R/W	0h	Powers down the TIA when the device comes out of Active mode. Always write '1'.
3	CONTROL_DYN_ADC	R/W	0h	Powers down the ADC when the device comes out of Active mode. Always write '1'.
2	0	W	0h	Must write 0
1	PDNRX	R/W	0h	0 = Normal mode 1 = RX portion of the AFE is powered down
0	PDNAFE	R/W	0h	0 = Normal mode 1 = Entire AFE is powered down

Register 24h (address = 24h) [reset = 0h]

Register 24h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	ILED4_MSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
15	14	13	12	11	10	9	8
ILED4_MSB					ILED4_LSB		0
R/W-0h					RW-0h		W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	W	0h	Must write 0
16-11	ILED4_MSB	R/W	0h	Top six bits (MSBs) of ILED4 (the LED4 current control)
10-9	ILED4_LSB	R/W	0h	Lower two bits (LSBs) of ILED4 (the LED4 current control)
8-0	0	W	0h	Must write 0

Register 28h (address = 28h) [reset = 0h]

Register 28h

23	22	21	20	19	18	17	16
x	FIFO_TOGGLE	x	DESIGN_ID				
R/x	R/x	R/x	R/x				
15	14	13	12	11	10	9	8
DESIGN_ID							
R/x							
7	6	5	4	3	2	1	0
DESIGN_ID	x	x	x	x	x	x	x
R/x	R/x	R/x	R/x	R/x	R/x	R/x	R/x

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
23	x	R	x	Read-only (Don't care)
22	FIFO_TOGGLE	R	x	Toggles between 0 and 1 at every FIFO_RDY. The FIFO_TOGGLE register bit can also be brought out on the ADC_RDY pin.
21	x	R	x	Read-only (Don't care)
20-7	DESIGN_ID	R	x	Revision id: Reads 00000001101010.
6-0	x	R	x	Read-only (Don't care)

Register 29h (address = 29h) [reset = 0h]

Register 29h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	SDOUT_ TRISTATE	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	W	0h	Must write 0
19	SDOUT_TRISTATE_D	R/W	0h	Dynamic SDOUT Tristate Mode[1] 0 = SDOUT is not tri-stated 1 = SDOUT is tri-stated only when SEN is high
18-11	0	W	0h	Must write 0
10	SDOUT_TRISTATE	R/W	0h	Static SDOUT Tristate Mode[1] 0 = SDOUT is not tri-stated 1 = SDOUT is tri-stated always (when SEN is high or low)
9-0	0	W	0h	Must write 0

[1] Use this bit control to control the tri-state of the SDOUT line when SDOUT is shared between the SPI interfaces of multiple devices. Note that excessive capacitance on SDOUT can reduce the operating speed of the SPI interface.

Register 2Ah (address = 2Ah) [reset = 0h]

Register 2Ah

23	22	21	20	19	18	17	16
LED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2VAL	R	0h	These bits are the LED2 output code in 24-bit, twos complement format.

Register 2Bh (address = 2Bh) [reset = 0h]

Register 2Bh

23	22	21	20	19	18	17	16
ALED2VAL\LED3VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED2VAL\LED3VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED2VAL\LED3VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED2VAL\LED3VAL	R	0h	These bits are the Ambient2 or LED3 output code in 24-bit, twos complement format.

Register 2Ch (address = 2Ch) [reset = 0h]

Register 2Ch

23	22	21	20	19	18	17	16
LED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1VAL	R	0h	These bits are the LED1 output code in 24-bit, twos complement format.

Register 2Dh (address = 2Dh) [reset = 0h]

Register 2Dh

23	22	21	20	19	18	17	16
ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED1VAL	R	0h	These bits are the Ambient1 output code in 24-bit, Twos complement format.

Register 2Eh (address = 2Eh) [reset = 0h]

Register 2Eh

23	22	21	20	19	18	17	16
LED2-ALED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2-ALED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2-ALED2VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2-ALED2VAL(1)	R	0h	These bits are the (LED2—Ambient2) output code in 2 4-bit, twos complement format.

(1) Ignore the content of this register when LED3 is used.

Register 2Fh (address = 2Fh) [reset = 0h]

Register 2Fh

23	22	21	20	19	18	17	16
LED1-ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1-ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1-ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1-ALED1VAL	R	0h	These bits are the (LED1—Ambient1) output code in 2 4-bit, twos complement format.

Register 2Fh (address = 2Fh) [reset = 0h]

Register 2Fh

23	22	21	20	19	18	17	16
LED1-ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1-ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1-ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1-ALED1VAL	R	0h	These bits are the (LED1—Ambient1) output code in 24-bit, twos complement format.

Register 31h (address = 31h) [reset = 0h]

Register 31h

23	22	21	20	19	18	17	16
FILTER_BW(1)	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	PD_DISCONNECT	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	ENABLE_INPUT_SHORT	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
23	FILTER_BW(1)	R/W	0h	Bit D1 controlling the Bandwidth setting of the Noise reduction filter
22-11	0	W	0h	Must write 0
10	PD_DISCONNECT	R/W	0h	This bit disconnects the PD signals (INP, INM) from the TIA inputs. When enabled, the current input to the TIA is determined completely by the offset cancellation DAC current (I_OFFDAC). Note that in this mode, the AFE no longer sets the bias for the PD.
9-6	0	W	0h	Must write 0
5	ENABLE_INPUT_SHORT	R/W	0h	INP, INN are shorted to VCM whenever the TIA is in power-down.
4-0	0	W	0h	Must write 0

Register 34h (address = 34h) [reset = 0h]

Register 34h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT2_STC							
W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_STC							
W-0h							

LEGEND: W = Write only; -n = value after reset

Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT2_STC	W	0h	Determines spare interrupt 2 start

Register 35h (address = 35h) [reset = 0h]

Register 35h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT2_ENDC							
W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_ENDC							
W-0h							

LEGEND: W = Write only; -n = value after reset

Register 35h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT2_ENDC	W	0h	Determines spare interrupt 2 end

Register 36h (address = 36h) [reset = 0h]

Register 36h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 36h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED3LEDSTC	R/W	0h	Determines LED3 start

Register 37h (address = 37h) [reset = 0h]

Register 37h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED3LEDENDC	R/W	0h	Determines LED3 end

Register 39h (address = 39h) [reset = 0h]

Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	CLKDIV_TE		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	W	0h	Must write 0
2-0	CLKDIV_TE	R/W	0h	Clock division ratio for the clock divider in the path of the input clock (external clock or 128 kHz oscillator clock) to the timing engine.

Register 3Ah (address = 3Ah) [reset = 0h]

Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	EARLY_OFFSET_DAC	POL_OFFDAC_LED2	I_OFFDAC_LED2_MID		
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
I_OFFDAC_LED2_MID	POL_OFFDAC_AMB1	I_OFFDAC_AMB1_MID				POL_OFFDAC_LED1	I_OFFDAC_LED1_MID
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
I_OFFDAC_LED1_MID			POL_OFFDAC_AMB2\ POL_OFFDAC_LED3	I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID			
R/W-0h			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 3Ah Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20	EARLY_OFFSET_DAC	R/W	0h	0 – Offset DAC for a phase transitions at start of SAMP 1- Offset DAC for a phase transitions at start of LED ON
19	POL_OFFDAC_LED2	R/W	0h	Offset cancellation DAC polarity for LED2
18-15	I_OFFDAC_LED2_MID	R/W	0h	Middle four bits of the offset cancellation DAC Setting for LED2
14	POL_OFFDAC_AMB1	R/W	0h	Offset cancellation DAC polarity for Ambient1
13-10	I_OFFDAC_AMB1_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for Ambient1
9	POL_OFFDAC_LED1	R/W	0h	Offset cancellation DAC polarity for LED1
8-5	I_OFFDAC_LED1_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for LED1
4	POL_OFFDAC_AMB2\POL_OFFDAC_LED3	R/W	0h	Offset cancellation DAC polarity for Ambient2 (or LED3)
3-0	I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for Ambient2 (or LED3)

Register 3Bh (address = 3Bh) [reset = 0h]

Register 3Bh

23	22	21	20	19	18	17	16
THR_DET_LOW_CODE							
R/W-0h							
15	14	13	12	11	10	9	8
THR_DET_LOW_CODE							
R/W-0h							
7	6	5	4	3	2	1	0
THR_DET_LOW_CODE							
R/W-0h							

LEGEND: R = Read only; -n = value after reset

Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THR_DET_LOW_CODE	R/W	0h	24-bit code in twos complement format used for setting the low threshold when checking the output code in threshold detect mode.

Register 3Ch (address = 3Ch) [reset = 0h]

Register 3Ch

23	22	21	20	19	18	17	16
THR_DET_HIGH_CODE							
R/W-0h							
15	14	13	12	11	10	9	8
THR_DET_HIGH_CODE							
R/W-0h							
7	6	5	4	3	2	1	0
THR_DET_HIGH_CODE							
R/W-0h							

LEGEND: R = Read only; -n = value after reset

Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THR_DET_HIGH_CODE	R/W	0h	24-bit code in twos complement format used for setting the high threshold when checking the output code in threshold detect mode.

Register 3Dh (address = 3Dh) [reset = 0h]

Register 3Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	WM_MODE	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	THR_DET_ PHASE_SEL<7>	THR_DET_ PHASE_SEL<6>	THR_DET_ PHASE_SEL<5>	THR_DET_ PHASE_SEL<4>	THR_DET_ PHASE_SEL<3>	THR_DET_ PHASE_SEL<2>	THR_DET_ PHASE_SEL<1>
W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
THR_DET_ PHASE_SEL<8>	FIFO_EN_DEC	DEC_EN	THR_DET_EN	DEC_FACTOR			THR_DET_ PHASE_SEL<0>
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 3Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	W	0h	Must write 0
18	WM_MODE	R/W	0h	Enables the 'Watermark FIFO mode' where the FIFO interrupt is generated based on a programmable watermark level
17-15	0	W	0h	Must write 0
14	THR_DET_PHASE_SEL<7>	R/W	0h	Controls priority for the (LED1-AMB2) phase in the threshold detect mode.
13	THR_DET_PHASE_SEL<6>	R/W	0h	Controls priority for the (AMB2-AMB1) phase in the threshold detect mode.
12	THR_DET_PHASE_SEL<5>	R/W	0h	Controls priority for the (LED2-AMB1) phase in the threshold detect mode.
11	THR_DET_PHASE_SEL<4>	R/W	0h	Controls priority for the (AMB1) phase in the threshold detect mode.
10	THR_DET_PHASE_SEL<3>	R/W	0h	Controls priority for the (LED1) phase in the threshold detect mode.
9	THR_DET_PHASE_SEL<2>	R/W	0h	Controls priority for the (AMB2) phase in the threshold detect mode.
8	THR_DET_PHASE_SEL<1>	R/W	0h	Controls priority for the (LED2) phase in the threshold detect mode.
7	THR_DET_PHASE_SEL<8>	R/W	0h	Controls priority for the (LED1-AMB1) phase in the threshold detect mode.
6	FIFO_EN_DEC	R/W	0h	Enables the FIFO in the Decimation mode.
5	DEC_EN	R/W	0h	0 = Decimation mode disabled 1 = Decimation mode enabled
4	THR_DET_EN	R/W	0h	Enable Threshold detect mode
3-1	DEC_FACTOR	R/W	0h	Decimation factor (how many samples are to be averaged);
0	THR_DET_PHASE_SEL<0>	R/W	0h	Controls priority for the (LED2-AMB2) phase in the threshold detect mode.

Register 3Eh (address = 3Eh) [reset = 0h]

Register 3Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	I_OFFDAC_ LED2_LSB_EXT	I_OFFDAC_ AMB1_LSB_EXT	I_OFFDAC_ LED1_LSB_EXT	I_OFFDAC_ LED3_LSB_EXT
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
I_OFFDAC_ LED2_MSB	I_OFFDAC_ LED2_LSB	I_OFFDAC_ AMB1_MSB	I_OFFDAC_ AMB1_LSB	I_OFFDAC_ LED1_MSB	I_OFFDAC_ LED1_LSB	I_OFFDAC_ LED3_MSB	I_OFFDAC_ LED3_LSB
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 3Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-12	0	W	0h	Must write 0
11	I_OFFDAC_LED2_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED2
10	I_OFFDAC_AMB1_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for AMB1
9	I_OFFDAC_LED1_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED1
8	I_OFFDAC_LED3_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED3
7	I_OFFDAC_LED2_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED2
6	I_OFFDAC_LED2_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED2
5	I_OFFDAC_AMB1_MSB	R/W	0h	MSB of the offset cancellation DAC setting for Ambient1
4	I_OFFDAC_AMB1_LSB	R/W	0h	LSB of the offset cancellation DAC setting for Ambient1
3	I_OFFDAC_LED1_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED1
2	I_OFFDAC_LED1_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED1
1	I_OFFDAC_LED3_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED3
0	I_OFFDAC_LED3_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED3

Register 3Fh (address = 3Fh) [reset = 0h]

Register 3Fh

23	22	21	20	19	18	17	16
AVG_LED2-ALED2VAL							
R-0h							
15	14	13	12	11	10	9	8
AVG_LED2-ALED2VAL							
R-0h							
7	6	5	4	3	2	1	0
AVG_LED2-ALED2VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 3Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AVG_LED2-ALED2VAL	R	0h	These bits are the 24-bit averaged output code for (LED2—Ambient2) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

Register 40h (address = 40h) [reset = 0h]

Register 40h

23	22	21	20	19	18	17	16
AVG_LED1-ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
AVG_LED1-ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
AVG_LED1-ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Register 40h Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AVG_LED1-ALED1VAL	R	0h	These bits are the 24-bit averaged output code for (LED1—Ambient1) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

Register 42h (address = 42h) [reset = 0h]

Register 42h

23	22	21	20	19	18	17	16
INT_MUX3		INT_MUX2		0	FIFO_EARLY		
R/W-0h		R/W-0h		W-0h	R/W-0h		
15	14	13	12	11	10	9	8
FIFO_EARLY		REG_FIFO_PERIOD/REG_WM_FIFO					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
REG_FIFO_PERIOD		INT_MUX1		FIFO_PARTITION			
R/W-0h		R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	INT_MUX3	R/W	0h	Selection for interrupt multiplexing on the SDOUT pin (only available in I²C interface mode).
21-20	INT_MUX2	R/W	0h	Selection for interrupt multiplexing on the PROG_OUT1 pin (available in both I²C and SPI interface modes).
19	0	W	0h	Must write 0
18-14	FIFO_EARLY	R/W	0h	Advances the generation of the FIFO_RDY interrupt start by a number of periods equal to the decimal equivalent of FIFO_EARLY.
13-6	REG_FIFO_PERIOD/ REG_WM_FIFO	R/W	0h	**Normal FIFO mode:** The decimal value of FIFO_PERIOD (periodicity of the FIFO write cycle) is set by (REG_FIFO_PERIOD +1). **Watermark FIFO mode**: Watermark level as set by (REG_WM_FIFO+1) determines the difference between Write and Read pointer at which a FIFO_RDY interrupt is generated. The interrupt is an indication to the MCU that (REG_WM_FIFO+1) are waiting to be read out.
5-4	INT_MUX1	R/W	0h	Selection for interrupt multiplexing on the ADC_RDY pin.
3-0	FIFO_PARTITION	R/W	0h	Partitioning of the FIFO depth across the different phases of data.

Register 43h (address = 43h) [reset = 0h]

Register 43h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED4LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED4LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED4LEDSTC	R/W	0h	Determines LED4 start. Note that LED4 does not physically exist and this signal is only used to define the gain transition point if ENSEPGAIN4 = 1; a separate R_F and C_F control is needed between the LED1 and Ambient1 phases.

Register 44h (address = 44h) [reset = 0h]

Register 44h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED4LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED4LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED4LEDENDC	R/W	0h	Determines LED4 end. Note that LED4 does not physically exist and this signal is only used to define the gain transition point if ENSEPGAIN4 = 1; a separate R_F and C_F control is needed between the LED1 and Ambient1 phases.

Register 45h (address = 45h) [reset = 0h]

Register 45h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD1STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD1STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 45h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD1STC	R/W	0h	Determines TG_PD1 start count. Must be defined if DUAL_PD_ENABLE is set to 1.

Register 46h (address = 46h) [reset = 0h]

Register 46h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD1ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 46h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD1ENDC	R/W	0h	Determines TG_PD1 end count. Must be defined if DUAL_PD_ENABLE is set to 1.

Register 47h (address = 47h) [reset = 0h]

Register 47h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD2STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD2STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 47h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD2STC	R/W	0h	Determines TG_PD2 start count. Must be defined if DUAL_PD_ENABLE is set to 1.

Register 48h (address = 48h) [reset = 0h]

Register 48h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD2ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD2ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 48h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD2ENDC	R/W	0h	Determines TG_PD2 end count. Must be defined if DUAL_PD_ENABLE is set to 1.

Register 49h (address = 49h) [reset = 0h]

Register 49h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD3STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD3STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 49h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD3STC	R/W	0h	Determines TG_PD3 start count. Must be defined if the PD3 is to be used.

Register 4Ah (address = 4Ah) [reset = 0h]

Register 4Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD3ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD3ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 4Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD3ENDC	R/W	0h	Determines TG_PD3 end count. Must be defined if the PD3 is to be used.

Register 4Bh (address = 4Bh) [reset = 0h]

Register 4Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	EN_PROG_OUT1
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	CONTROL_DYN_VCM	CONTROL_DYN_DLDO	CONTROL_DYN_ALDO	CONTROL_DYN_BG
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0
8	EN_PROG_OUT1	R/W-0h	0h	This bit enables the PROG_OUT1 to become an output pin where interrupts can be made to come out on.
7-4	0	W	0h	Must write 0
3	CONTROL_DYN_VCM	R/W-0h	0h	Powers down the VCM buffer used to set the DC bias at the input pins and inside the ADC when the device is in Deep Sleep mode.
2	CONTROL_DYN_DLDO	R/W-0h	0h	When operating with the internal LDOs enabled, this bit puts the Digital LDO in a low power state when the device is in Deep Sleep mode.
1	CONTROL_DYN_ALDO	R/W-0h	0h	When operating with the internal LDOs enabled, this bit powers down the Analog LDO (and tristates its output) when the device is in Deep Sleep mode. If this bit is set to '1', then the output of the Analog LDO in Deep sleep mode should be shorted to the output of the Digital LDO using the register control SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP
0	CONTROL_DYN_BG	R/W-0h	0h	Powers down the Bandgap and reference circuits when the device is in Deep Sleep mode.

Register 4Eh (address = 4Eh) [reset = 0h]

Register 4Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	TRIPLE_PD_ENABLE	DUAL_PD_ENABLE	0	0	0
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-5	0	W	0h	Must write 0
4	TRIPLE_PD_ENABLE	R/W-0h	0h	This bit enables Triple PD mode.
3	DUAL_PD_ENABLE	R/W-0h	0h	This bit enables dual PD mode.
2-0	0	W	0h	Must write 0

Register 50h (address = 50h) [reset = 0h]

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	SHORT_ALDO_TO_DLDO_IN_ DEEP_SLEEP	0	CONTROL_DYN_TX(1)	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
23-6	0	W	0h	Must write 0
5	SHORT_ALDO_TO_DLDO_IN_ DEEP_SLEEP	R/W	0h	Shorts the output of the Analog LDO to the output of the Digital LDO when in Deep Sleep mode.
4	0	W	0h	Must write 0
3	CONTROL_DYN_TX(1)	R/W	0h	Second bit that powers down LED current bias when the device is in Deep Sleep mode. Always write '1'.
2-1	0	W	0h	Must write 0

Register 51h (address = 51h) [reset = 0h]

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	MASK_FIFO_ RDY	FORCE_FIFO_ OFFSET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
FIFO_OFFSET_TO_FORCE							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 51h Field Descriptions

Bit	Field	Type	Reset	Description
23-10	0	W	0h	Must write 0
9	MASK_FIFO_RDY	R/W	0h	Masks the FIFO_RDY interrupt generation when operating in the Watermark FIFO mode.
8	FORCE_FIFO_OFFSET	R/W	0h	Force the read offset address part of the FIFO read p ointer. The read offset address to force is set by FIFO_OFFSET_TO_FORCE.
7-0	FIFO_OFFSET_TO_FORCE	R/W	0h	8-bit number whose decimal equivalent determines t he read offset address part of the FIFO read pointer. Use in conjunction with FORCE_FIFO_OFFSET set to 1.

Register 52h (address = 52h) [reset = 0h]

Register 52h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DATA_RDY_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DATA_RDY_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DATA_RDY_STC	R/W	0h	Determines the start count for DATA_RDY, also determines the start count for FIFO_RDY and THR_DET_EN.

Register 53h (address = 53h) [reset = 0h]

Register 53h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DATA_RDY_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DATA_RDY_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DATA_RDY_ENDC	R/W	0h	Determines the end count for DATA_RDY, also determines the end count for FIFO_RDY and THR_DET_EN.

Register 54h (address = 54h) [reset = 0h]

Register 54h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	MASK_PPG			0	0	0	MASK1_PPG
W-0h	R/W-0h			W-0h	W-0h	W-0h	
7	6	5	4	3	2	1	0
MASK1_PPG		MASK2_PPG			MASK3_PPG		
R/W-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 54h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14-12	MASK_PPG	R/W	0h	Determines the sampling rate (relative to the PRF) for the PPG signal acquisition
11-9	0	W	0h	Must write 0
8-6	MASK1_PPG	R/W	0h	Write same value as the value for MASK_PPG
5-3	MASK2_PPG	R/W	0h	Write same value as the value for MASK_PPG
2-0	MASK3_PPG	R/W	0h	Write same value as the value for MASK_PPG

Register 57h (address = 57h) [reset = 0h]

Register 57h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT1_STC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT1_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 57h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT1_STC	R/W	0h	Determines spare interrupt 1 start

Register 58h (address = 58h) [reset = 0h]

Register 58h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT1_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT1_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 58h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT1_ENDC	R/W	0h	Determines spare interrupt 1 end

Register 60h (address = 60h) [reset = 0h]

Register 60h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	EN_AMB_LOOP	CHOOSE_AMB_PHASE		0
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		W-0h
7	6	5	4	3	2	1	0
0	0	FREEZE_LOOP	HYST_LOOP		0	0	0
W-0h	W-0h	R/W-0h	R/W-0h		W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 60h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	W	0h	Must write 0
11	EN_AMB_LOOP	R/W	0h	Enables the Automatic Ambient Cancellation loop
10-9	CHOOSE_AMB_PHASE	R/W	0h	Chooses which of the 4 phases are used by the Automatic Ambient Cancellation loop to detect and cancel the ambient current
8-6	0	W	0h	Must write 0
5	FREEZE_LOOP	R/W	0h	Freezes the state of the Automatic Ambient Cancellation loop and retains/ applies the last value of the Ambient cancellation portion of the Offset DAC (IA)
4-3	HYST_LOOP	R/W	0h	Programs the hysteresis thresholds (in terms of output voltage) used by the Automatic Ambient Cancellation loop to trigger its re- convergence.
2-0	0	W	0h	Must write 0

Register 64h (address = 64h) [reset = 0h]

Register 64h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_TIA_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_TIA_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 64h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_TIA_STC	R/W	0h	Determines the start of the active phase of the TIA coi nciding with the start of the device Active Phase

Register 65h (address = 65h) [reset = 0h]

Register 65h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_TIA_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_TIA_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 65h Field Descriptions

Bit`	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_TIA_ENDC	R/W	0h	Determines the end of the active phase of the TIA coinciding with the end of the device Active phase

Register 66h (address = 66h) [reset = 0h]

Register 66h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_ADC_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_ADC_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 66h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_ADC_STC	R/W	0h	Determines the start of the active phase of the ADC coinciding with the start of the device Active phase

Register 67h (address = 67h) [reset = 0h]

Register 67h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_ADC_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_ADC_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 67h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_ADC_ENDC	R/W	0h	Determines the end of the active phase of the ADC coinciding with the end of the device Active Phase

Register 68h (address = 68h) [reset = 0h]

Register 68h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_CLK_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_CLK_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 68h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_CLK_STC	R/W	0h	Determines the start of the active phase of the 4 MHz oscillator used for ADC conversion. Coincides with the start of the device Active phase

Register 69h (address = 69h) [reset = 0h]

Register 69h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_CLK_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_CLK_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 69h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_CLK_ENDC	R/W	0h	Determines the end of the active phase of the 4 MHz oscillator used for ADC conversion. Coincides with the end of the device Active phase

Register 6Ah (address = 6Ah) [reset = 0h]

Register 6Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DEEP_SLEEP_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DEEP_SLEEP_STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 6Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DEEP_SLEEP_STC	R/W	0h	Determines the start of the Deep sleep phase.

Register 6Bh (address = 6Bh) [reset = 0h]

Register 6Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DEEP_SLEEP_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DEEP_SLEEP_ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 6Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DEEP_SLEEP_ENDC	R/W	0h	Determines the end of the Deep sleep phase.

Register 6Dh (address = 6Dh) [reset = 0h]

Register 6Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
REG_POINTER_DIFF							
R							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 6Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-8	x	R	x	Read-only (Don't care)
7-0	REG_POINTER_DIFF	R/W	x	The instantaneous value of the (Write pointer *minus* Read pointer) *minus* 1 is stored in REG_POINTER_DIFF. When a FIFO_RDY interrupt is issued, the value stored in REG_POINTER_DIFF is expected to be equal to the value programmed in REG_WM_FIFO.

Register 72h (address = 72h) [reset = 0h]

Register 72h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
EN_DRV2_	EN_DRV2_	EN_DRV2_	EN_DRV2_	DIS_DRV1_	DIS_DRV1_	DIS_DRV1_	DIS_DRV1_
LED4	LED3	LED1	LED1	LED4	LED3	LED2	LED1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

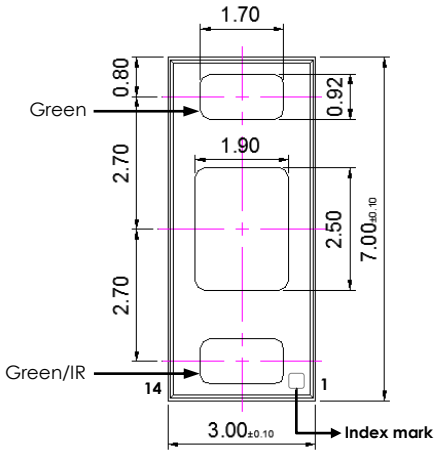
LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Register 72h Field Descriptions

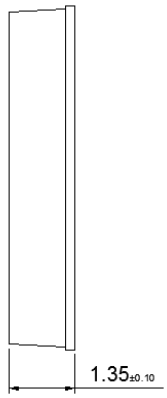
Bit	Field	Type	Reset	Description
23-8	0	W	0h	Must write 0
7	EN_DRV2_LED4	R/W	0h	Enables Driver 1 controls for LED4
6	EN_DRV2_LED3	R/W	0h	Enables Driver 1 controls for LED3
5	EN_DRV2_LED2	R/W	0h	Enables Driver 1 controls for LED2
4	EN_DRV2_LED1	R/W	0h	Enables Driver 1 controls for LED1
3	DIS_DRV1_LED4	R/W	0h	Disables Driver 2 controls for LED4
2	DIS_DRV1_LED3	R/W	0h	Disables Driver 2 controls for LED3
1	DIS_DRV1_LED2	R/W	0h	Disables Driver 2 controls for LED2
0	DIS_DRV1_LED1	R/W	0h	Disables Driver 2 controls for LED1

6. Mechanical Design

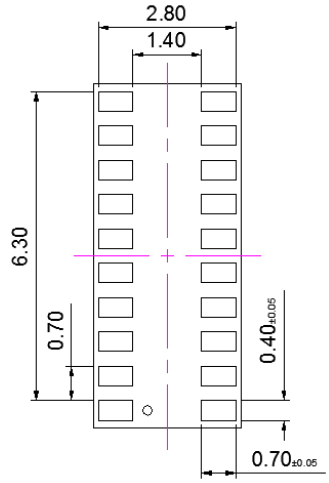
6.1 Mechanical data(unit : mm)



Top View



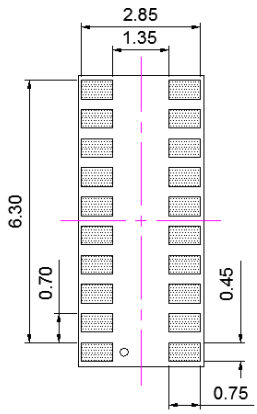
Side View



Bottom View

Pin No.	Function	Pin No.	Function
1	NC	11	TX_SUP
2	NC	12	ADC_RDY
3	BG	13	SEN
4	NC	14	PROG_OUT
5	RX_SUP	15	GND
6	RESETZ	16	IO_SUP
7	CLK	17	NC
8	SDA	18	Control1
9	SDOUT	19	I2C_SPI_SEL
10	SCL	20	NC

6.2 PCB Layout Footprint (unit : mm)



7. Application and Implementation

7.1 Application Information

The PPSI262 is designed to operate with a minimal number of external components. A reset (hardware or software reset) is essential after power-up to ensure that all registers are reset to their default values.
The PPSI262 can be driven with an external clock. The photodiode outputs are prone to picking up noise. Especially when operating in coexistence and close proximity with RF communication circuitry
[such as Bluetooth® low energy (BLE)], a common-mode choke can be used in the path of the device inputs to reject the RF interference.

7.2 Typical Application

Figure 43, 44 shows the typical connection of PPSI262. The following points are to be noted:

1. Use decoupling capacitors (1 uF or higher) placed close to the PPSI262 to filter the noise on RX_SUP and TX_SUP.
2. Use decoupling capacitors (0.1 uF) placed close to the PPSI262 to improve the AFE noise on BG
3. The voltage level used for IO_SUP should be the same as I/O voltage level for the MCU.
4. The pull up resistors of two line serial bus are recommended to be 2.2 KΩ
5. When in power-down mode (PWDN) the external CLK can be shut off to avoid any switching current. Also CONTROL1 should be pulled to '0'.

1) External clock mode

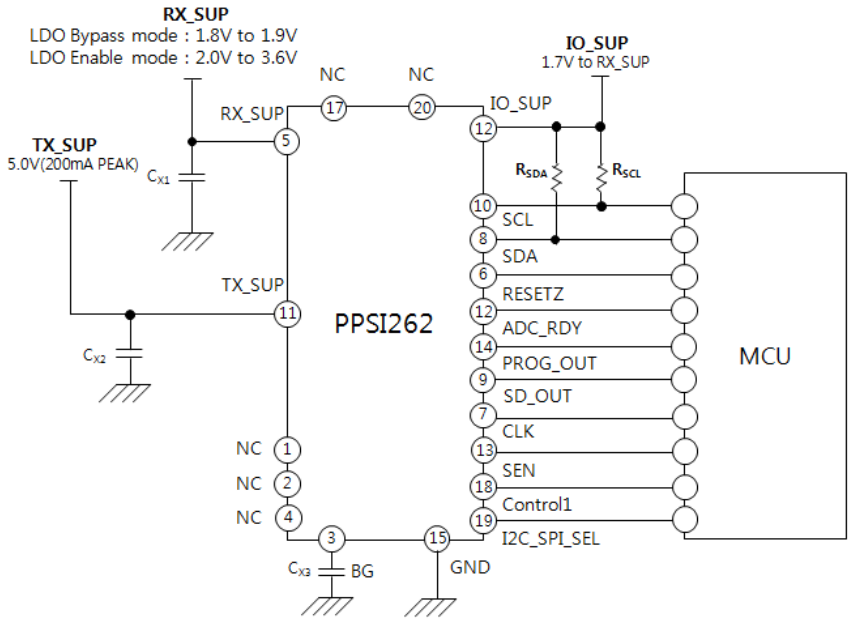


Figure 43. Hardware pin connection diagram in external clock mode

2) Internal oscillator mode

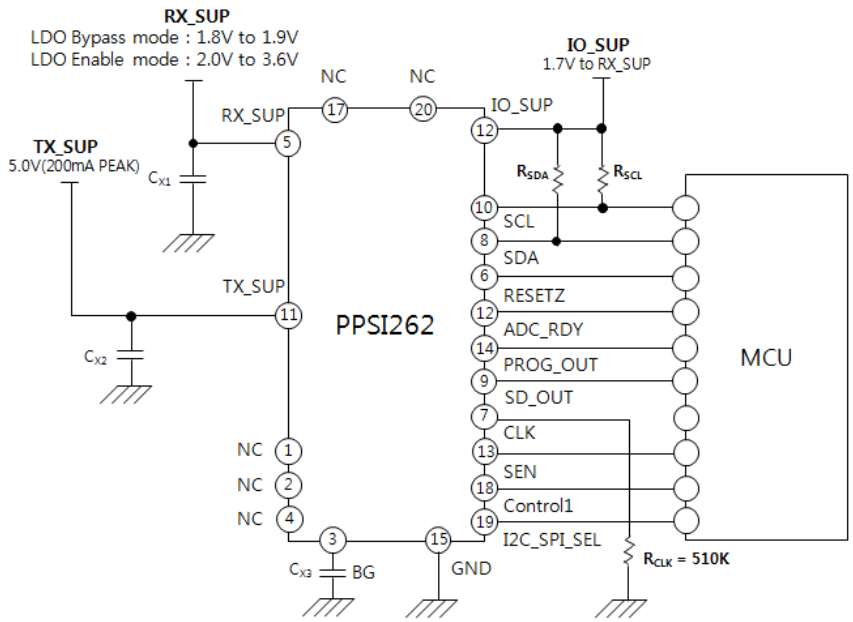


Figure 44. Hardware pin connection diagram in internal oscillator mode

7.3 Detailed design procedure

7.3.1 choosing the correct AFE settings

The AFE signal chain offers several knobs that can be adjusted to achieve the SNR requirements needed for high-end, clinical, pulse-oximeter applications as well as for the low-power demands of battery-operated, optical, heart- rate monitoring applications. The knobs include TIA gain (RF), TIA bandwidth, LED current (ILED), offset cancellation DAC (I_OFFDAC), and Bandwidth setting of the Noise reduction filter (f_{RC}). A calibration algorithm is recommended to be run at startup and also periodically on the MCU to monitor the dc level at the output of the AFE and to adjust the AFE signal chain settings to get close to the target dc level. The optimum gain and LED current depends on the current transfer ratio (CTR) from the LED to the photodiode and the perfusion index at the ADC output (the ac-to-dc ratio of the signal).

For clinical SPO2 applications demanding the highest SNR, where power may not be a primary concern, the LED and sampling pulse durations are recommended to be set to greater than 200 µs. To simplify system design, keeping the pulse duration fixed across use cases is easiest. Set the LED current to the highest value that can be afforded by the system power budget. Initialize the TIA gain to the lowest gain setting of 10 kΩ and use the initial calibration routine to determine the optimum gain. Set the ADC in averaging mode with the number of averages being the maximum afforded by the choice of pulse repetition period and pulse duration. Eight ADC averages is usually sufficient to obtain good SNR.

For power-critical, battery-operated applications, choose a sampling pulse duration between 50 µs to 100 µs and operate the device at a high TIA gain setting (for example, 1 MΩ). Set the ADC in averaging mode with four to eight averages. Initialize the LED current to the desired lowest setting (of a few milliamps) and use the initial calibration routine to determine the optimum LED current setting up to the highest value allowed by the system power budget. While operating with very low LED/sampling pulse widths, it must be kept in mind that the effective signal bandwidth due to the switched RC filter is determined by the product of its physical R-C bandwidth and the sampling duty cycle. It is recommended to operate with a signal bandwidth that is at least twice the largest frequency content expected in the signal.

For pulse-oximeter applications using red and IR LEDs, the target dc level can be typically set to 50% of positive full-scale.

For HRM applications, the offset cancellation DAC can be additionally used such that the dc offset can be subtracted from the signal, thereby allowing for a larger TIA gain to be applied without saturating the signal.

The calibration routine must be designed in a manner that does not rely on the accuracy of the LED current, TIA gain, and offset cancellation DAC, thus allowing for device-to-device variations. Specifically, the offset cancellation DAC is not trimmed at production and can have a significant device-to-device variation (±20%). If the calibration routine requires an accurate estimate of the offset cancellation DAC, then the PD_DISCONNECT mode can be used to estimate the offset cancellation DAC range on a given unit. The PD_DISCONNECT mode disconnects the photodiode from the TIA inputs. In this mode IPD = 0 and, thus, the effective input current to the TIA comes solely from the offset cancellation DAC (I_{eff} = I_OFFDAC). As a result, the offset cancellation DAC value can be directly estimated from the AFE output code.

When the calibration loop is in the process of converging to the steady state, the device settings can continue to be refreshed to new values. Ideally, a time equal to $t_{CHANNEL}$ is provided for the AFE to settle to any change in signal- chain settings. However, this time can lead to unacceptably large delays in the convergence of the calibration routine. Therefore, during the transient (when the calibration routine is in the transient phase), the wait times can be reduced to as low as $t_{CHANNEL}$ / 10. After the calibration routine converges to the final settings, a wait time of $t_{CHANNEL}$ can then be applied before high-accuracy data are read out from the AFE. Another method to speed up the settling of the channel is to temporarily set the sampling pulse-widths to a higher value and open up the bandwidth of the switched RC filter to a higher value.

There may be cases where data from only one or two out of the four phases are required. Even in such cases, the calibration loop is recommended to monitor the device output even for the unused phases and adjust the TIA gain and LED current so that the output does not saturate. The reason for such is that whenever the TIA output saturates, the TIA amplifier no longer effectively sets the bias of the PD. Thus, if the TIA output saturates in one of the phases, then there can be additional unwanted settling times for the PD bias to recover when the saturation is removed.

7.3.2 Operation with 1, 2, or 3 LEDs

Up to three LEDs can be turned on sequentially within a pulse repetition period. Using all three LEDs leaves a common ambient phase that can be subtracted from each of the three LED signals. For the subtraction to be effective, the TIA settings must be the same between each of the LED phases and the ambient phase.

Figure 45 shows the LED ON and sample signals for the case of three LEDs and one Ambient phase.

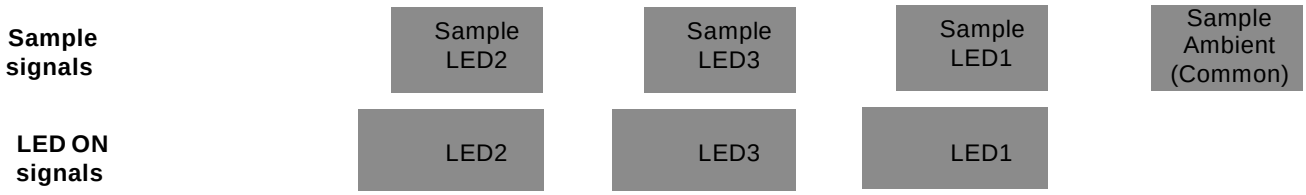


Figure 45. Use Case with Three LEDs and One Ambient Phase

If two LED phases are used, then the remaining two phases can be used as ambient phases. The gain settings for the L ED and the corresponding ambient must be set to the same value. However, the gain settings for LED1, Ambient1 can be set differently from LED2, Ambient2 by setting ENSEPGAIN = 1. Figure 46 details this case.

Figure 46. Use Case with Two LEDs and Two Ambient Phases

If only one LED phase is required, then one of the other phases can be used as an Ambient phase and the other two phases can be blanked out. Use a common TIA setting (default, ENSEPGAIN = 0, ENSEPGAIN4 = 0). Figure 47 shows the case with one LED and one Ambient phase.

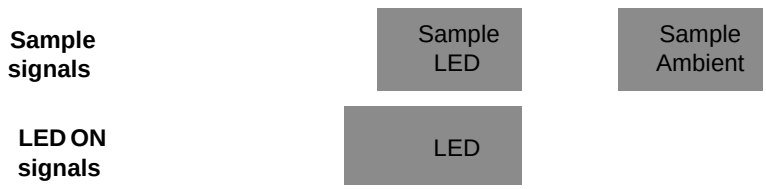


Figure 47. Use Case with One LED and One Ambient Phase

When operating with a timing scheme that is different from the one described in Figure 45, follow these guidelines:

1. If a particular LED or Ambient phase is not required, then the timing signals (LED ON, sampling, ADC conversion) corresponding to the unused phase are recommended to be blanked out by setting their start and end counts to a value greater than PRPCT.
2. If the sequence of the phases is altered with respect to what is described in Figure 45, then a common R_F, C_F settin g (ENSEPGAIN = 0, ENSEPGAIN4 = 0) is recommended to be kept across the four phases to avoid complication. The contents of the output registers must be reinterpreted in the manner described in Table 42. Note that if some of the conversion phases are blanked out, then the corresponding registers do not hold any relevant content.
3. If the sequence of LED ON signals is different from the one shown in Figure 45 and if separate Gain and Cf controls are needed in each phase, then follow guidelines in Section 7.3.3.

REGISTER	CONTENT
2Ah	ADC output corresponding to the 1st CONV phase
2Bh	ADC output corresponding to the 2nd CONV phase
2Ch	ADC output corresponding to the 3rd CONV phase
2Dh	ADC output corresponding to the 4th CONV phase
2Eh	ADC output corresponding to the difference of the 1st and 2nd CONV phases
2Fh	ADC output corresponding to the difference of the 3rd and 4th CONV phases
3Fh	Averaged output in decimation mode corresponding to the difference of the 1st and 2nd CONV phases
40h	Averaged output in decimation mode corresponding to the difference of the 3rd and 4th CONV phases

Table 42. Generalized Content of the Output Registers

4. The FIFO_PARTITION for a generalized timing scheme is shown in Table 43.

FIFO_PARTITION	PHASE1	PHASE2	PHASE3	PHASE4	PHASE5	PHASE6
0000	1st CONV	2nd CONV	3rd CONV	4th CONV	—	—
0001	(3rd—4th CONV)	—	—	—	—	—
0010	3rd CONV	4th CONV	—	—	—	—
0011	(1st—2nd CONV)	—	—	—	—	—
0100	1st CONV	2nd CONV	—	—	—	—
0101	(1st—2nd CONV)	(3rd—4th CONV)	—	—	—	—
0110	(3rd—4th CONV)	(1st—4th CONV)	(2nd—4th CONV)	-	-	-
0111	1st CONV	2nd CONV	(1st—2nd CONV)	3rd CONV	4th CONV	(3rd—4th CONV)
1000	Average (all 4 CONVs)	—	—	—	—	—
Other settings	Do not use	Do not use	Do not use	Do not use	Do not use	Do not use

Table 43. FIFO Partitioning Based on Conversion Order

7.3.3 Setting separate Rf, Cf when the sequence of SAMP is changed

The transition of Rf and Cf across the 4 LED phases are implemented using an internal state machine that maps two btis D1, D0 to the 4 settings as shown in Table 44.

D1	D0	Gain applied	Cf used
0	0	TIA_GAIN_SEP	TIA_CF_SEP
0	1	TIA_GAIN_SEP2	TIA_CF_SEP2
1	0	TIA_GAIN	TIA_CF
1	1	TIA_GAIN_SEP3	TIA_CF_SEP3

Table 44. Mapping of bits D1, D0 to the 4 TIA settings

The bits D1 and D0 transition as per the logic in Table 45.

Edge	D1	D0
LED2 ON rising edge	Force to 0 (F0)	Force to 0 (F0)
LED3 ON rising edge	No change (NC)	Force to 1 (F1)
LED1 ON rising edge	Force to 1 (F1)	Force to 0 (F0)
LED4 ON rising edge	No change (NC)	Force to 1 (F1)

Table 45. Mapping of bits D1, D0 to the 4 TIA settings

The logic in Table 44 and Table 45 applied to the standard sequence of the LED ON signals is shown in Table 46.

Sequence	D1 state	D0 state	D1,D0	Gain	Cf
LED2 ON	F0	F0	00	TIA_GAIN_SEP	TIA_CF_SEP
LED3 ON	NC	F1	01	TIA_GAIN_SEP2	TIA_CF_SEP2
LED1 ON	F1	F0	10	TIA_GAIN	TIA_CF
LED4 ON (Amb)	NC	F1	11	TIA_GAIN_SEP3	TIA_CF_SEP3

Table 46. Gain, Cf transitions for the standard sequence of LED ON signals

The method shown in Table 50 can be used to deduce the Gain and Cf applied for each phase if the LED_ON sequence is changed from the standard sequence.

7.3.4 Reducing Sensitivity to Ambient Light Modulation

Because ambient light is incident on the photodiode in a manner similar to the light originating from the LED, the ambient light has an additive effect to the LED phase output of the AFE. Any artefacts in the ambient light can therefore interfere with the extraction of the heart rate from the signal in the LED phase. The purpose of subtracting the ambient phase signal from the LED phase signal is to remove this effect. The effect of low frequency ambient light is rejected by subtracting the Ambient phase data from the LED phase data.

If the effect of ambient light on the LED and ambient phase outputs is unequal, then subtraction of ambient data from LED data gives only an incomplete cancellation of the ambient light modulation effect. In that case, a periodic pattern in the ambient light can cause spurious tones to appear in the (LED minus Ambient) data. The start of LED ON to start of SAMP (tLED_SAMP) plays a role in the sensitivity to ambient light modulation. Also, the TIA maintains the photodiode bias through a negative feedback. If the TIA output saturates, then the photodiode bias is disturbed. The associated transient for the photodiode bias to get restored can increase the sensitivity to ambient light modulation. For example, in the timing scheme described in Figure 45, a saturation of the TIA during LED3 phase can lead to the TIA recovery response to span both the LED1 and Ambient1 phases. Such transient recovery can cause the channel response to differ between these two phases, thereby rendering ambient subtraction through ambient subtraction to be incomplete. Therefore, the output of every phase is recommended to be prevented from saturating (through periodic signal monitoring and gain adjustment) even if data from that phase is not being used by the heart-rate estimation algorithm.
If the ambient light changes at a fast rate, the effective ambient signal during the LED and Ambient phases can be different because of the difference between the sampling instants. This difference also can cause the ambient subtraction to be incomplete. Reducing the spacing between the sampling instants of the LED and Ambient phases can reduce this effect.

Figure 48 shows the modulation in ambient light common to both LED and Ambient phases. Ideal ambient cancellation requires the (LED minus Ambient) to completely reject the modulation. Figure 49 shows (LED minus Ambient) when the AFE settings are not optimal. Figure 50 shows (LED minus Ambient) for optimalsettings.

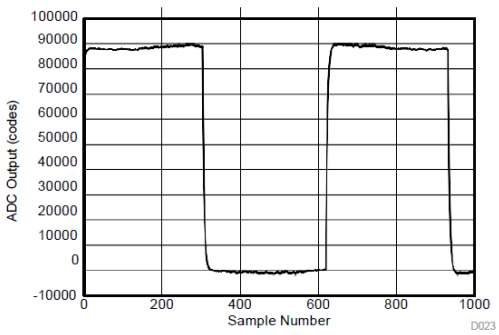


Figure 48. Ambient data with ambient light modulation

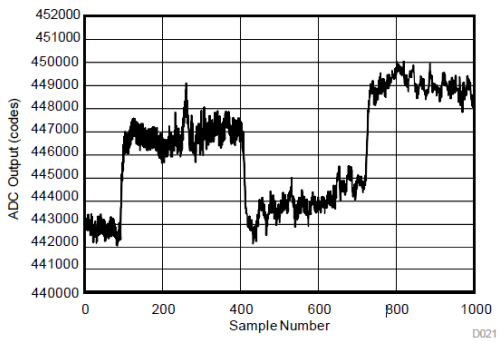


Figure 49. (LED-Ambient) data with Non-Optimal AFE setting

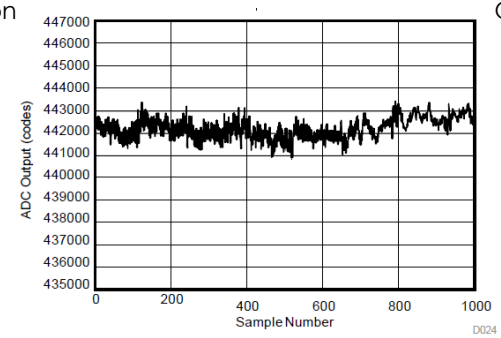


Figure 50. (LED-Ambient) data with Optimal AFE setting

7.3.5 Sampling width considerations

There are multiple factors that govern the choice of the sampling width (SAMP signal) and LED ON time. Figure 51 shows the TIA settling behavior during the LED and SAMP phases. The TIA is shown to be the superposition of two components:

- o $V(TIA_{LED})$ which is the settling of the TIA to the current signal from the PD due to the LED turning on
- o $V(TIA_{OFFSET\_DAC})$ which is the settling of the TIA to the transition in the Offset DAC

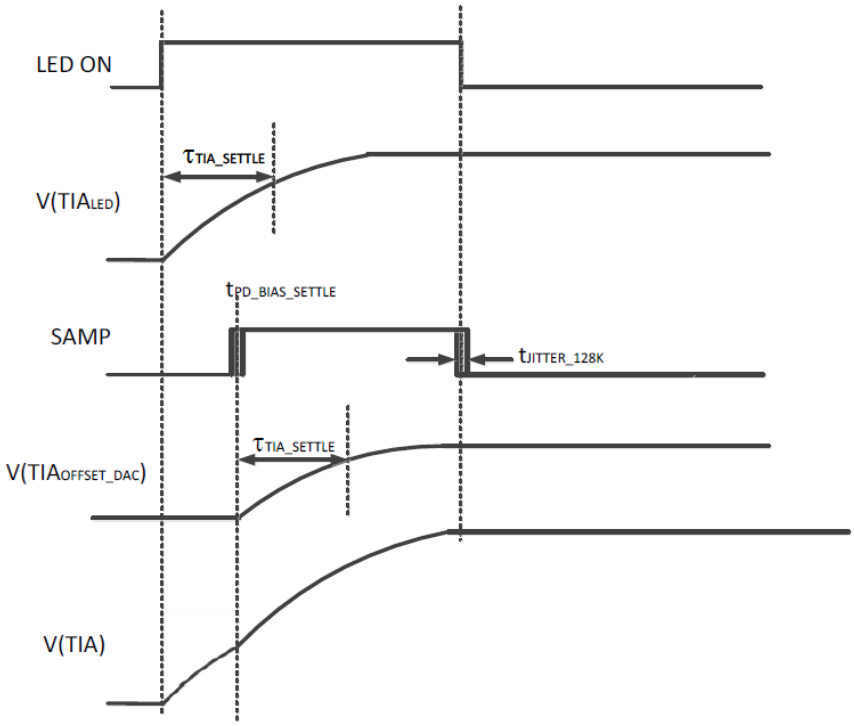


Figure 51. TIA settling transient

To speed up the TIA settling when there is a transition in the Offset DAC setting across phases, it is recommended to set the register bit EARLY_OFFSET_DAC. This bit causes the Offset DAC transition to start at the start of the LED ON signal instead of at the start of the SAMP signal and results in a faster transient as shown in Figure 52.

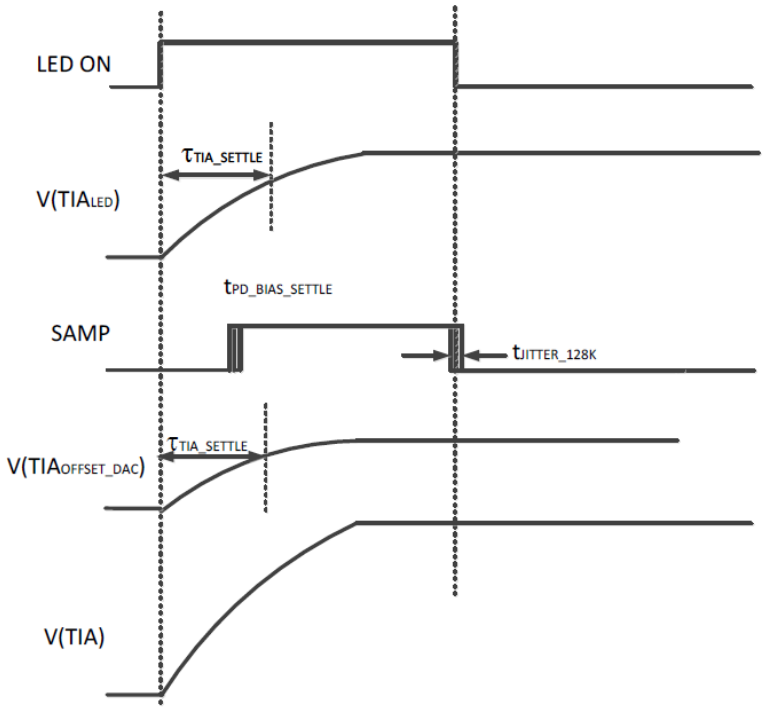


Figure 52. TIA settling transient with EARLY_OFFSET_DAC set to '1'

With the EARLY_OFFSET_DAC set to '1' (Recommended), the considerations for determining the LED and SAMP width are as follows:

- The TIA time constant (t_{TIA_SETTLE})is given by the product of R_F and C_F
- The Noise reduction filter is connected to the TIA output in the SAMP phase. Ideally, the noise reduction filter should be connected to the TIA output only after the output has settled close to its final value. It is therefore recommended that t_{LED_SAMP}, the separation between the LED ON start and SAMP start be at least $3xt_{TIA\_SETTLE}$. Note that additional considerations from achieving optimal ambient rejection might require a separation higher than this value.
- f_{SIG}, the effective signal bandwidth is determined as $f_{RC}*t_{W\_SAMP}/t_{PRF}$ where f_{RC}, t_{W_SAMP} and t_{PRF} correspond to the Noise reduction filter bandwidth, SAMP width and PRF period respectively. The parameters should be chosen such that the signal bandwidth is much higher than the bandwidth of interest (eg. 4 Hz). Note that f_{RC} can have a device-to-device variation that could cause its value to be up to 35% lower than its nominal value.
  As an example, with an external clock of 32 kHz (t_{TE} = 31.25us): f_{RC} = 2.5 kHz, t_{W_SAMP} = 93.75us ($3xt_{TE}$), t_{PRF} = 20ms (50Hz PRF). For this case, a worst case (lowest) f_{SIG} would be:

  $$f_{SIG} = (2.5kHz \times 0.65) \times (93.75us) / 20ms = 7.6\ Hz$$

- An additional consideration while operating in the Internal oscillator mode (t_{TE}=7.8125us) comes from the jitter of the 128 kHz oscillator which affects the sampling instant. To avoid any noise degradation from this jitter, the TIA output should be well settled at the falling edge of the SAMP signal. It is recommended that the SAMP width be at least 7-8 TIA time constants to keep that the noise degradation from jitter to be small. As an example, for t_{W_SAMP} = 31.25us ($4xt_{TE}$), Rf = 500 Kohm. The jitter considerations would require τ_{TIA_SETTLE} to be about 4us or lesser. So for this case, C_F can be chosen to be the highest setting with a value lower than 8 pF. With the EARLY_OFFSET_DAC bit set to '1', the TIA settling gets advanced and the effect of jitter reduces for the same SAMP width.

7.3.6 Handling signal chain transient behavior

Due to presence of the Noise reduction filter in the Receiver signal chain, any disturbance to the 'steady-state' signal from the PD in a given phase can result in an associated settling time that can span multiple PRF cycles. The time constant associated with the noise reduction filter is equal to $1/(2\pi f_{RC})$. So for a f_{RC}=2.5 kHz, the time constant of the filter is 64 us. Depending on the extent of the signal transient, 5-10 filter time constants may be required to get back to steady state. Since the filter is switched to the TIA output only during the SAMP phase, the filter recovery may span over several PRF cycles. For example, at 50 Hz PRF, 90.55 us SAMP width and f_{RC}=2.5 kHz, the time required for recovery from a disturbance to the signal could be in the range of 100 ms, a parameter referred to as $t_{CHANNEL}$.

The quickest way to speed up this transient and reduce $t_{CHANNEL}$ is to change the timing temporarily to a higher PRF so that the filter has more frequent active for quicker settling. The other way to speed up the transient is to temporarily increase the filter bandwidth setting. However, it should be noted that a change in the filter bandwidth setting slightly changes the DC value of the output code

The other type of transient behavior is when the TIA saturates in one of the phases. The recovery of the TIA might affect the subsequent phase especially if the SAMP phases are close to each other. The recovery time also depends on the over-saturation factor, which is the factor by which the signal current in the saturating phase is higher than the input current required to cause a full-scale TIA output. The recovery in the Ambient phase as a function of the over-saturation factor in the preceding LED phase is shown in Figure 53.

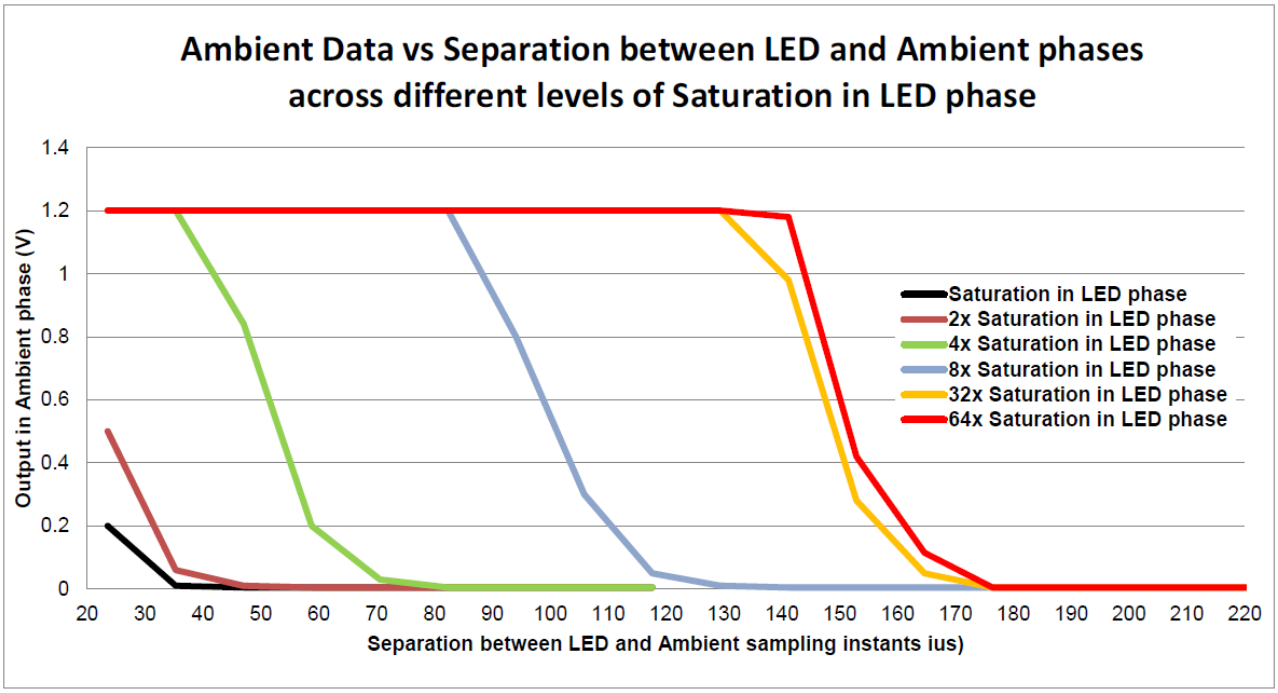


Figure 53. Recovery of the ambient phase as a function of the over-saturation factor in the LED phase

7.3.7 Connecting PPSI262s in parallel

If two PPSI262s running in parallel must share a common I²C bus, then such parallel operation can be accomplished by keeping the slave address of the two PPSI262s different in the LSB by connecting the SEN pins of PPSI262-1and PPSI262-2, as shown in Figure 54.

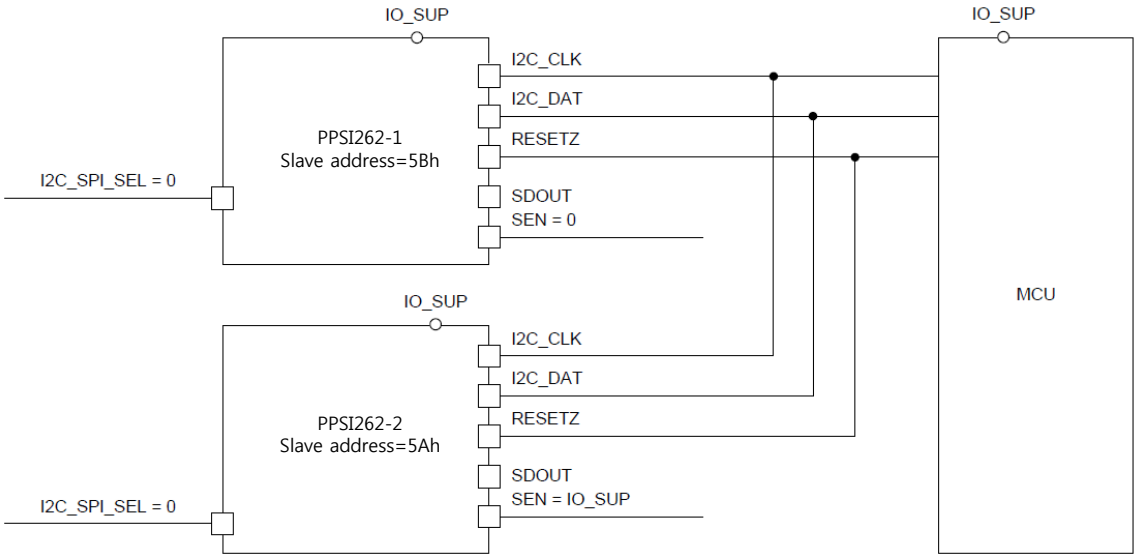


Figure 54. Connection of two PPSI262s to the MCU when operating in I²C mode

Figure 55 shows a case where the parallel PPSI262s are operated in SPI mode with two fully independent SPI interfaces from the MCU.

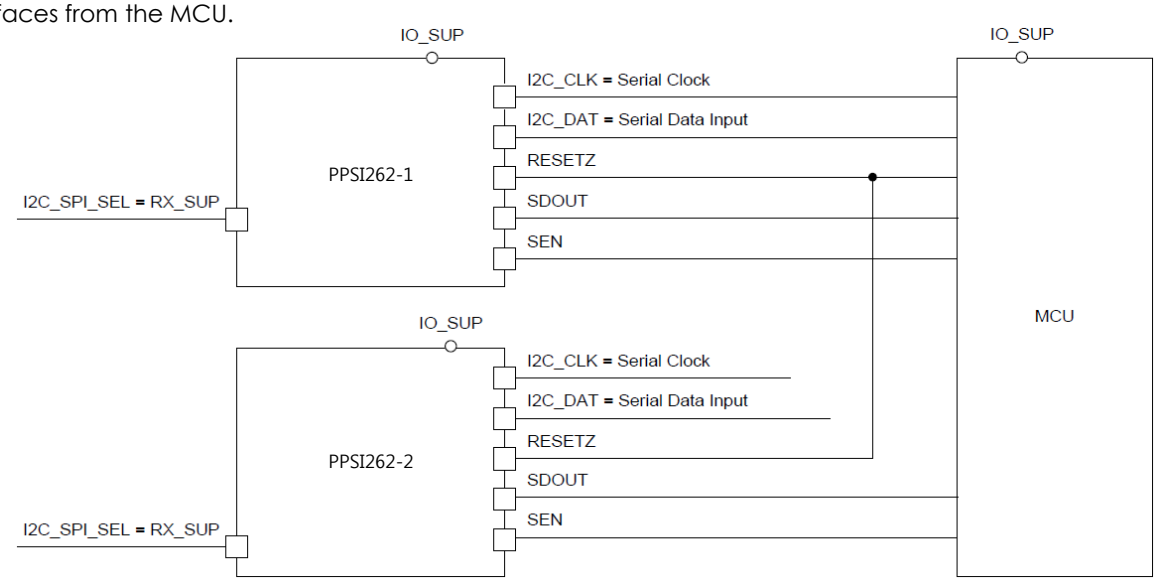


Figure 55. Connection of two PPSI262s in SPI mode with an independent SPI bus

Figure 56 shows a case where the parallel PPSI262s share some part of the SPI bus. The serial clock and serial data can be shared between the two PPSI262s but the SEN control to each PPSI262 must be separate.
Additionally, if the SDOUTs are shared between the two PPSI262s, then care must be taken to use the SDOUT_TRISTATE register bit to ensure that there is no contention of the SDOUT bus between the two PPSI262s.

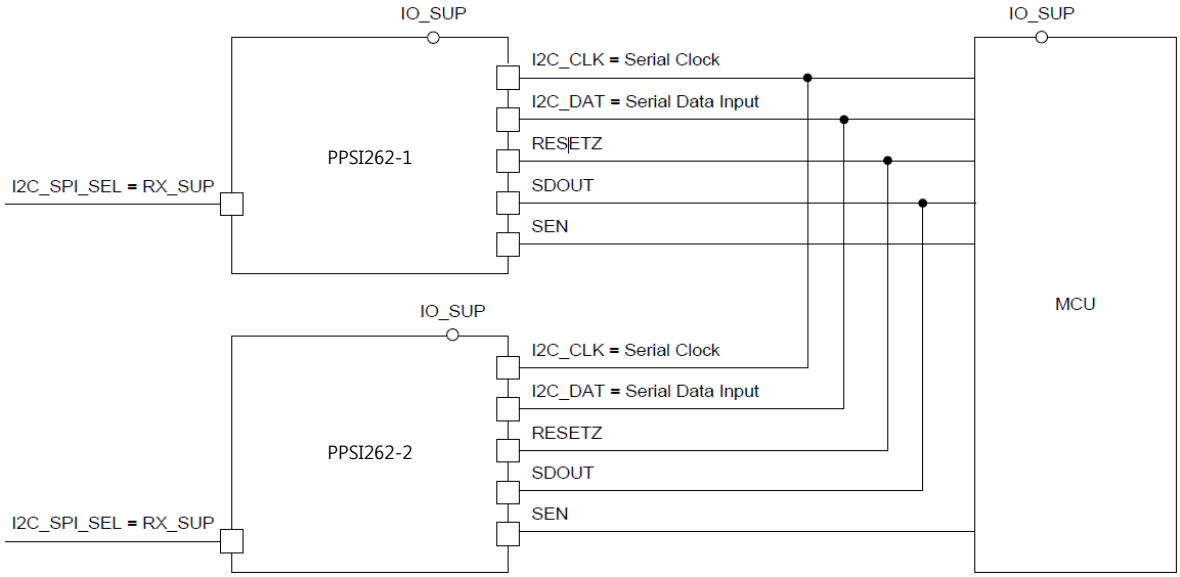


Figure 56. Connection of two PPSI262s in SPI mode that share a portion of SPI bus

7.3.8 Example register settings:

This section shows example register settings for different PRFs. The clock for the timing engine is assumed to be a 32 kHz external clock corresponding to t_{TE}=31.25us. The SAMP width is set to 3xt_{TE} and the LED ON time is 4xt_{TE}. NUMAV is set to 1 (two ADC averages).

Table 47 shows the sample timing registers at 1 kHz PRF. At this high PRF, there is insufficient time to operate the device in Deep sleep mode. Note how the Active phase spans the entire PRF period and the first LED starts at A count of 0.

Register address in Hex	Timing register name	Value in Hex
1	LED2STC	1
2	LED2ENDC	3
3	LED1LEDSTC	A
4	LED1LEDENDC	D
5	LED3STC	6
6	LED3ENDC	8
7	LED1STC	B
8	LED1ENDC	D
9	LED2LEDSTC	0
A	LED2LEDENDC	3
B	ALED1STC	10
C	ALED1ENDC	12
D	LED2CONVST	5
E	LED2CONVEND	8
F	ALED2CONVST	A
10	ALED2CONVEND	D
11	LED1CONVST	F
12	LED1CONVEND	12
13	ALED1CONVST	14
14	ALED1CONVEND	17
1D	PRPCOUNT	1F
36	LED3LEDSTC	5
37	LED3LEDENDC	8
43	LED4LEDSTC	F
44	LED4LEDENDC	12
52	DATA_RDY_STC	1D
53	DATA_RDY_END	1D
64	DYN_TIA_STC	0
65	DYN_TIA_END	20
66	DYN_ADC_STC	0
67	DYN_ADC_END	20
68	DYN_CLK_STC	0
69	DYN_CLK_END	20
6A	DEEP_SLEEP_STC	21
6B	DEEP_SLEEP_ENDC	18

Table 47. Sample timing register settings – 1kHz PRF

Table 48 shows the sample timing registers at 500 Hz PRF. The device is put in Deep sleep mode for a fraction of the PRF cycle. The Active phase (as defined by the time counts of DYN_TIA_STC, DYN_ADC_STC and DYN_CLK_STC) start at 0. The first LED ON signal is offset by a time determined by t_{ACTIVE_PWRUP}.

Register address in Hex	Timing register name	Value in Hex
1	LED2STC	B
2	LED2ENDC	D
3	LED1LEDSTC	14
4	LED1LEDENDC	17
5	LED3STC	10
6	LED3ENDC	12
7	LED1STC	15
8	LED1ENDC	17
9	LED2LEDSTC	A
A	LED2LEDENDC	D
B	ALED1STC	1A
C	ALED1ENDC	1C
D	LED2CONVST	F
E	LED2CONVEND	12
F	ALED2CONVST	14
10	ALED2CONVEND	17
11	LED1CONVST	19
12	LED1CONVEND	1C
13	ALED1CONVST	1E
14	ALED1CONVEND	21
1D	PRPCOUNT	3F
36	LED3LEDSTC	F
37	LED3LEDENDC	12
43	LED4LEDSTC	19
44	LED4LEDENDC	1C
52	DATA_RDY_STC	27
53	DATA_RDY_END	27
64	DYN_TIA_STC	0
65	DYN_TIA_END	23
66	DYN_ADC_STC	0
67	DYN_ADC_END	23
68	DYN_CLK_STC	0
69	DYN_CLK_END	23
6A	DEEP_SLEEP_STC	2E
6B	DEEP_SLEEP_ENDC	38

Table 48. Sample timing register settings – 500Hz PRF

To adapt the same conditions to a different PRF, only the PRPCT and DEEP_SLEEP_ENDC registers need to be modified with respect to Table 48. For example, at 100 Hz PRF, change PRPCT to 13Fh and DEEP_SLEEP_ENDC to 138h.

8. Power Supply Recommendations

The guidelines for Power supply sequencing and Device initialization are shown in Figure 57 and Figure 58.

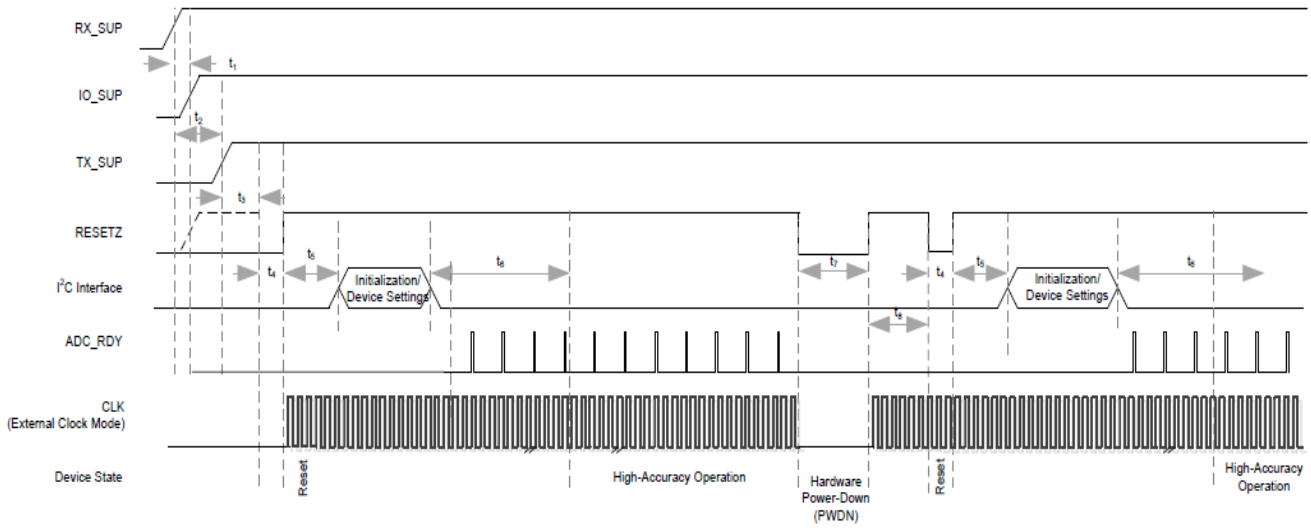


Figure 57. Power Supply Sequencing, Device Initialization, and Hardware Powerdown Timing

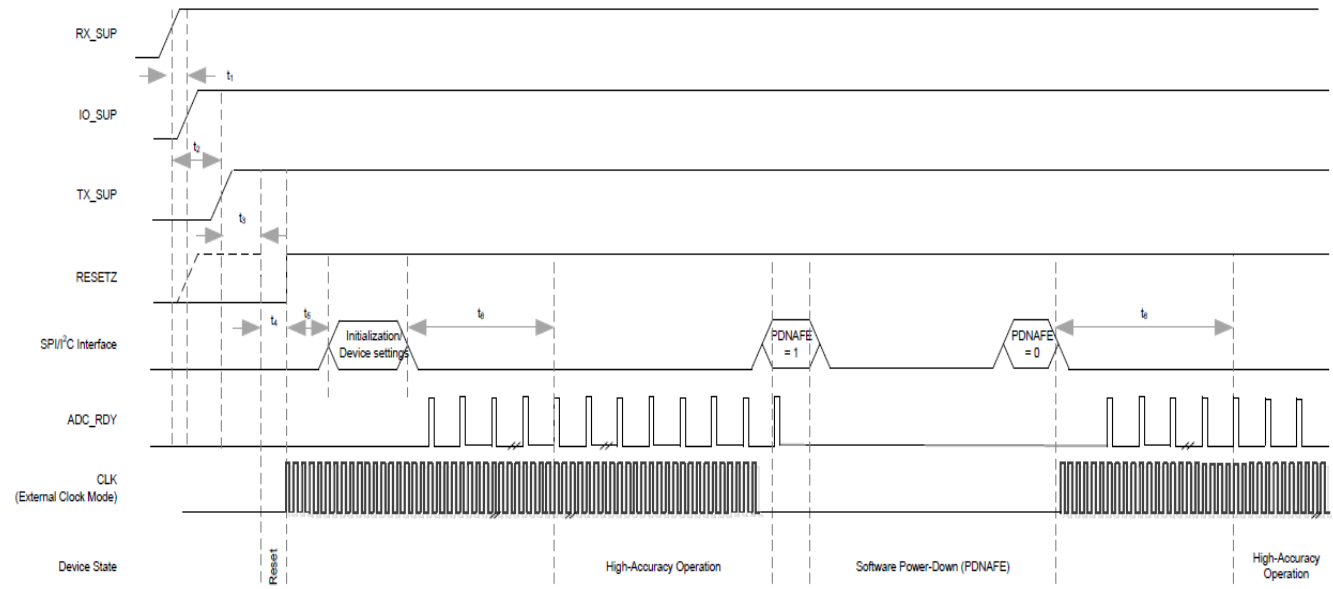


Figure 58. Power Supply Sequencing, Device Initialization, and Software Powerdown Timing

Timing	Description	Value
T1	Time between RX_SUP and IO_SUP ramping up	Ramp up RX_SUP before or at the same time as IO_SUP. Keep T1 as small as possible. Eg.10 ms
T2	Time between RX_SUP and TX_SUP ramping up	Keep t_2 as small as possible (for example,10 ms).
T3	Time between all supplies stabilizing and start of RESETZ low going pulse	> 10 ms
T4	RESETZ pulse width for the device to get reset	Between 25 us and 50 us
T5	Time between resetting the device and issue of I^2C commands	> 1 ms
T6	Time between I^2C commands and the ADC_RDY pulse which corresponds to valid data	$T_{CHANNEL}$ (1)
T7	Width of RESETZ pulse for the device to enter into PWDN (power-down) mode	> 200 us
T8	Time from exiting power-down mode and subsequently resetting the device	> 10 ms

Table 49. Timing Parameter for power Supply Sequencing, Device Initialization, and Powerdown Timing

(1) Parameter $T_{CHANNEL}$ parameter is described in the section Handling signal chain transient behavior

Table 50 illustrates the configuration register that are recommended to be programmed as part of the Initialization sequence after Power up when operatingin the LDO Bypass mode

Register control	Register bit address in Hex[Bit(S)]	Setting	Comments
ENABLE_ULP	0[5]	1	Enable ULP mode, Set this bit first before setting other bits
CONTROL_DYN_TIA	23[4]	1	TIA is power cycled
CONTROL_DYN_ADC	23[3]	1	ADC is power cycled
CONTROL_DYN_BIAS	23[14]	1	Bias is power cycled
CONTROL_DYN_TX(1)	50[3]	1	TX amp is power cycled
CONTROL_DYN_TX(0)	23[20]	1	
CONTROL_DYN_BG(1)	4B[0]	1	Bandgap is power cycled
CONTROL_DYN_VCM(1)	4B[3]	1	VCM is power cycled
ENABLE_INPUT_SHORT	31[5]	1	During power-down phase of the TIA, the analog inputs are Differentially shorted to maintain the PD bias
EARLY_OFFSET_DAC	3A[20]	1	Offset DAC is transitioned at the rising edge of LED ON instead of at the rising edge of SAMP
ENABLE__PTT(2)	4E[2]	1	Enable PTT mode
ENABLE_ECG_CHOP(2)	61[19]	1	Enable ECG chop mode
ENABLE_RLD(2)	62[23]	1	Enable RLD mode
CONTROL_DYN_ALDO(3)	4B[1]	1	ALDO is power cycled
CONTROL_DYN_DLDO(3)	4B[2]	1	DLDO is power cycled
SHORT_ALDO_TO _DLDO_IN_DEEP_SLEEP(3)	50[5]	1	ALDO output is shorted to DLDO output in deep sleep phase

Table 50. Recommended Register settings for Device Initialization

(1) Do not set these bits if operating in the PTT mode
(2) Set these bits if operating in the PTT mode
(3) Set these bits additionally if operating in the 'LDO enable' mode

9. Layout guidelines

Two key layout guidelines are:

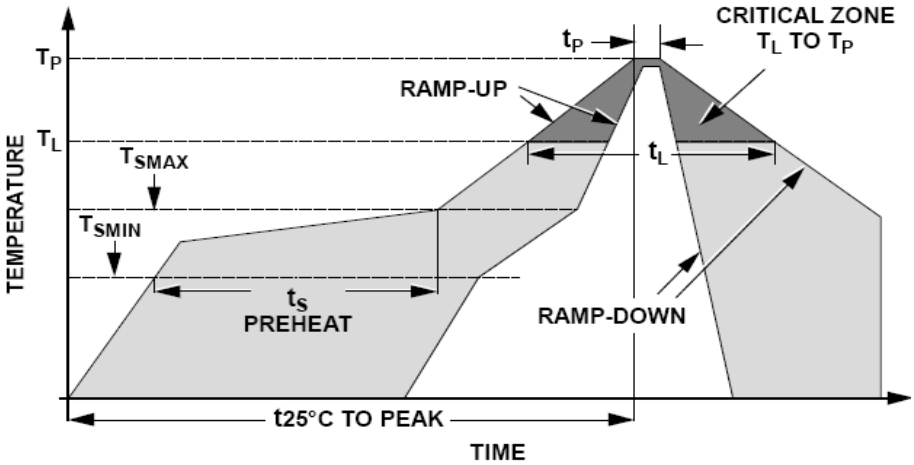
1. TX1, TX2, and TX3 are fast-switching lines and must be routed away from sensitive lines (such as the INP, INN inputs).
2. The device can draw high-switching currents from the TX_SUP pin. A decoupling capacitor must be electrically close to the pin.

10. Reflow Profile

***Standard Reflow soldering condition**

Reference	J-STD-020-C, J-STD-033		
Maximum Peak Temperature	260℃		
Moisture Sensitivity Level	MSL 3		
Bake Condition		Exposure Time > 72 hours	Exposure Time < 72 hours
	Bake @ 125℃	9 hours	7 hours
	Bake @ 90℃, < 5% RH	33 hours	23 hours
	Bake @ 40℃, < 5% RH	13 days	9 days

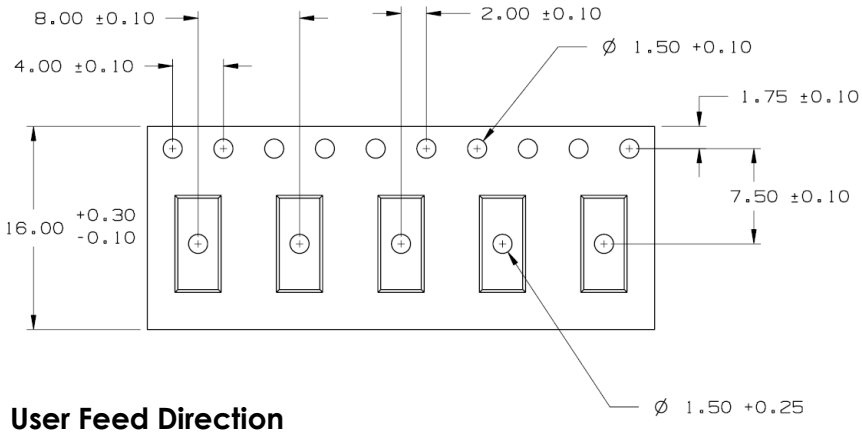
- Recommended Solder Reflow

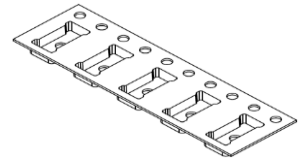


Profile Feature	Pb-Free Assembly
Average ramp-up rate(T_{SMAX} to T_P)	3℃/second max.
Preheat - Temperature Min.(T_{SMIN}) - Temperature Max.(T_{SMAX}) - Time(T_{SMIN} to T_{SMAX}) (T_S)	150℃ 200℃ 60 ~ 180 seconds
Time maintained above : - Temperature(T_L) - Time(t_L)	217℃ 60 ~ 150 seconds
Peak temperature(T_P)	260℃
Time within 5℃ of actual peak temperature(T_P)^2	20 ~ 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

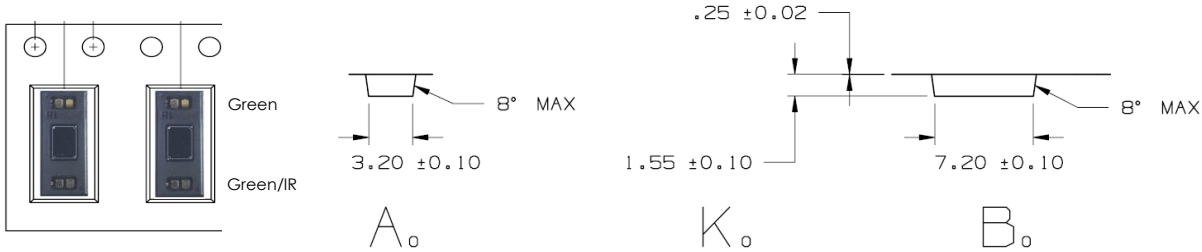
11. Package Specifications

11.1 Carrier Tape Information I[Unit : mm]



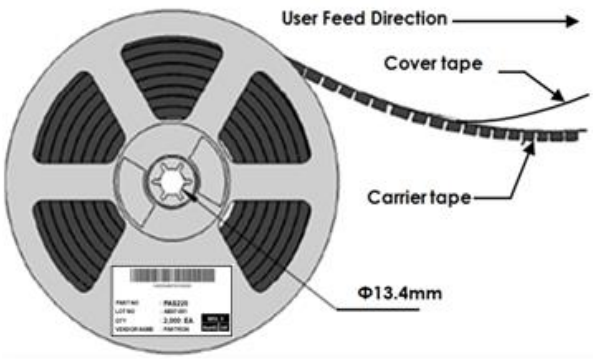


User Feed Direction



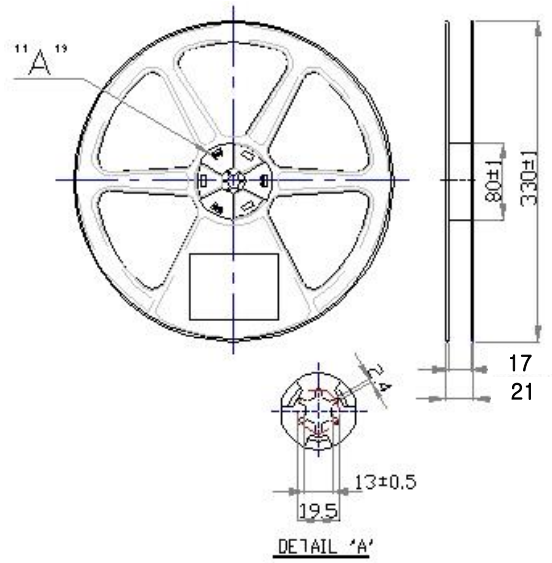
※ Note
1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ±0.20mm.
3. Measured from centerline of sprocket hole to centerline of pocket.

11.2. Carrier tape Information II(unit : mm)



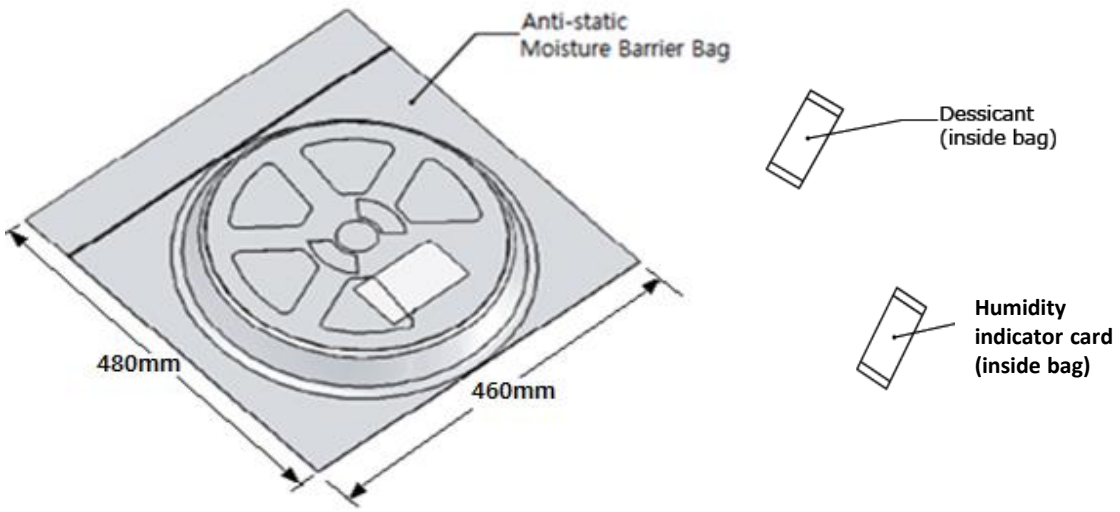
※ Note 1. Reel Diameter : 330±1 mm
2. Quantity Per Reel : 5,000EA
3. Label : external package & reel

11.3. Reel Information (unit : mm)



11.4. Aluminum Bag Information(Unit : mm)

(1) Material: Aluminum + Nylon + LDPE
(2) Quantity: 5,000ea / 1pcs
(3) Put Silica gel and humidity indicator into package and attach the Label



12. Conditions of product storage and baking

Please use this product within 6 months after receipt.

- The product shall be stored without opening the packing under the ambient temperature from 5 to 35℃(Celsius) and humidity from 20 to 70% RH.
  (Packing materials, in particular, may be deformed at the temperature over 40℃ (Celsius)).

- The product left more than 6 months after receipt, it needs to be confirmed the solderbility before used.

- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_X, etc.).

- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

  This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020).

- After the packing opened, the product shall be stored at <30℃(Celsius) / <60% RH and the product shall be used within 168 hours.

- When the color of the indicator in the packing changed, the product shall be baked before soldering.

- Baking condition : 125±5℃(Celsius), 9 hours, 1 time

- The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant

13. Reliability Specifications

No.	Test item	Test condition
1	**Preconditioning Test**	Bake + Soak(MSL3 or above) + 3X reflow [Test was performed after a lapse of two hours.]
2	**High Temperature & Humidity Resistance**	+85℃/85% R.H., 120 hours, [Test was performed after a lapse of two hours.]
3	**Temperature Cycle**	-40±2℃(30 min.) → +85℃±2℃(30 min.), 300 cycles [Test was performed after a lapse of two hours.]
4	**Low Temperature Resistance**	-20℃, 1000 hours [Test was performed after a lapse of two hours.]
5	**High Temperature Resistance**	+125℃, 1000 hours [Test was performed after a lapse of two hours.]
6	**High Temperature Operating Life**	125℃ / Max V_{CC} / Dynamic, 1000 hours
7	**Low Temperature Operating Life**	-20℃ / Max V_{CC} / Dynamic, 1000 hours
8	**Unbiased HAST**	130℃ / 85% / 33.3psi, 96 hours [Test was performed after a lapse of two hours.]
9	**ESD**	HBM : 2kV, MM : 200V CDM : 1kV, Latch up : ±100mA/3.6V
10	**Vibration**	Frequency: 0 ~ 500Hz, Amplitude : 1.52 mm(duration of 1 minute) 2 hours, 3 axis (X, Y, Z direction) [Test was performed after a lapse of two hours.]
11	**Drop**	1.5 m, Steel plate, 12 times
12	**Reflow**	3 reflow cycles [Test was performed after a lapse of two hours.]
13	**Solder heat**	+350℃, 5 sec., each pad(4-point) respectively
14	**EMI**	1kV/m, 60Hz