LPN2010C

Enhancement Mode N-Channel Power MOSFET

Description

LPN2010C use advanced FSMOS™ technology to provide low $R_{DS(on)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in Synchronous-rectification applications.

◆ $V_{DS,min}$	100V
◆ $I_{D,pulse}$	140A
◆ $R_{DS(ON),max}$@V_{GS}=10V	20mΩ
◆ Q_g	19.8nC

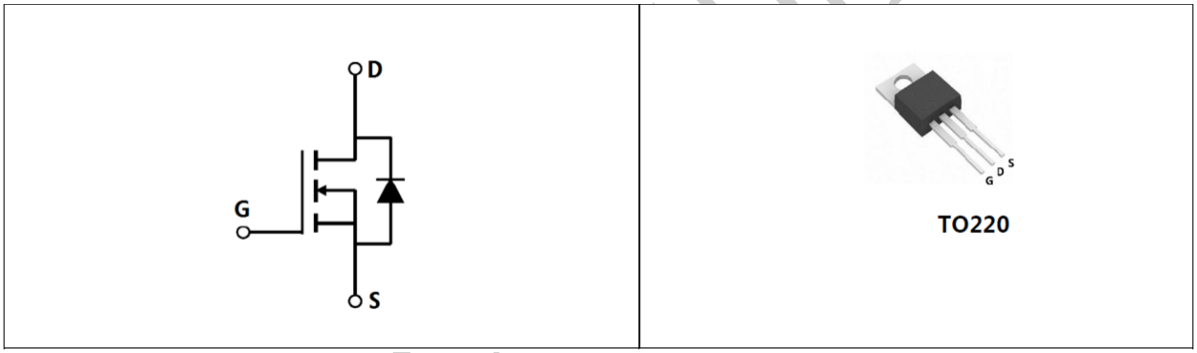
Features

- Low $R_{DS(on)}$&FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

Schematic and Package Information



Schematic Diagram　　Pin Assignment Top View

Ordering Information

Package	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Box/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
LPN2010C	TO220	yes	yes	yes

Absolute Maximum Rating at T_j=25℃ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	±20	V
Continuous drain current[1)]	I_D	50	A
Pulsed drain current[2)]	$I_{D,puse}$	140	A
Power dissipation[3)]	P_D	80	W
Single pulsed avalanche energy[5)]	E_{AS}	30	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	℃

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.38	℃/W
Thermal resistance, junction-ambient[4)]	$R_{\theta JA}$	62.5	℃/W

Electrical Characteristics at T_j=25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	V_{DS}= V_{GS}, I_D=250uA
Drain-source on-state resistance	$R_{DS(ON)}$		17	20	mΩ	V_{GS}=10V, I_D=8A
Drain-source on-state resistance	$R_{DS(ON)}$		12	26	mΩ	V_{GS}=4.5V, I_D=6A
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=20V
				-100		V_{GS}=-20V
Drain-source leakage current	I_{DSS}			1	uA	V_{DS}=100V, V_{GS}=0V

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		1190.6		pF	V_{GS}=0V,
Output capacitance	C_{oss}		194.6		pF	V_{DS}=50V,
Reverse transfer capacitance	C_{rss}		4.1		pF	f=1MHz
Turn-on delay time	$T_{d(on)}$		17.8		nS	V_{GS}=10V,
Rise time	t_r		3.9		nS	V_{DS}=50V,
Turn-off delay time	$T_{d(off)}$		33.5		nS	R_G=2.2Ω,
Fall time	t_f		3.2		nS	I_D=10A

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		19.8		nC	I_D=8A, V_{DS}=50V, V_{GS}=10V
Gate-source charge	Q_{gs}		2.4		nC	
Gate-drain charge	Q_{gd}		5.3		nC	
Gate plateau voltage	$V_{plateau}$		3.2		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward current	I_S			50	A	V_{GS}<Vth
Pulsed source current	I_{SP}			140	A	
Diode forward voltage	V_{SD}			1.3	V	I_S=8A，V_{GS}=0V
Reverse recovery time	t_{rr}		50.2		nS	I_S=8A，di/dt=100A/uS
Reverse recovery charge	Q_{rr}		95.1		nC	
Peak reverse recovery current	I_{rrm}		2.5		A	

Note

1） Calculated continuous current based on maximum allowable junction temperature.

2） Repetitive rating；pulse width limited by max. junction temperature.

3） Pd is based on max. junction temperature，using junction-case thermal resistance.

4） The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper，in a still air environment with T_a=25℃.

5） V_{DD}=50V，R_G=25Ω，L=0.3mH，starting T_j=25℃

Electrical Characteristics Diagrams

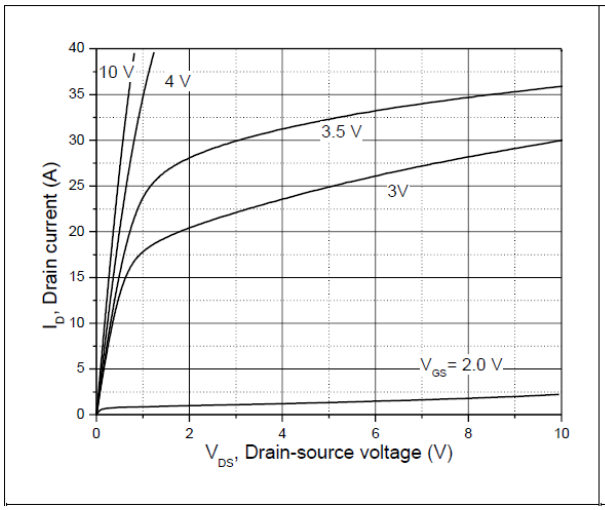


Figure 1， Typ. Output characteristics

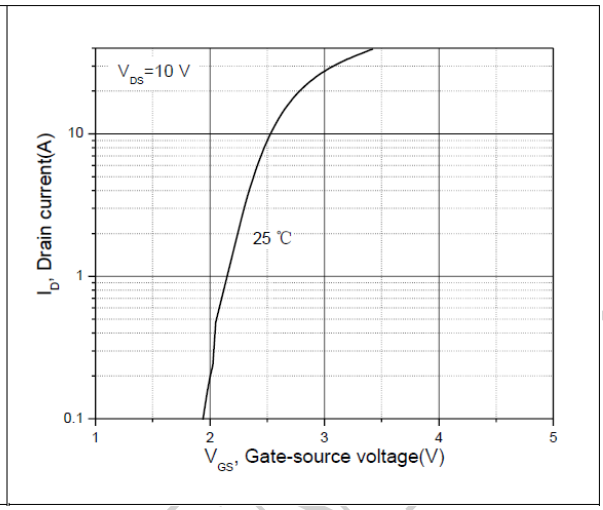


Figure 2， Typ. Transfer characteristics

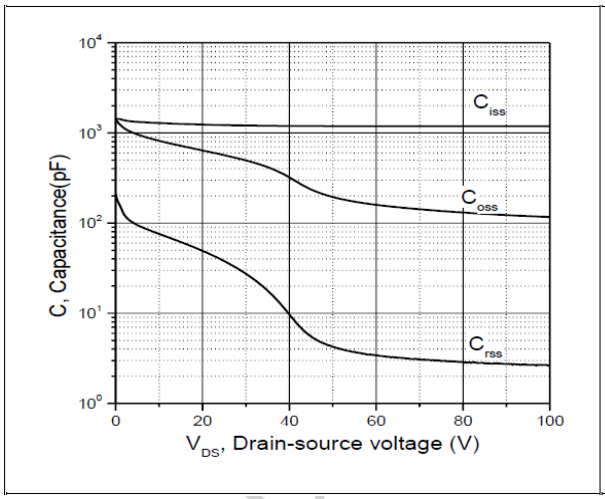


Figure 3， Typ. capacitances

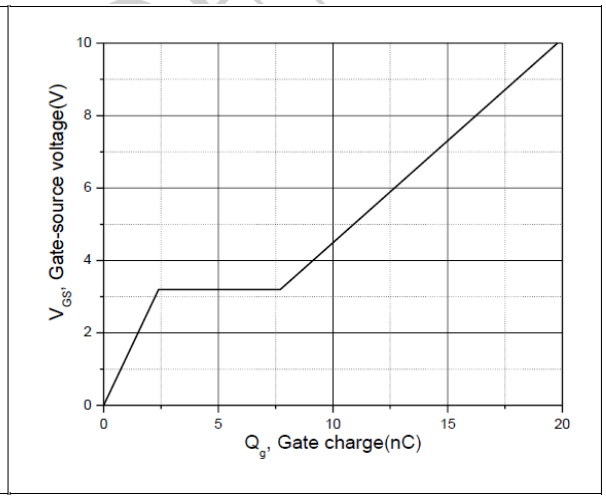


Figure 4， Typ. gate charge

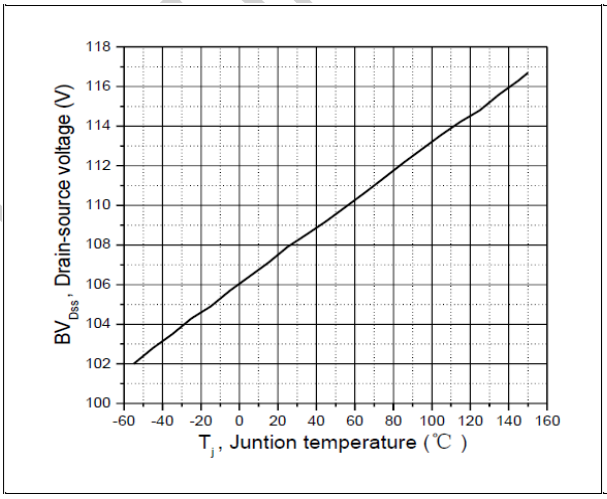


Figure 5， Drain-source breakdown voltage

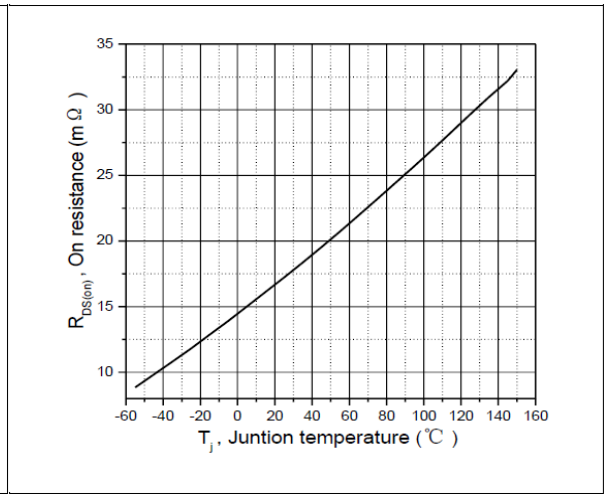


Figure 6， Drain-source on-state resistance

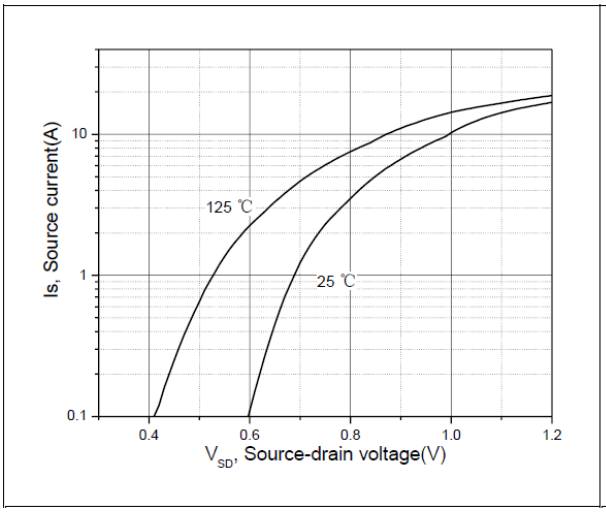


Figure 7，Forward characteristics of body diode

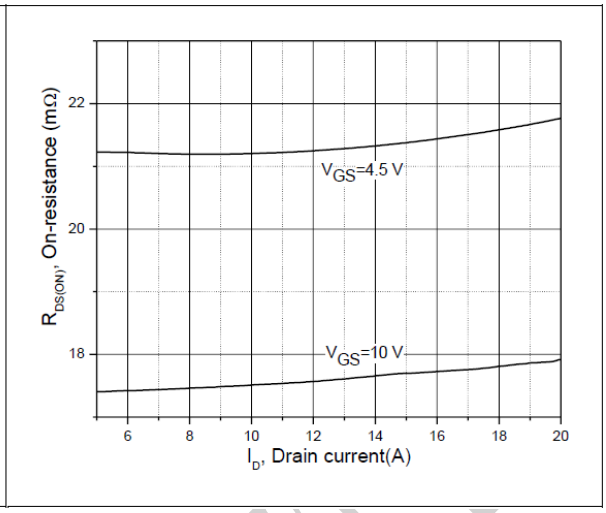


Figure 8，Drain-source on-state resistance

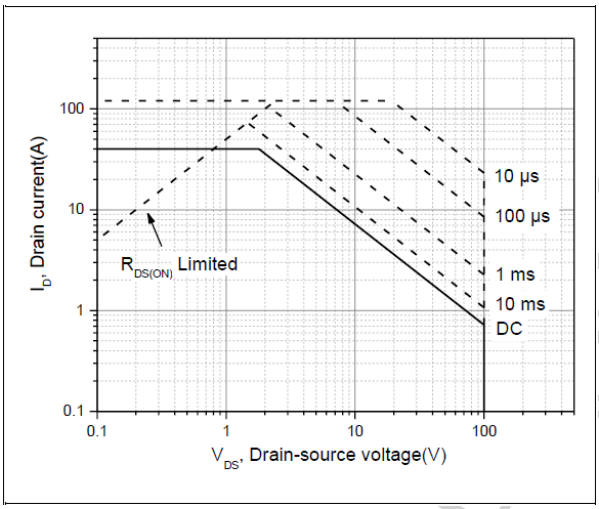


Figure 9，Safe operation area T_C=25℃

Test circuits and waveforms

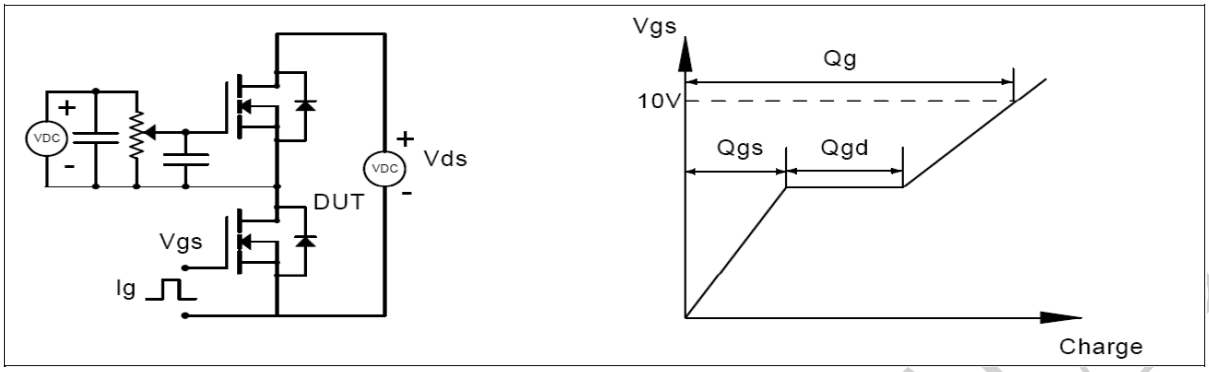


Figure 1，Gate charge test circuit &waveform

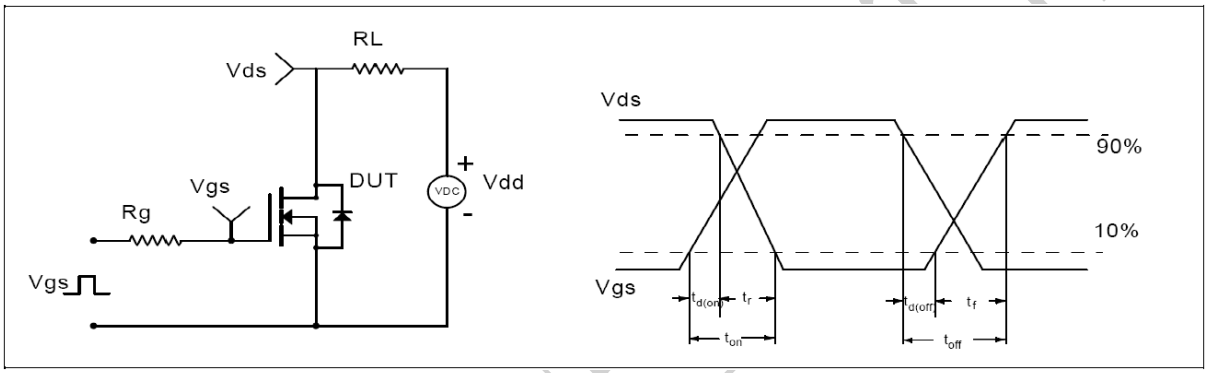


Figure 2，Switching time test circuit & waveforms

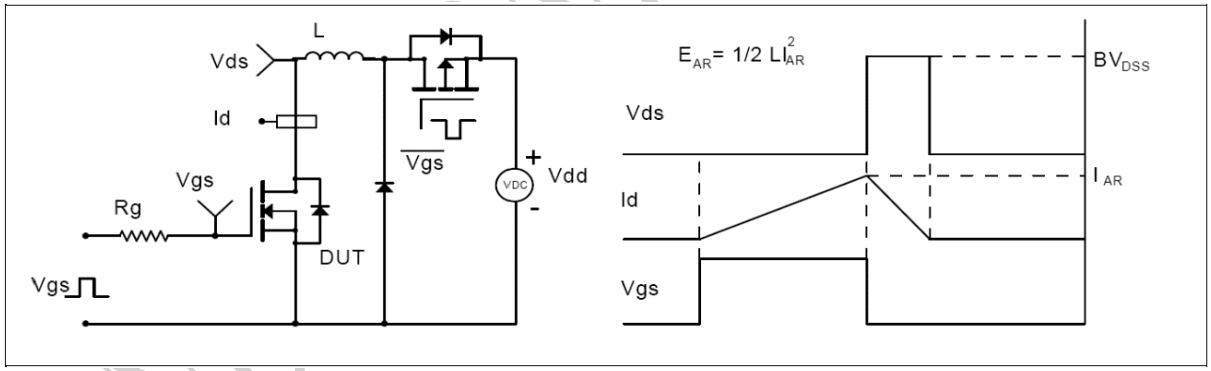


Figure 3，Unclamped inductive switching (UIS) test circuit & waveforms

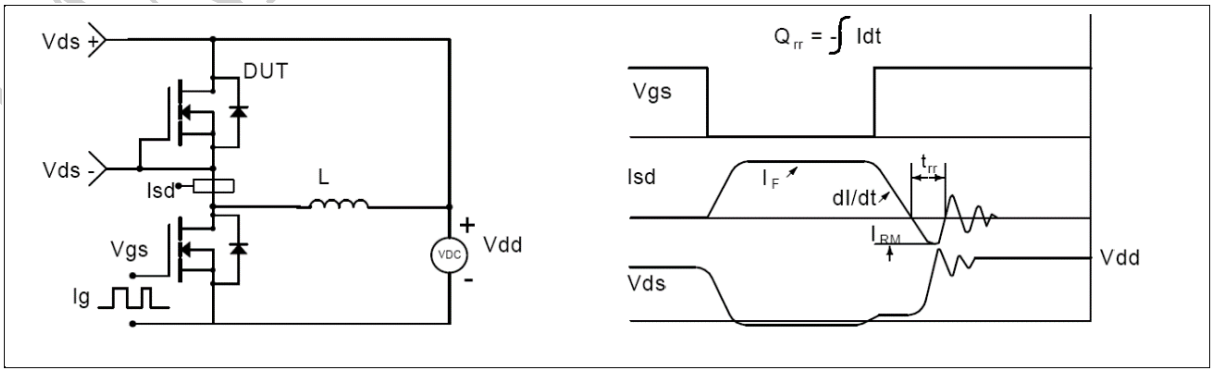
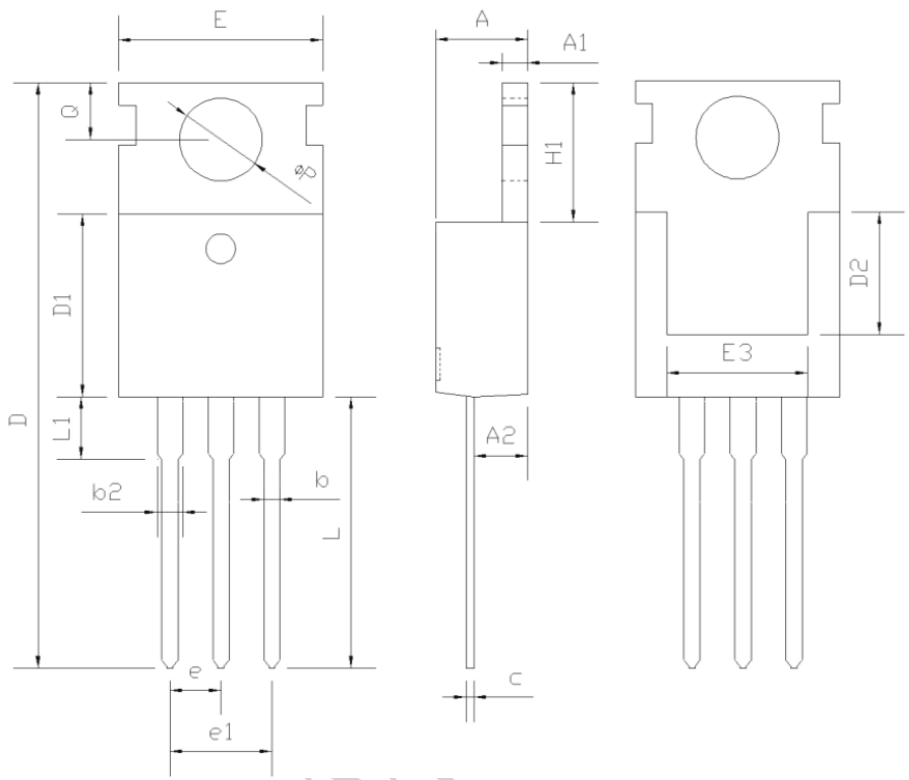


Figure 4，Diode reverse recovery test circuit & waveforms

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	