SN2040 1 A, Single-Input, Single Cell Li-Ion and Li-Pol Battery Charger

1 Features

- Charging
  - 1% Charge Voltage Accuracy
  - 10% Charge Current Accuracy
  - Pin Selectable USB 100 mA and 500 mA Maximum Input Current Limit
  - Programmable Termination and Precharge Threshold
- Protection
  - 30-V Input Rating; with 6.6 V or 7.1 V Input Overvoltage Protection
  - Input Voltage Dynamic Power Management
  - 125°C Thermal Regulation; 150°C Thermal Shutdown Protection
  - OUT Short-Circuit Protection and ISET Short Detection
  - Operation over JEITA Range via Battery NTC – 1/2 Fast-Charge-Current at Cold, 4.06 V at Hot
  - Fixed 10 Hour Safety Timer
- System
  - Automatic Termination and Timer Disable Mode (TTDM) for Absent Battery Pack With Thermistor
  - Status Indication – Charging/Done
  - Available in Small 2×2mm^2 DFN-10 Package

2 Applications

- Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

3 Description

The SN2040 is a highly integrated Li-Ion and Li-Pol linear charger device targeted at space-limited portable applications. The device operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The SN2040 has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

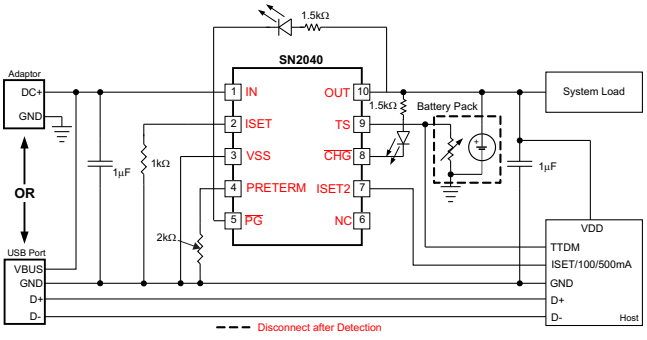
The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The pre-charge current and termination current threshold are programmed through an external resistor on the SN2040. The fast charge current value is also programmable through an external resistor.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN2040	WSON (10)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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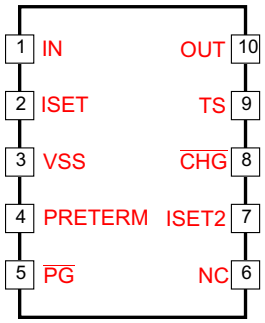
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2016	*	Initial release

5 Pin Configuration and Functions

DSQ Package
10-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1 μF to 10 μF, connect from IN to VSS.
OUT	10	O	Battery Connection. System Load may be connected. Expected range of bypass capacitors 1 μF to 10 μF.
PRE-TERM	4	I	Programs the Current Termination Threshold (5 to 50% of Iout which is set by ISET) and Sets the Pre-Charge Current to twice the Termination Current Level. Expected range of programming resistor is 1 k to 10 kΩ (2 k: Ipgm/10 for term; Ipgm/5 for precharge)
ISET	2	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 10.8 k (50 mA) to 540 Ω (1000 mA).
ISET2	7	I	Programming the Input/Output Current Limit for the USB or Adaptor source: High = 500 mA max, Low = ISET, FLOAT = 100 mA max.
TS	9	I	Temperature sense terminal connected to SN2040 -10 k at 25°C NTC thermistor, in the battery pack. Floating T terminal or pulling High puts part in TTDM “Charger” Mode and disable TS monitoring, Timers and Termination. Pulling terminal Low disables the IC. If NTC sensing is not needed, connect this terminal to VSS through an external 10-kΩ resistor. A 250 kΩ from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
VSS	3	–	Ground terminal
$\overline{\text{CHG}}$	8	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
$\overline{\text{PG}}$	5	O	Low (FET on) indicates the input voltage is above UVLO and the OUT (battery) voltage.
NC	6	NA	Do not make a connection to this terminal (for internal use) – Do not route through this terminal
Thermal Pad		–	There is an internal electrical connection between the exposed thermal pad and the VSS terminal of the device. The thermal pad must be connected to the same potential as the VSS terminal on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS terminal must be connected to ground at all times

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Input voltage	IN (with respect to VSS)	–0.3	30	V
		OUT (with respect to VSS)	–0.3	7	V
		PRE-TERM, ISET, ISET2, TS, $\overline{CHG}$, $\overline{PG}$ (with respect to VSS)	–0.3	7	V
	Input current	IN		1.25	A
	Output current (continuous)	OUT		1.25	A
	Output sink current	$\overline{CHG}$		15	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1500	

(1) The test was performed on IC terminals that may potentially be exposed to the customer at the product level. The SN2040 IC requires a minimum of the listed capacitance, external to the IC, to pass the ESD test. The D+ D- lines require clamp diodes such as CM1213A-02SR from CMD to protect the IC for this testing.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)

		MIN	NOM	UNIT
V_{IN}	IN voltage range	3.5	28	V
	IN operating voltage range, Restricted by V_{DPM} and V_{OVP}	4.45	6.45	V
I_{IN}	Input current, IN terminal		1	A
I_{OUT}	Current, OUT terminal		1	A
T_J	Junction temperature	0	125	°C
$R_{PRE-TERM}$	Programs precharge and termination current thresholds	1	10	kΩ
R_{ISET}	Fast-charge current programming resistor	0.540	10.8	kΩ
R_{TS}	10k NTC thermistor range without entering TTDM	1.66	258	kΩ

(1) Operation with V_{IN} less than 4.5V or in drop-out may result in reduced performance.

6.4 Thermal Information

THERMAL METRIC(1)		SN2040 DSQ (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out Exit	V_{IN}: 0 V → 4 V Update based on sim/char	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4 V→0 V, $V_{UVLO\_FALL} = V_{UVLO\_RISE} – V_{HYS-UVLO}$	175	227	280	mV
V_{IN-DT}	Input power good detection threshold is V_{OUT} + V_{IN-DT}	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); V_{OUT} = 3.6 V, V_{IN}: 3.5 V → 4 V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V, V_{IN}: 4 V → 3.5 V		31		mV
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5 V → 12 V	6.5	6.65	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V → 5 V		95		mV
V_{IN-DPM}	USB/Adaptor low input voltage protection. Restricts Iout at V_{IN-DPM}	Feature active in USB mode; Limit Input Source Current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825 Ω	4.34	4.4	4.46	V
		Feature active in Adaptor mode; Limit Input Source Current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 825 Ω	4.24	4.3	4.46	
$I_{IN-USB-CL}$	USB input I-Limit 100mA	ISET2 = Float; R_{ISET} = 825 Ω	85	92	100	mA
	USB input I-Limit 500mA	ISET2 = High; R_{ISET} = 825 Ω	430	462	500	
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest Resistor value considered a fault (short). Monitored for Iout>90mA	R_{ISET}: 540 Ω → 250 Ω, Iout latches off. Cycle power to Reset.	280		500	Ω
I_{OUT_CL}	Maximum OUT current limit Regulation (Clamp)	V_{IN} = 5 V, V_{OUT} = 3.6 V, V_{ISET2} = Low, R_{ISET}: 540 Ω → 250 Ω, I_{OUT} latches off after $t_{DGL-SHORT}$	1.05		1.4	A
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT terminal short-circuit detection threshold/ precharge threshold	V_{OUT}: 3 V → 0.5 V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT terminal Short hysteresis	Recovery ≥ $V_{OUT(SC)}$ + $V_{OUT(SC-HYS)}$ Rising, no Deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT terminal during short-circuit detection		10	15	20	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT terminal	V_{IN} = 0 V			1	µA
$I_{OUT(DONE)}$	OUT terminal current, charging terminated	V_{IN} = 6 V, $V_{OUT} > V_{OUT(REG)}$			6	
$I_{IN(STDBY)}$	Standby current into IN terminal	TS = LO, V_{IN} ≤ 6 V			125	µA
I_{CC}	Active supply current, IN terminal	TS = open, V_{IN} = 6 V, TTDM – no load on OUT terminal, $V_{OUT} > V_{OUT(REG)}$, IC enabled		0.8	1	mA

Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage	V_{IN} = 5.5 V, I_{OUT} = 25 mA, ($V_{TS-45°C}$≤ V_{TS} ≤ $V_{TS-0°C}$	4.16	4.2	4.23	V
$V_{O\_HT(REG)}$	Battery hot regulation Voltage	V_{IN} = 5.5 V, I_{OUT} = 25 mA, $V_{TS-45°C}$ ≤ V_{TS} ≤ $V_{TS-0°C}$	4.02	4.06	4.1	V
$I_{OUT(RANGE)}$	Programmed Output “fast charge” current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, ISET2 = LO, R_{ISET} = 540 to 10.8 kΩ	10		1000	mA
$V_{DO(IN-OUT)}$	Drop-Out, VIN – VOUT	Adjust VIN down until I_{OUT} = 0.5 A, V_{OUT} = 4.15 V, R_{ISET} = 540 , ISET2 = LO (adaptor mode); T_J ≤ 100°C		325	500	mV
I_{OUT}	Output “fast charge” formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}; V_{IN} = 5 V, ISET2 = LO		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} /I_{OUT}; 50 < I_{OUT} < 1000 mA	510	540	570	AΩ
		R_{ISET} = K_{ISET} /I_{OUT}; 25 < I_{OUT} < 50 mA	480	527	600	
		R_{ISET} = K_{ISET} /I_{OUT}; 10 < I_{OUT} < 25 mA	350	520	680	
PRECHARGE – SET BY PRETERM Terminal						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$I_{PRE-TERM}$	See the Termination Section					
$\%_{PRECHG}$	Pre-charge current, default setting	V_{OUT} < V_{LOWV}; R_{ISET} = 1080 Ω; **$R_{PRE-TERM}$= High Z**	18	20	22	$\%I_{OUT-CC}$
	Pre-charge current formula	$R_{PRE-TERM}$ = $K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)		$R_{PRE-TERM}/K_{PRE-CHG\%}$		
$K_{PRE-CHG}$	% Pre-charge Factor	V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2 k to 10 kΩ; R_{ISET} = 1080 Ω , $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 20 to 100%	90	100	110	Ω/%
		V_{OUT} < V_{LOWV}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 1 k to 2 kΩ; R_{ISET} = 1080 Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 20%	84	100	117	Ω/%
TERMINATION – SET BY PRE-TERM Terminal						
%TERM	Termination Threshold Current, default setting	V_{OUT} > V_{RCH}; R_{ISET} = 1 k; **$R_{PRE-TERM}$= High Z**	9	10	11	$\%I_{OUT-CC}$
	Termination Current Threshold Formula	$R_{PRE-TERM}$ = K_{TERM} (Ω/%) × %TERM (%)		$R_{PRE-TERM}/ K_{TERM}$		
K_{TERM}	% Term Factor	V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2 k to 10 kΩ ; R_{ISET} = 750Ω K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10 to 50%	182	200	216	Ω/%
		V_{OUT} > V_{RCH}, V_{IN} = 5 V, $R_{PRE-TERM}$ = 1 k to 2 kΩ ; R_{ISET} = 750 Ω K_{TERM} × %Iset, where %Iset is 5 to 10%	174	199	224	
$I_{PRE-TERM}$	Current for programming the term. and pre-chg with resistor. $I_{Term-Start}$ is the initial PRE-TERM curent.	$R_{PRE-TERM}$ = 2 k, V_{OUT} = 4.15 V	71	75	81	µA
%TERM	Termination current formula			R_{TERM}/ K_{TERM} %		
$I_{Term-Start}$	Elevated PRE-TERM current for, $t_{Term-Start}$, during start of charge to prevent recharge of full battery,		80	85	92	µA
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold – Normal Temp	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT}: 4.25 V → V_{RCH}	$V_{O(REG)}$ –0.120	$V_{O(REG)}$–0.095	$V_{O(REG)}$–0.070	V
	Recharge detection threshold – Hot Temp	V_{IN} = 5 V, V_{TS} = 0.2 V, V_{OUT}: 4.15 V → V_{RCH}	$V_{O\_HT(REG)}$ –0.130	$V_{O\_HT(REG)}$ –0.105	$V_{O\_HT(REG)}$ –0.080	V
BATTERY DETECT ROUTINE (NOTE: In Hot mode $V_{O(REG)}$ BECOMES $V_{O\_HT(REG)}$)						
V_{REG-BD}	VOUT Reduced regulation during battery detect	V_{IN} = 5 V, V_{TS} = 0.5 V, Battery Absent	$V_{O(REG)}$-0.450	$V_{O(REG)}$-0.400	$V_{O(REG)}$-350	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}		7		10	mA
V_{BD-HI}	High battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, Battery Absent	$V_{O(REG)}$ -0.150	$V_{O(REG)}$-0.100	$V_{O(REG)}$-0.050	V
V_{BD-LO}	Low battery detection threshold	V_{IN} = 5 V, V_{TS} = 0.5 V, Battery Absent	V_{REG-BD} +0.50	V_{REG-BD} +0.1	V_{REG-BD} +0.15	V

Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY-PACK NTC MONITOR; TS TERMINAL: 10 k NTC						
$I_{NTC-10k}$	NTC bias current	V_{TS} = 0.3 V	48	50	52	µA
$I_{NTC-DIS-10k}$	10k NTC bias current when Charging is disabled.	V_{TS} = 0 V	27	30	34	µA
$I_{NTC-FLDBK-10k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V_{TS}: Set to 1.525 V	4	5	6.5	µA
$V_{TTDM(TS)}$	Termination and timer disable mode Threshold – Enter	V_{TS}: 0.5 V → 1.7 V; Timer Held in Reset	1550	1600	1650	mV
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V → 0.5 V; Timer Enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (Float)	1800	1950	2000	mV
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6 µS) takes place near this spec threshold. V_{TS}: 1.425 V → 1.525 V		1475		mV
C_{TS}	Optional Capacitance – ESD			0.22		µF
$V_{TS-0°C}$	Low temperature CHG Pending	Low Temp Charging to Pending; V_{TS}: 1 V → 1.5 V	1205	1230	1255	mV
$V_{HYS-0°C}$	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS}: 1.5 V → 1 V		86		mV
$V_{TS-10°C}$	Low temperature, half charge	Normal charging to low temp charging; V_{TS}: 0.5 V → 1 V	765	790	815	mV
$V_{HYS-10°C}$	Hysteresis at 10°C	Low temp charging to normal CHG; V_{TS}: 1 V → 0.5 V		35		mV
$V_{TS-45°C}$	High temperature at 4.1V	Normal charging to high temp CHG; V_{TS}: 0.5 V → 0.2 V	263	278	293	mV
$V_{HYS-45°C}$	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS}: 0.2 V → 0.5 V		10.7		mV
$V_{TS-60°C}$	High temperature Disable	High temp charge to pending; V_{TS}: 0.2 V → 0.1 V	170	178	186	mV
$V_{HYS-60°C}$	Hysteresis at 60°C	Charge pending to high temp CHG; V_{TS}: 0.1 V → 0.2 V		11.5		mV
$V_{TS-EN-10k}$	Charge Enable Threshold, (10 k NTC)	V_{TS}: 0 V → 0.175 V;	80	88	96	mV
$V_{TS-DIS\_HYS-10k}$	HYS below $V_{TS-EN-10k}$ to Disable, (10 k NTC)	V_{TS}: 0.125 V → 0 V;		12		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LIVELS ON ISET2						
V_{IL}	Logic LOW input voltage	Sink 8 µA			0.4	V
V_{IH}	Logic HIGH input voltage	Source 8 µA	1.4			V
I_{IL}	Sink current required for LO	V_{ISET2} = 0.4 V	2		9	µA
I_{IH}	Source current required for HI	V_{ISET2} = 1.4 V	1.1		8	µA
V_{FLT}	ISET2 Float Voltage		575	900	1225	mV
LOGIC LEVELS ON $\overline{CHG}$ AND $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	$V_{\overline{CHG}}$ = 5V, $V_{\overline{PG}}$ = 5V			1	µA

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INPUT						
$t_{DGL(PG\_PWR)}$	Deglitch time on exiting sleep.	Time measured from V_{IN}: 0 V → 5 V 1µs rise-time to $\overline{PG}$ = low, V_{OUT} = 3.6 V		45		µs
$t_{DGL(PG\_NO-PWR)}$	Deglitch time on $V_{HYS-INDT}$ power down. Same as entering sleep.	Time measured from V_{IN}: 5 V → 3.2 V 1 µs fall-time to $\overline{PG}$ = OC, V_{OUT} = 3.6 V		29		ms
$t_{DGL(OVP-SET)}$	Input over-voltage blanking time	V_{IN}: 5 V → 12 V		113		µs
$t_{DGL(OVP-REC)}$	Deglitch time exiting OVP	Time measured from V_{IN}: 12 V → 5 V 1 µs fall-time to $\overline{PG}$ = LO		30		µs
ISET SHORT CIRCUIT TEST						
t_{DGL_SHORT}	Deglitch time transition from ISET short to I_{OUT} disable	Clear fault by disconnecting IN or cycling (high / low) TS		1		ms
PRECHARGE – SET BY PRETERM PIN						
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			70		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
TERMINATION – SET BY PRE-TERM PIN						
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
$t_{Term-Start}$	Elevated termination threshold initially active for $t_{Term-Start}$			1.25		min
RECHARGE OR REFRESH						
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT}: 4.25 V → 3.5 V in 1 µs; $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold detected in OUT-Detect Mode	V_{IN} = 5 V, V_{TS} = 0.5 V, V_{OUT} = 3.5 V inserted; $t_{DGL(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DETECT ROUTINE (NOTE: In Hot mode $V_{O(REG)}$ becomes $V_{O\_HT(REG)}$)						
$t_{DGL(HI/LOW\ REG)}$	Regulation time at V_{REG} or V_{REG-BD}			25		ms
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Pre-charge safety timer value	Restarts when entering Pre-charge; Always enabled when in pre-charge.	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS disable, OUT Short, exiting LOWV and Refresh	34000	38800	45000	s
BATTERY-PACK NTC MONITOR; TS Terminal: 10 k NTC						
$t_{DGL(TTDM)}$	Deglitch exit TTDM between states			57		ms
	Deglitch enter TTDM between states			8		µs
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10C.	Normal to Cold Operation; V_{TS}: 0.6 V → 1 V		50		ms
		Cold to Normal Operation; V_{TS}: 1 V → 0.6 V		12		ms
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45/60C.	Battery charging		30		ms

6.7 Typical Operational Characteristics (Protection Circuits Waveforms)

SETUP: SN2040 typical applications schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise indicated)

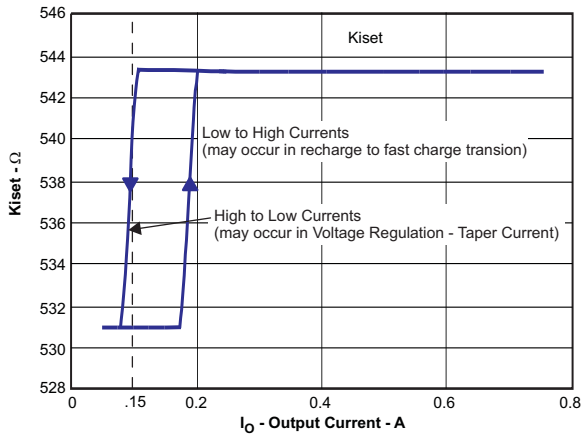


Figure 1. K_{ISET} for Low and High Currents

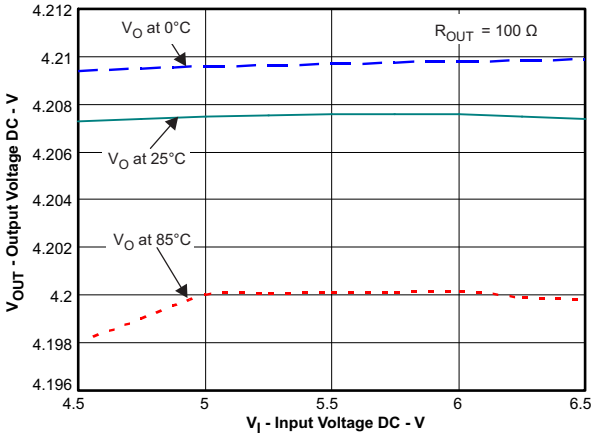


Figure 2. Line Regulation

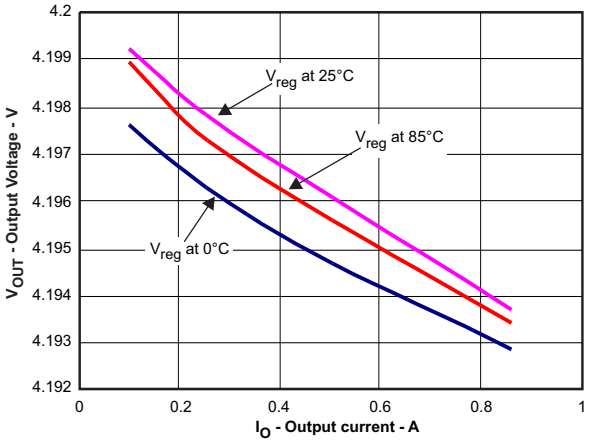


Figure 3. Load Regulation Over Temperature

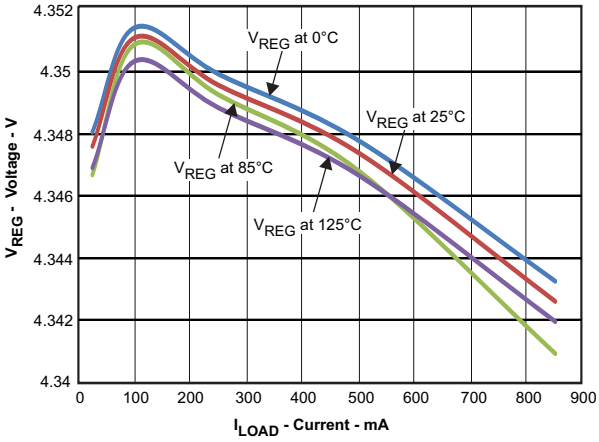


Figure 4. Load Regulation

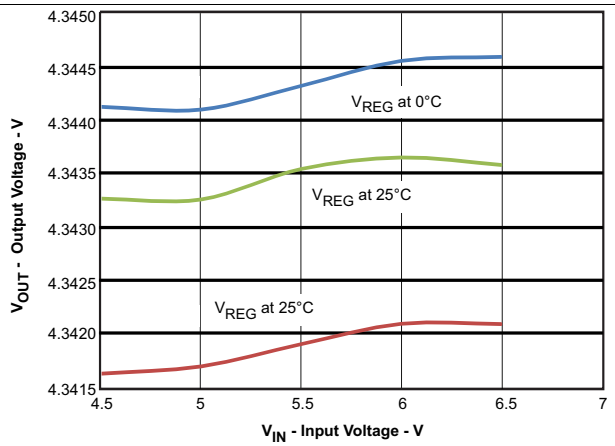


Figure 5. Line Regulation

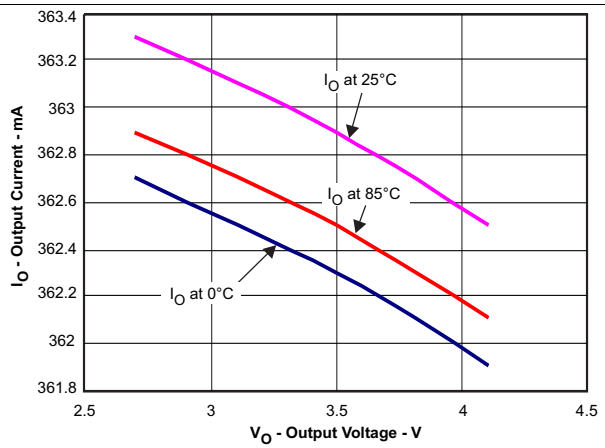


Figure 6. Current Regulation Over Temperature

7 Detailed Description

7.1 Overview

The SN2040 is a highly integrate family of 2×2 single cell Li-Ion and Li-Pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Pre-charge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current and Pre-charge/Termination Current . This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA Temperature Standard, Over-Voltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5 VDC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

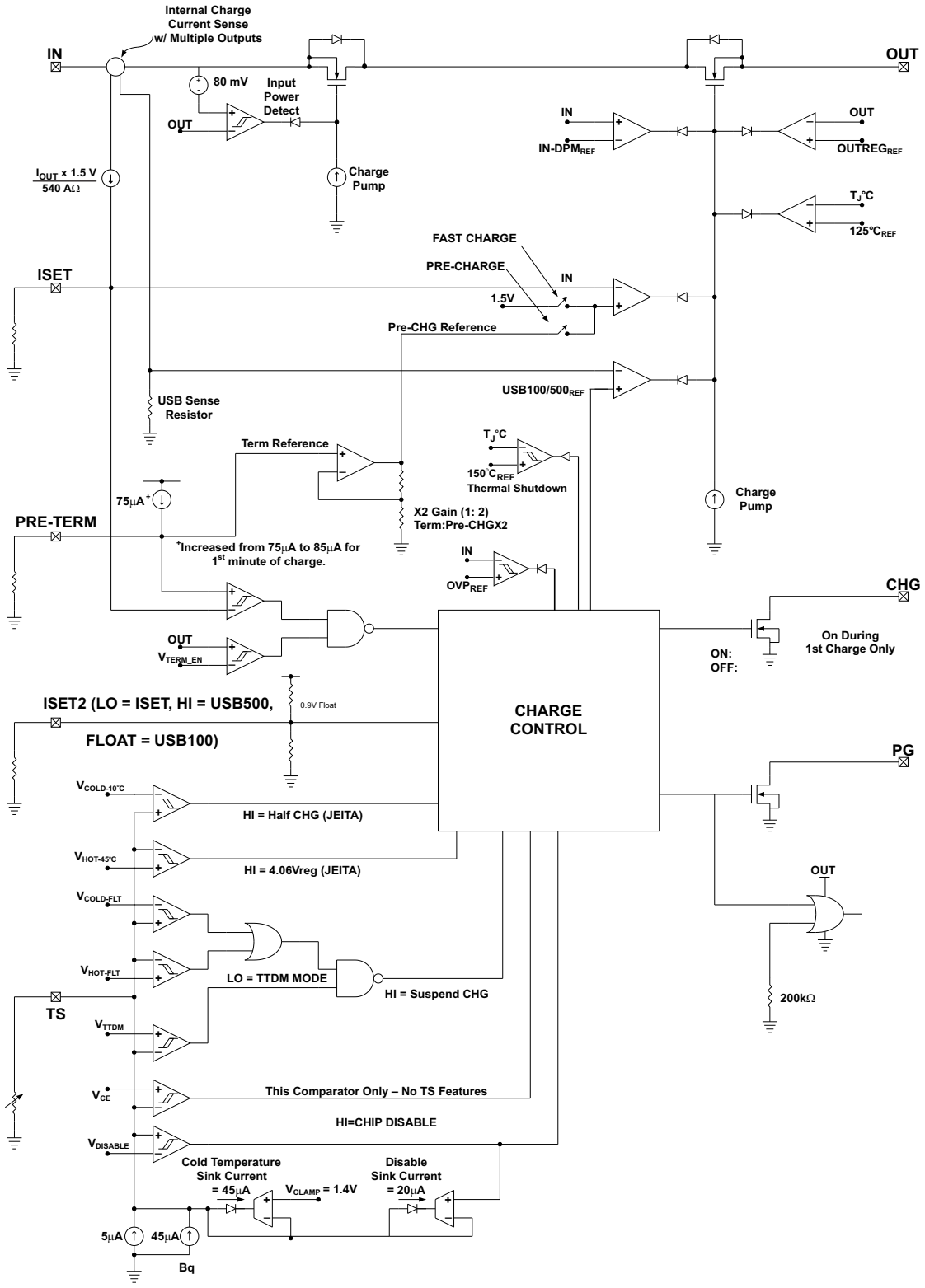
If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM terminal which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery “stealing” the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM terminal is a dual function terminal which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET terminal. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal requlation, slows the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. Figure 7 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC’s junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination can be disabled if desired. The $\overline{\text{CHG}}$ terminal is low (LED on) during the first charge cycle only and turns off once the termination threshold is reached, regardless if termination, for charge current, is enabled or disabled.

Further details are mentioned in the Operating Modes section.

7.2 Functional Block Diagram



7.3 Feature Description

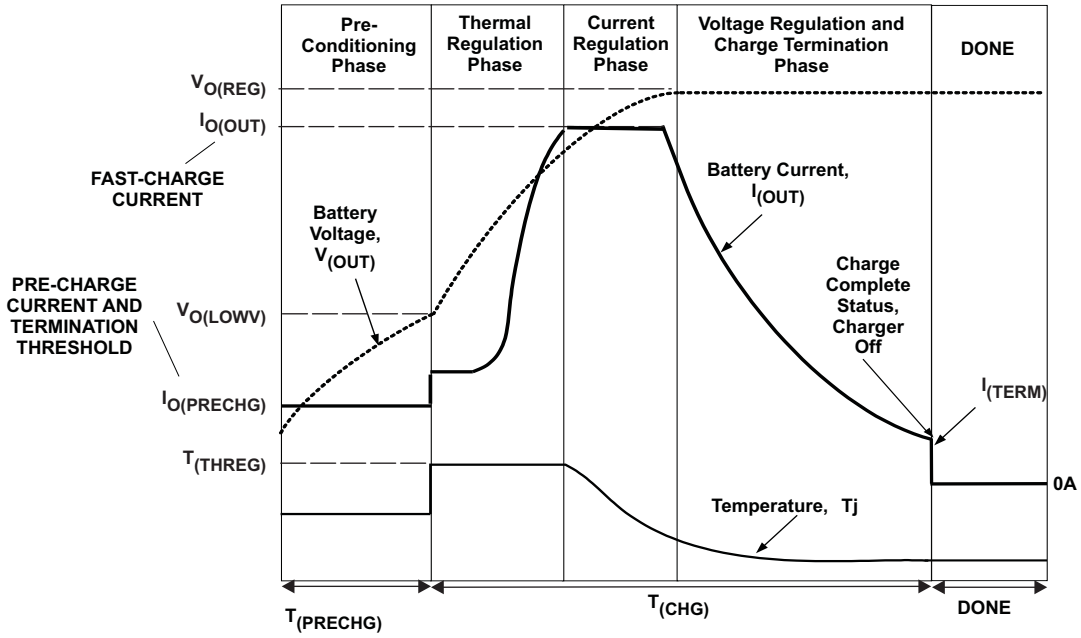


Figure 7. Charging Profile With Thermal Regulation

7.3.1 Power-Down or Undervoltage Lockout (UVLO)

The SN2040 is in power down mode if the IN terminal voltage is less than UVLO. The part is considered “dead” and all the terminals are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT terminal (battery) voltage.

7.3.2 Power-up

The IC is alive after the IN voltage ramps above UVLO (see *Sleep Mode*), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100 mA, sets the input current limit threshold base on the ISET2 terminal, starts the safety timer and enables the $\overline{CHG}$ terminal. See Figure 8.

7.3.3 Sleep Mode

If the IN terminal voltage is between than V_{OUT}+V_{DT} and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{PG}$ and $\overline{CHG}$ terminals are high impedance. As the input voltage rises and the charger exits sleep mode, the $\overline{PG}$ terminal goes low, the safety timer continues to count, charge is enabled and the $\overline{CHG}$ terminal returns to its previous state. See Figure 9.

7.3.4 New Charge Cycle

A new charge cycle is started when any of these events occur:

- A valid power source is applied;
- The chip is enabled/disabled using TS pin or BAT_EN;
- Exit of termination/Timer Disable Mode (TTDM);
- Detection of batter insertion;
- OUT voltage drops below the VRCH threshold.

The $\overline{CHG}$ signal is active only during the first charge cycle. Exiting TTDM or the OUT voltage falling below VRCH will not activate the $\overline{CHG}$ signal if it is already in the open-drain (off) state.

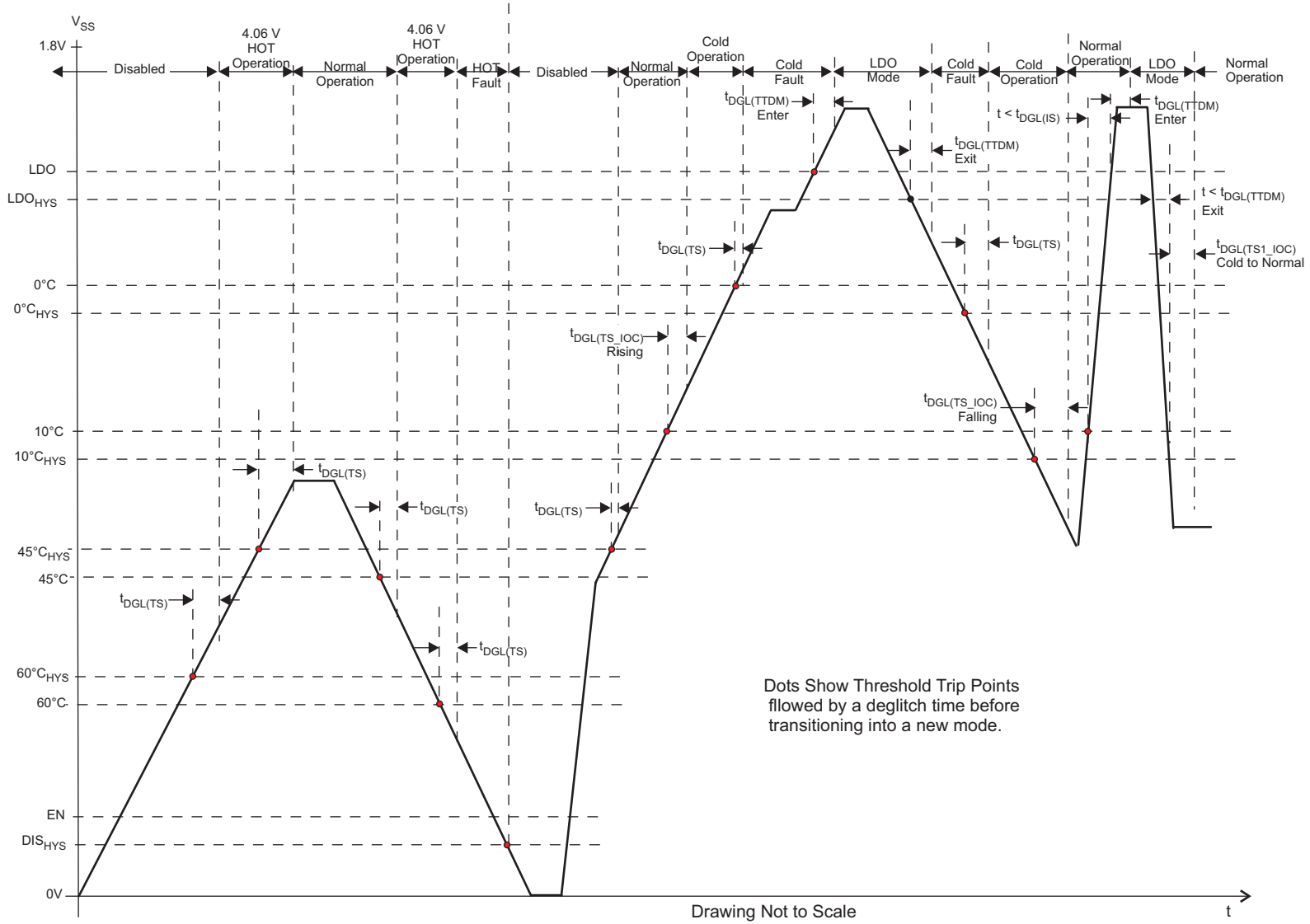


Figure 8. TS Battery Temperature Bias Threshold and Deglitch Timers

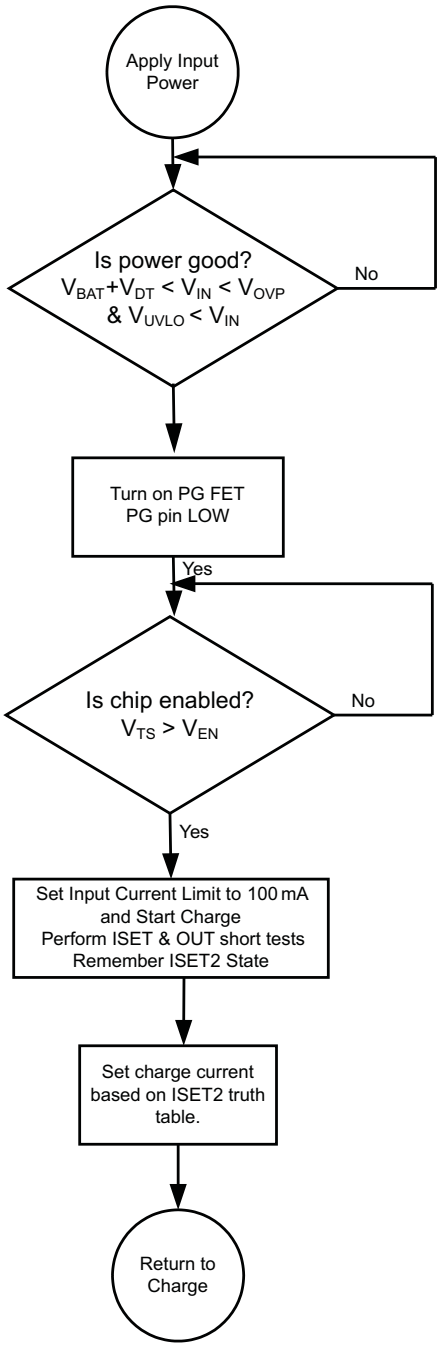


Figure 9. SN2040 Power-Up Flow Diagram

7.3.5 Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ and $\overline{PG}$ terminal goes to a high impedance state. Once the overvoltage returns to a normal voltage, the $\overline{PG}$ terminal goes low, timer continues, charge continues and the $\overline{CHG}$ terminal goes low after a 25 ms deglitch. PG terminal is optional on some packages

7.3.6 Power Good Indication ($\overline{PG}$)

After application of a 5V source, the input voltage rises above the UVLO and sleep thresholds ($V_{IN}>V_{BAT}+V_{DT}$), but is less than OVP ($V_{IN}<V_{OVP}$,), then the PG FET turns on and provides a low impedance path to ground. See Figure 19, Figure 20, and Figure 32.

7.3.7 $\overline{\text{CHG}}$ Terminal Indication

The charge terminal has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor.

The charge terminal is high impedance in sleep mode and OVP (if $\overline{\text{PG}}$ is high impedance) and return to its previous state once the condition is removed.

Cycling input power, pulling the TS terminal low and releasing or entering pre-charge mode causes the $\overline{\text{CHG}}$ terminal to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

7.4 Device Functional Modes

7.4.1 $\overline{\text{CHG}}$ and $\overline{\text{PG}}$ LED Pull-up Source

For host monitoring, a pullup resistor is used between the STATUS terminal and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the STATUS terminal and a power source. If the $\overline{\text{CHG}}$ or $\overline{\text{PG}}$ source is capable of exceeding 7 V, a 6.2 V Zener should be used to clamp the voltage. If the source is the OUT terminal, note that as the battery changes voltage, and the brightness of the LEDs vary.

Table 1.

CHARGING STATE	$\overline{\text{CHG}}$ FET/LED
First charge after VIN applied	ON
Refresh charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

Table 2.

V_{IN} POWER GOOD STATE	$\overline{\text{PG}}$ FET/LED
UVLO	OFF
SLEEP mode	
OVP mode	
Normal input ($V_{OUT} + V_{DT} < V_{IN} < V_{OUP}$)	ON
PG is independent of chip disable	

7.4.2 IN-DPM (V_{IN-DPM} or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out terminal. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3 V and 4.4 V respectively. This is an added safety feature that helps protect the source from excessive loads.

7.4.3 OUT

The Charger's OUT terminal provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT terminal is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

7.4.4 ISET

An external resistor is used to Program the Output Current (50 to 1000 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} / I_{OUT} \quad (1)$$

where

- I_{OUT} is the desired fast charge current;
- K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Figure 1 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15 A.

The ISET resistor is short protected and will detect a resistance lower than ≠340 Ω. The detection requires at least 80 mA of output current. If a “short” is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.05 A and 1.4 and is independent of the ISET short detection circuitry, as shown in Figure 11. Also, see Figure 27 and Figure 28.

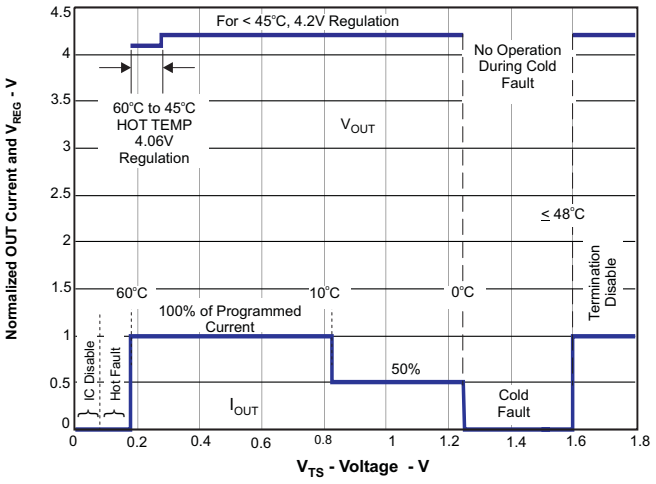


Figure 10. Operation Over TS Bias Voltage

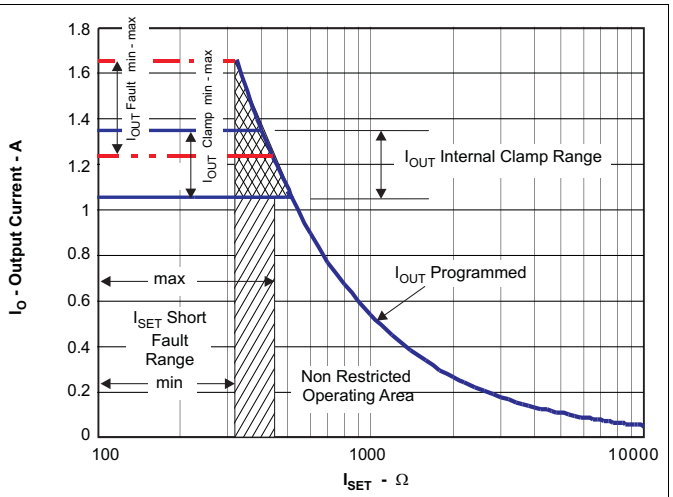


Figure 11. Programmed/Clamped Out Current

7.4.5 PRE_TERM – Pre-Charge and Termination Programmable Threshold

Pre-Term is used to program both the pre-charge current and the termination current threshold. The pre-charge current level is a factor of two higher than the termination current level. The termination can be set between 5 and 50% of the programmed output current level set by ISET. If left floating the termination and pre-charge are set internally at 10/20% respectively. The pre-charge-to-fast-charge, V_{lowv} threshold is set to 2.5V.

$$R_{PRE\text{-}TERM} = \%Term \times K_{TERM} = \%Pre\text{-}CHG \times K_{PRE\text{-}CHG} \quad (2)$$

where

- %Term is the percent of fast charge current where termination occurs;
- %Pre-CHG is the percent of fast charge current that is desired during precharge;
- K_{TERM} and $K_{PRE\text{-}CHG}$ are gain factors found in the electrical specifications.

7.4.6 ISET2

ISET2 is a 3-state input and programs the Input Current Limit/Regulation Threshold. A low will program a regulated fast charge current via the ISET resistor and is the maximum allowed input/output current for any ISET2 setting, Float will program a 100 mA Current limit and High will program a 500 mA Current limit.

Below are two configurations for driving the 3-state ISET2 terminal:

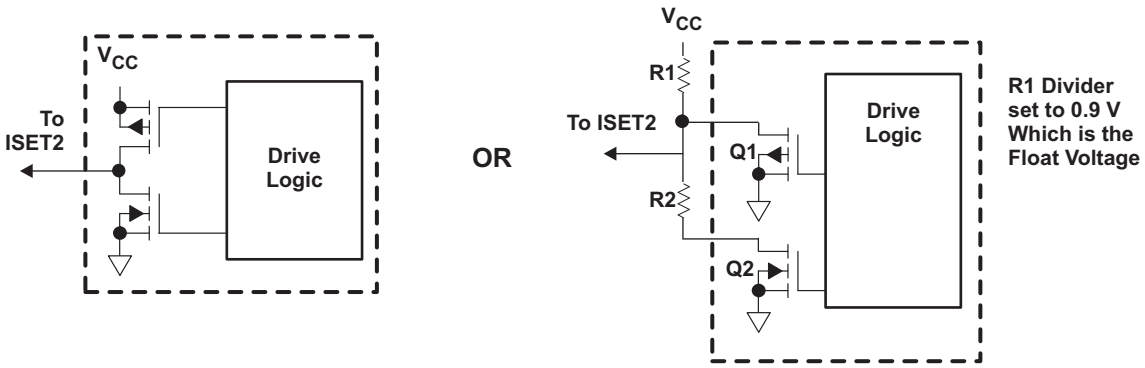


Figure 12. 3-State ISET2 Terminal Circuits

7.4.7 TS

The TS function for the device is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1 Vmax, see Figure 10.

The TS feature is implemented using an internal 50 μA current source to bias the thermistor (designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS terminal to V_{SS}. If this feature is not needed, a fixed 10 kΩ can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS terminal low to disable charge.

The TS terminal has two additional features, when the TS terminal is pulled low or floated/driven high. A low disables charge and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disabled. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM mode. If the TS terminal is pulled low into disable mode, the current is reduce to ≠30 μA, see Figure 8. Since the I_{TS} curent is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10 k NTC (at 25°C).

7.4.8 Termination and Timer Disable Mode (TTDM) - TS Terminal High

The battery charger is in TTDM when the TS terminal goes high from removing the thermistor (removing battery pack/floating the TS terminal) or by pulling the TS terminal up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ terminal will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ terminal does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ terminal goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237-k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS terminal into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

7.4.9 Timers

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{CHG}$ terminal goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power or going into and out of TTDM.

7.4.10 Termination

Once the OUT terminal goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, the $\overline{CHG}$ terminal goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS terminal is driven high and the charge enters TTDM. If the battery was removed and the TS terminal is held in the active region, then the battery detect routine will continue until a battery is inserted.

7.4.11 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT terminal at a useable voltage. Whenever the battery is missing the $\overline{CHG}$ terminal should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See Figure 13 for the Battery Detect Flow Diagram.

7.4.12 Refresh Threshold

After termination, if the OUT terminal voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ terminal remains at a high impedance (off).

7.4.13 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

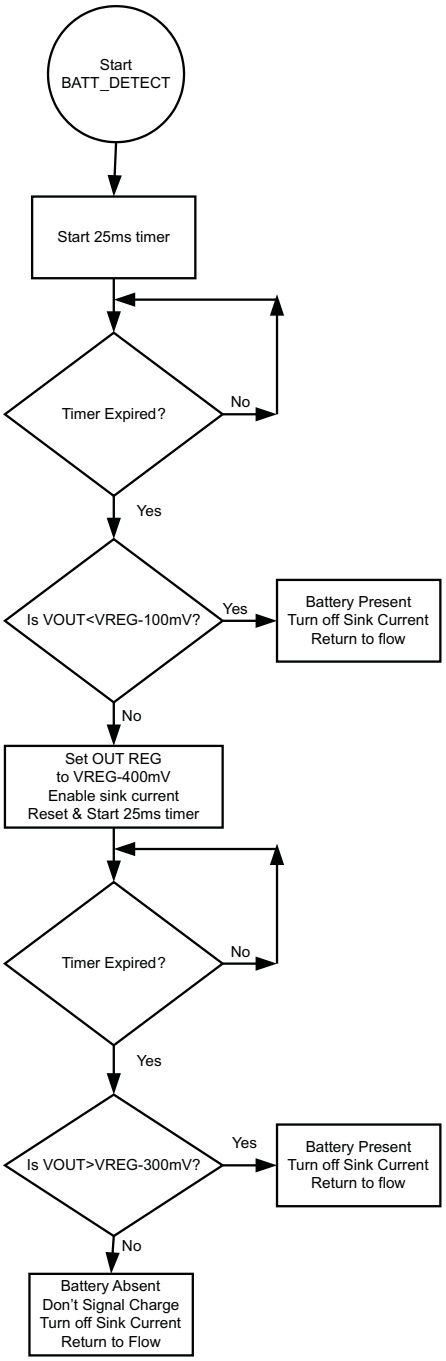


Figure 13. Battery Detect Routine

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN2040 series of devices are highly integrated Li-Ion and Li-Pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters. These devices have a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

8.2 Typical Applications

8.2.1 Typical Application

$I_{OUT\_FAST\_CHG}$ = 540 mA; $I_{OUT\_PRE\_CHG}$ = 108 mA; I_{OUT_TERM} = 54 mA

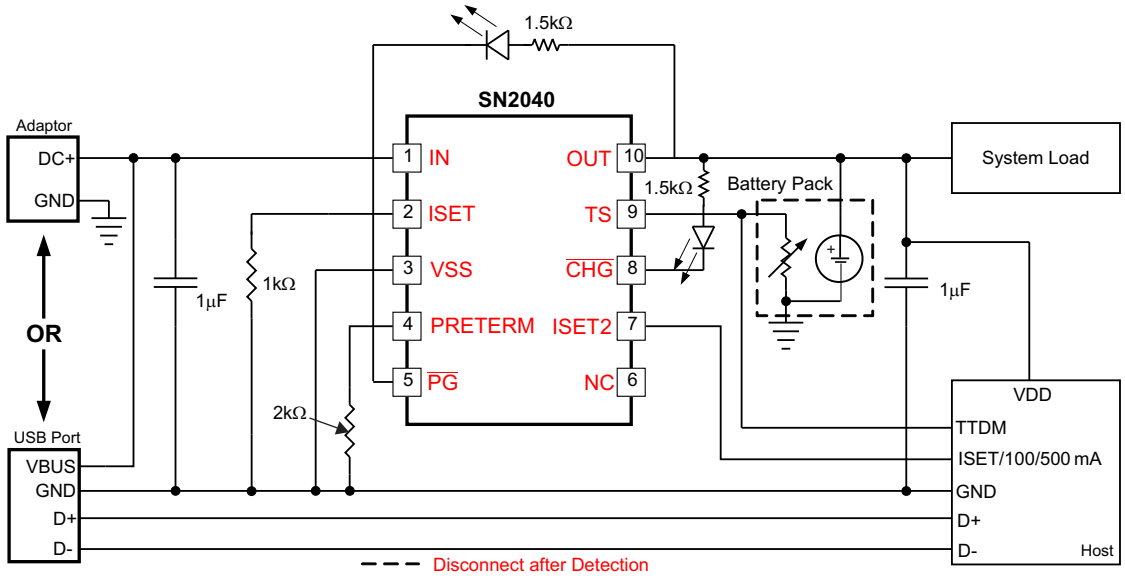


Figure 14. Typical Application Circuit

8.2.1.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: $I_{OUT\text{-}FC}$ = 540 mA; ISET-terminal 2
- Termination Current Threshold: $\%_{IOUT\text{-}FC}$ = 10% of Fast Charge or about 54 mA
- Pre-Charge Current by default is twice the termination Current or about 108 mA
- TS – Battery Temperature Sense = 10 k NTC (103AT)

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Calculations

8.2.1.2.1.1 Program the Fast Charge Current, ISET:

$$R_{ISET} = [K_{(ISET)} / I_{(OUT)}] \quad (3)$$

From the *Electrical Characteristics* table:

- $K_{(SET)}$ = 540 AΩ
- R_{ISET} = [540 AΩ/0.54A] = 1 kΩ

Selecting the closest standard value, use a 1 kΩ resistor between ISET (terminal 16) and VSS.

8.2.1.2.1.2 Program the Termination Current Threshold, ITERM:

$$R_{PRE\text{-}TERM} = K_{(TERM)} \times \%_{IOUT\text{-}FC} \quad (4)$$

$$R_{PRE\text{-}TERM} = 200\ \Omega/\% \times 10\% = 2\ k\Omega \quad (5)$$

Selecting the closest standard value, use a 2 kΩ resistor between ITERM (terminal 15) and VSS.

One can arrive at the same value by using 20% for a pre-charge value (factor of 2 difference).

$$R_{PRE\text{-}TERM} = K_{(PRE\text{-}CHG)} \times \%_{IOUT\text{-}FC} \quad (6)$$

$$R_{PRE\text{-}TERM} = 100\ \Omega/\% \times 20\% = 2\ k\Omega \quad (7)$$

8.2.1.2.1.3 TS Function

Use a 10k NTC thermistor in the battery pack (103AT).

To Disable the temp sense function, use a fixed 10k resistor between the TS (terminal 1) and VSS.

8.2.1.2.1.4 $\overline{CHG}$ and PG

LED Status: connect a 1.5-k resistor in series with a LED between the OUT terminal and the $\overline{CHG}$ terminal. Connect a 1.5k resistor in series with a LED between the OUT terminal and the and PG terminal.

Processor Monitoring: Connect a pull-up resistor between the processor's power rail and the $\overline{CHG}$ terminal. Connect a pull-up resistor between the processor's power rail and the PG terminal.

8.2.1.2.2 Selecting In and Out Terminal Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power terminal, input and output terminals. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30 V transient (verify tested rating with capacitor manufacturer).

Typical Applications (continued)

8.2.1.3 Application Curves

SETUP: typical applications schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise indicated)

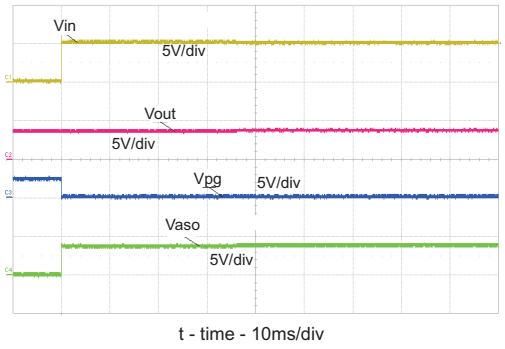


Figure 15. Power-up Timing

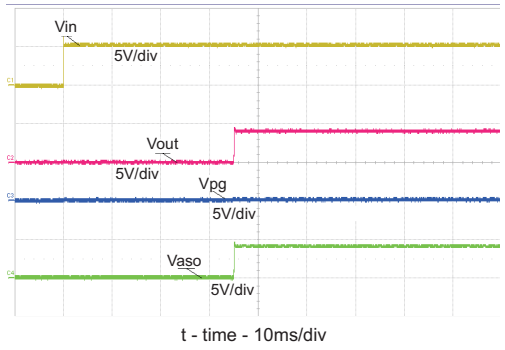


Figure 16. Power-up Timing – No Battery or Load

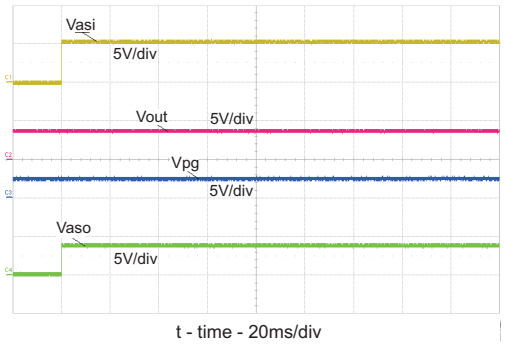


Figure 17. – ASI and OUT Power-up Timing – No Input

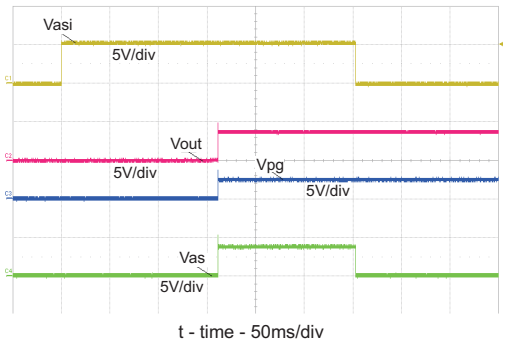


Figure 18. ASI and delayed OUT Power-up Timing – No Input

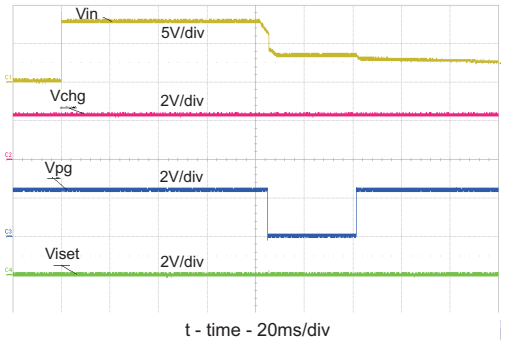


Figure 19. OVP 8V Adaptor - Hot Plug

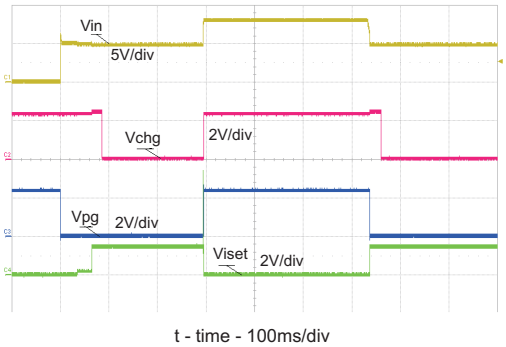
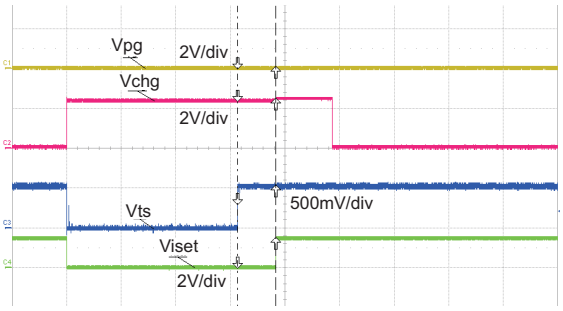


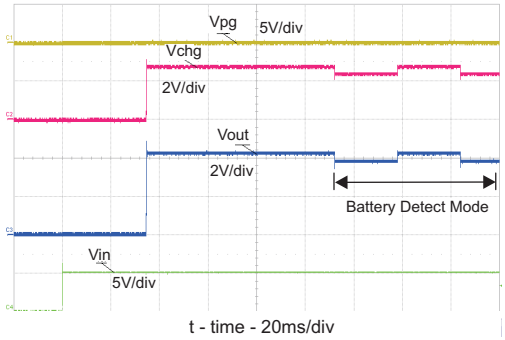
Figure 20. OVP from Normal Power-up Operation – V_{IN} 0 V → 5 V → 8 V →5 V

Typical Applications (continued)



.

Figure 21. TS Enable and Disable



Fixed 10kΩ resistor, between TS and GND.

Figure 22. Hot Plug Source w/No Battery – Battery Detection

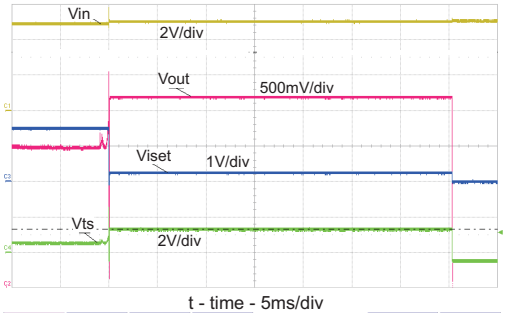


Figure 23. Battery Removal – GND Removed 1st, 42 Ω Load

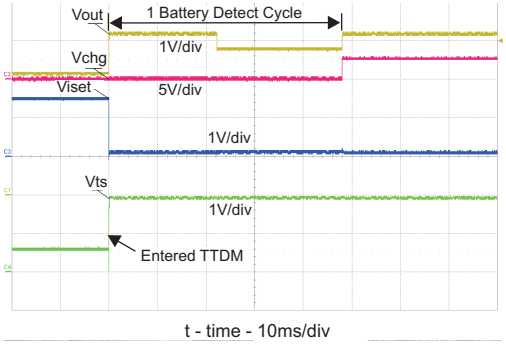
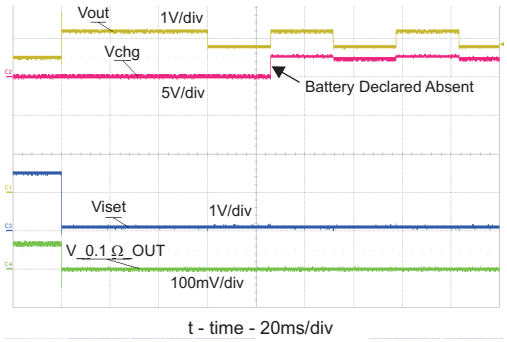
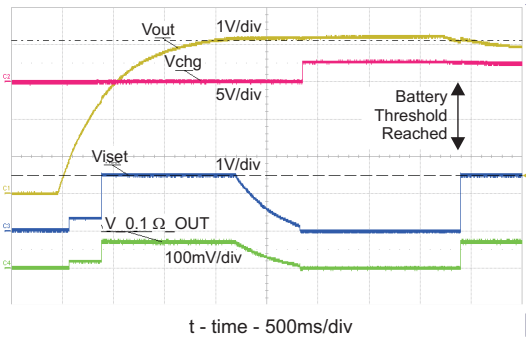


Figure 24. Battery Removal with OUT and TS Disconnect 1st, With 100 Ω Load



Continuous battery detection when not in TTDM

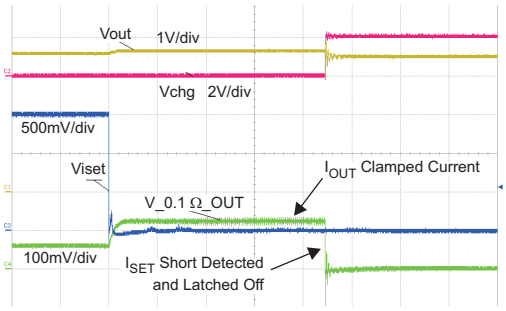
Figure 25. Battery Removal with fixed TS = 0.5 V



CH4: I_{OUT} (1 A/Div)
Battery voltage swept from 0V to 4.25 V to 3.9 V.

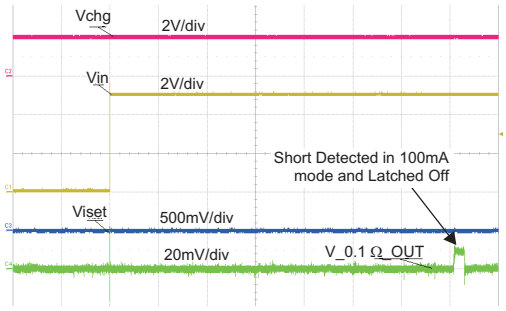
Figure 26. Battery Charge Profile

Typical Applications (continued)



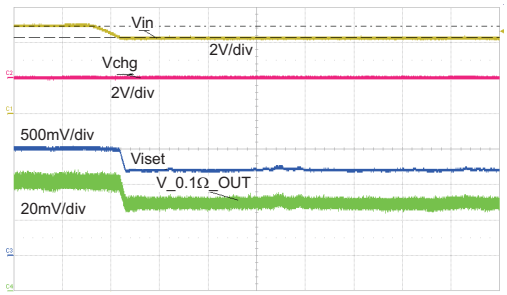
CH4: I_{OUT} (1 A/Div)

Figure 27. ISET Shorted During Normal Operation



CH4: I_{OUT} (0.2 A/Div)

Figure 28. ISET Shorted Prior to USB Power-up



CH4: I_{OUT} (0.2 A/Div)

Figure 29. DPM – Adaptor Current Limits – V_{IN} Regulated

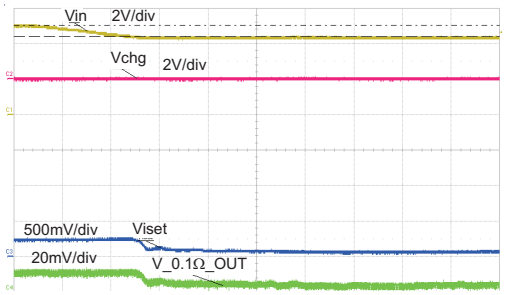
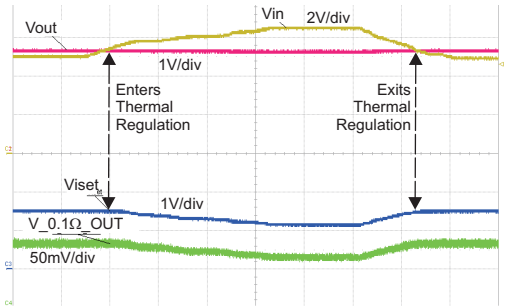


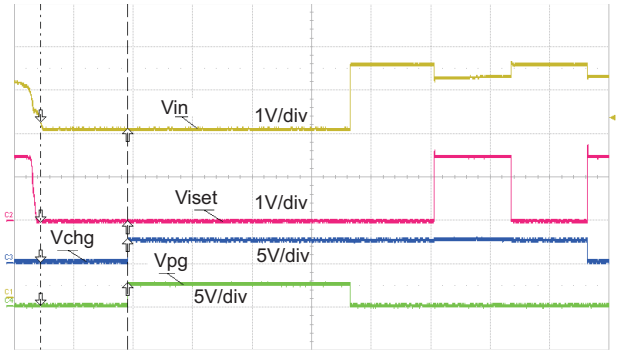
Figure 30. DPM – USB Current Limits – V_{IN} Regulated to 4.4 V



The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C. VIN is reduced, the IC temperature drops, the charge current returns to the programmed value

.

Figure 31. Thermal Reg. – V_{IN} increases PWR/Iout Reduced



V_{IN} swept from 5 V to 3.9 V to 5 V V_{BAT} = 4V

Figure 32. Entering and Exiting Sleep mode

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the device IN and GND terminals, a larger capacitor is recommended.

10 Layout

10.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the device, with short trace runs to both IN, OUT, and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN terminal and from the OUT terminal must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The SN2040 family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10mil vias in the power pad of the IC and close enough to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that “cut off” the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8mil thick) copper on top and bottom, and is a good example of optimal thermal performance.

10.2 Layout Example

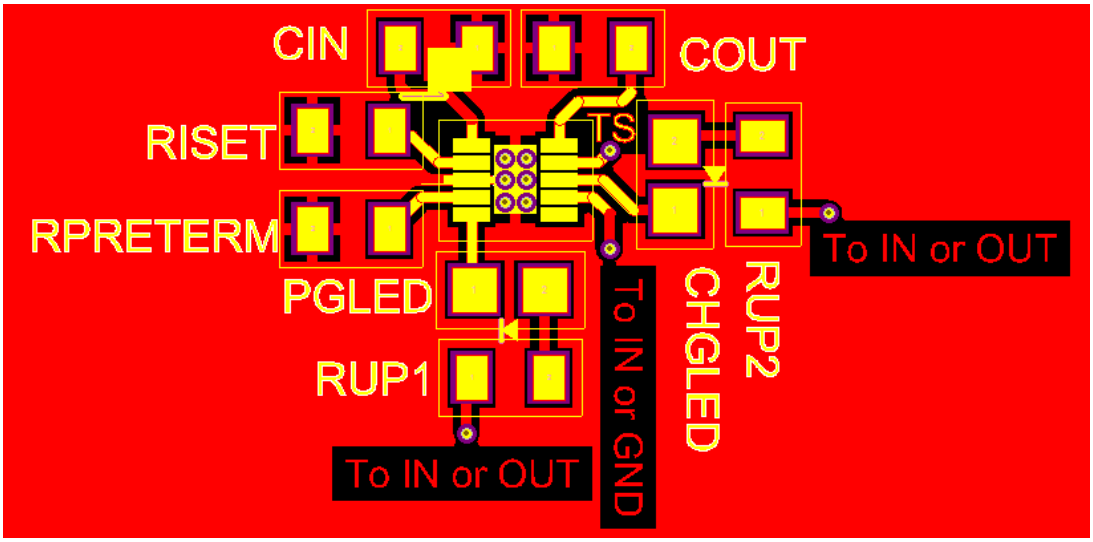


Figure 33. Board Layout

10.3 Thermal Considerations

The SN2040 family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS terminal. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment* Application Note (SLUA271). The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for $R_{\theta JA}$ is:

$$R_{\theta JA} = (T_J – T) / P$$

where

- T_J = Chip junction temperature
- T = Ambient temperature
- P = Device power dissipation (8)

Factors that can influence the measurement and calculation of $R_{\theta JA}$ include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} – V_{(BAT)}] \times I_{(BAT)} \quad (9)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

10.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75 AHr battery and a 10 μA leakage current (750 mAHr / 0.010 mA = 75000 hours), it would take 75k hours or 8.8 years to discharge. In reality the self discharge of the cell would be much faster so the 10 μA leakage would be considered negligible.

11 Device and Documentation Support

11.1 Documentation Support

QFN/SON PCB Attachment Application Report, SLUA271

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
SN2040DSQR	ACTIVE	WSON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	NXE
SN2040DSQT	ACTIVE	WSON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	NXE

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

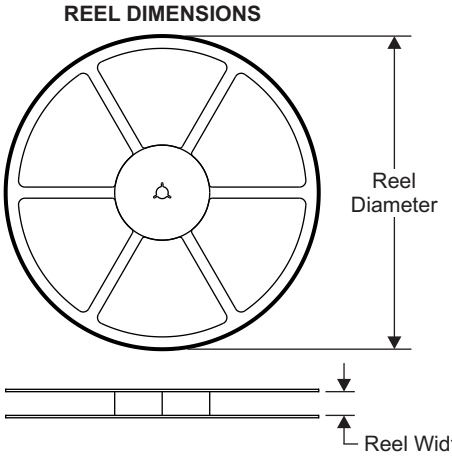
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

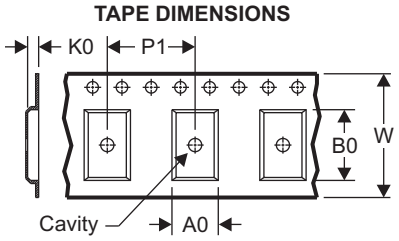
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

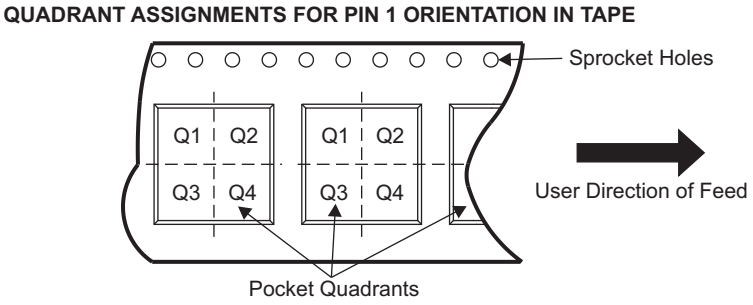
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information



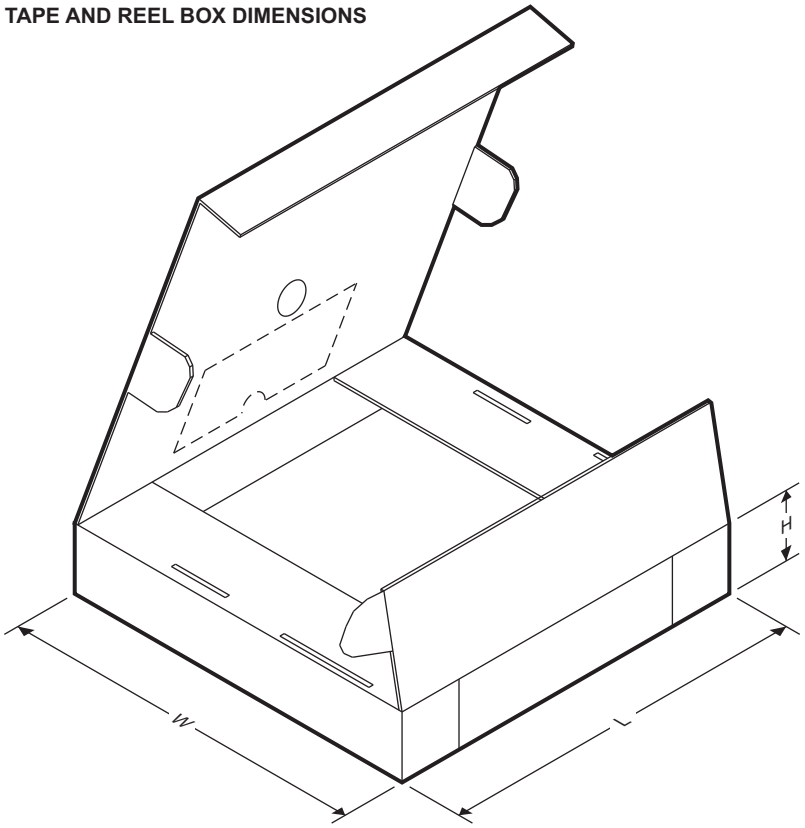


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN2040DSQR	WSON	DSQ	10	3000	180	8.4	2.3	2.3	1.15	4.0	8.0	Q2
SN2040DSQT	WSON	DSQ	10	250	180	8.4	2.3	2.3	1.15	4.0	8.0	Q2

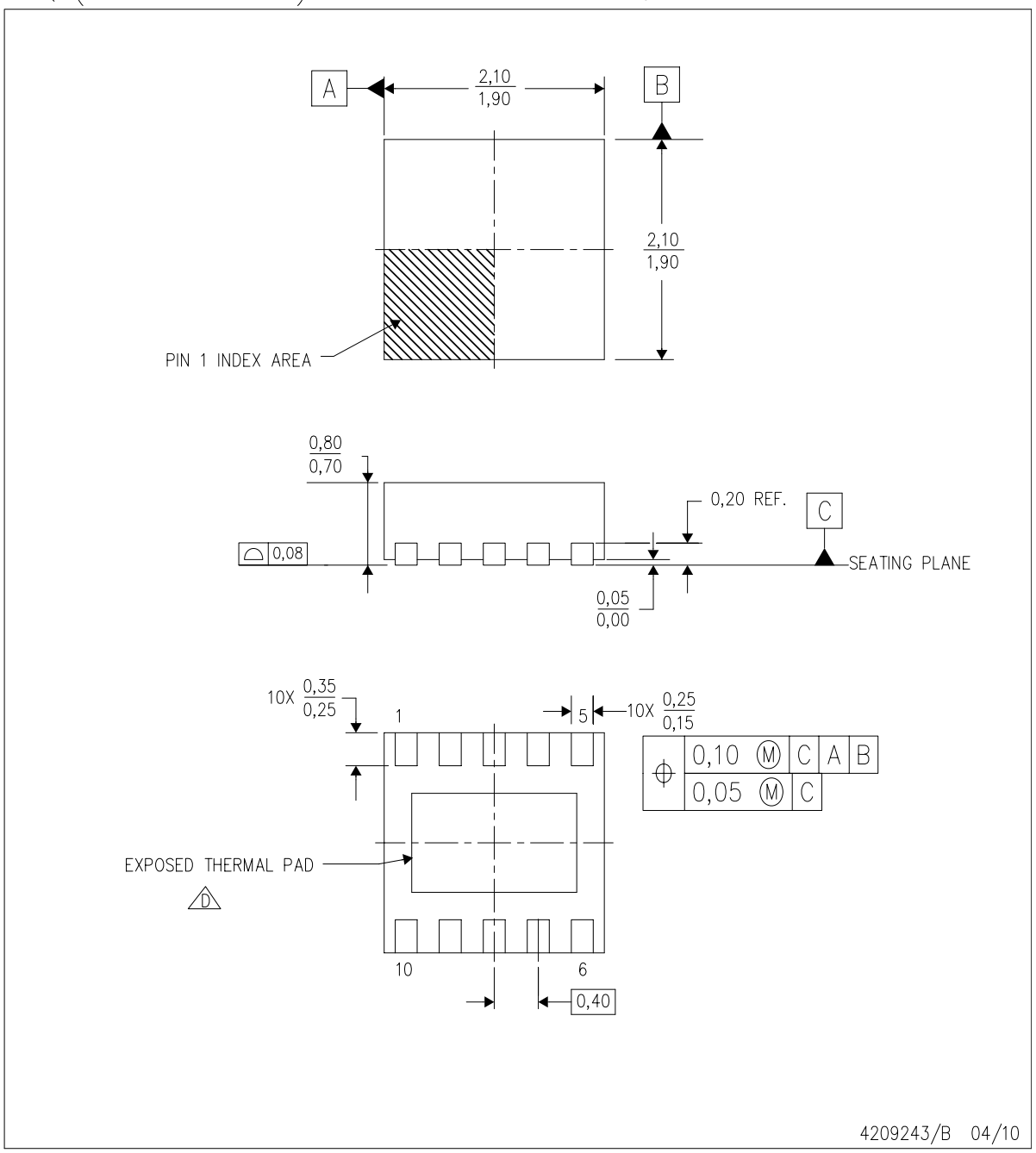
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN2040DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
SN2040DSQT	WSON	DSQ	10	250	210.0	185.0	35.0

MECHANICAL DATA

DSQ (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

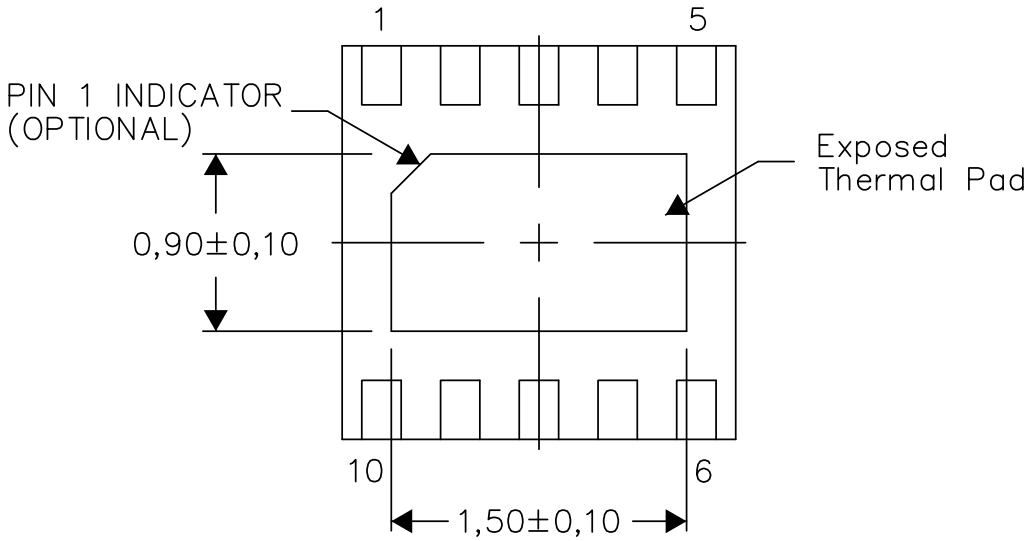
DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

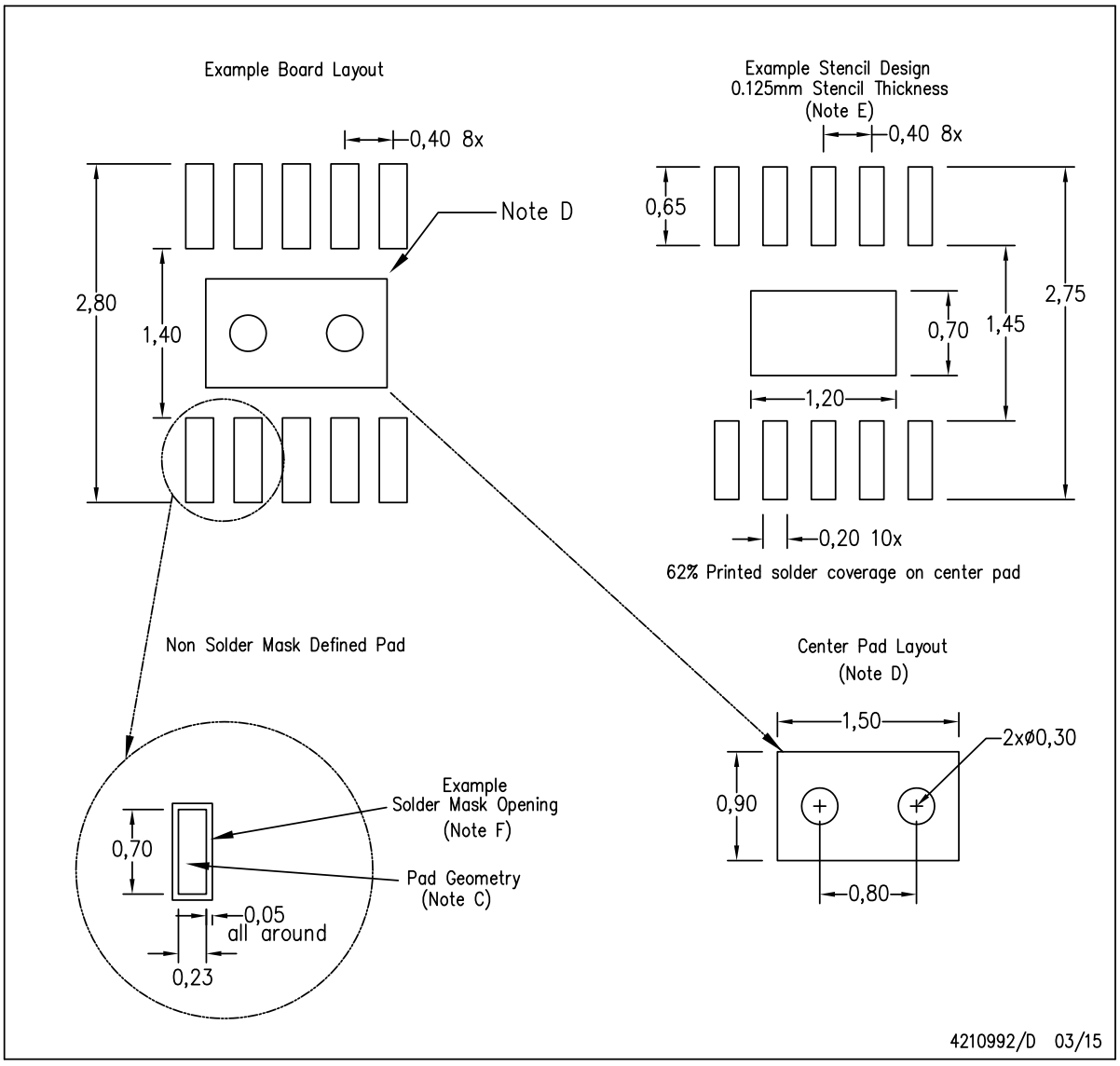
Exposed Thermal Pad Dimensions

4210993/E 06/15

NOTES: A. All linear dimensions are in millimeters

LAND PATTERN DATA

DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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