N-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM3400 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.1V. This device is suitable for use as a load switch or in PWM applications. Standard Product LPM3400 is Pb-free.

Features

- 20V/5A, $R_{DS(ON)}$ < 33mΩ(max.)@VGS=4.5V
- 20V/4A, $R_{DS(ON)}$ < 52mΩ(max.)@VGS=2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOT23 Package

Order Information

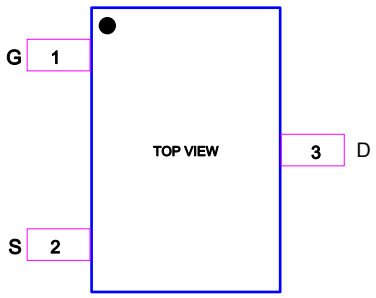
LPM3400 □ □ □

- F: Pb-Free
- Package Type: B3: SOT23

Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power Switch
- Load Switch
- Charging

Pin Configurations



Marking Information

Device	Marking	Package	Shipping
LPM340B3F	A2SXX	SOT23	3K

Absolute Maximum Ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	TA=25℃	I_D	5.8	A
	TA=70℃		4.9	
Pulsed Drain Current		I_{DM}	30	
Power Dissipation	TA=25℃	P_D	1.4	W
	TA=70℃		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal resistance ratings

Parameter	Symbol	MAX	Unit
Junction-to-Case Thermal Resistance	$R_{\theta JA}$	125	℃/W

Electrical Characteristics

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.7	1.1	1.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5.8A		22	28	mΩ
		V_{GS}=4.5V, I_D=5A		27	33	
		V_{GS}=2.5V, I_D=4A		43	52	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=5A	10	15		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		400		pF
C_{oss}	Output Capacitance			99		pF
C_{rss}	Reverse Transfer Capacitance			77		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.2	3.6	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=5.8A		9.7		nC
Q_g(4.5V)	Total Gate Charge			1.6		nC
Q_{gs}	Gate Source Charge			3.1		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=15V, R_L=2.7Ω,R_{GEN}=3Ω		3.3		ns
t_r	Turn-On Rise Time			4.8		ns
$t_{D(off)}$	Turn-Off Delay Time			26.3		ns
tf	Turn-Off Fall Time			4.1		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5A, dI/dt=100A/μs		16		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5A, dI/dt=100A/μs		8.9		nC

Typical Characteristics

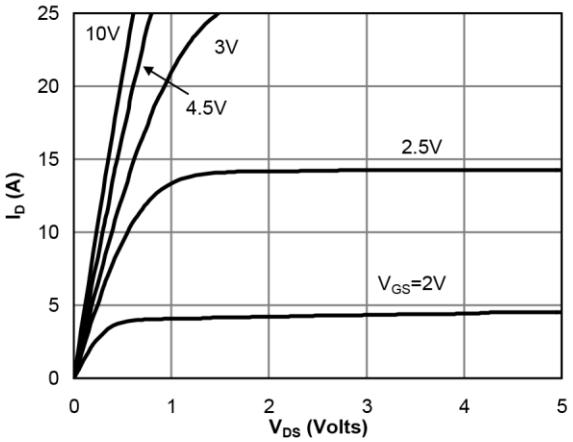


Fig 1: On-Region Characteristics

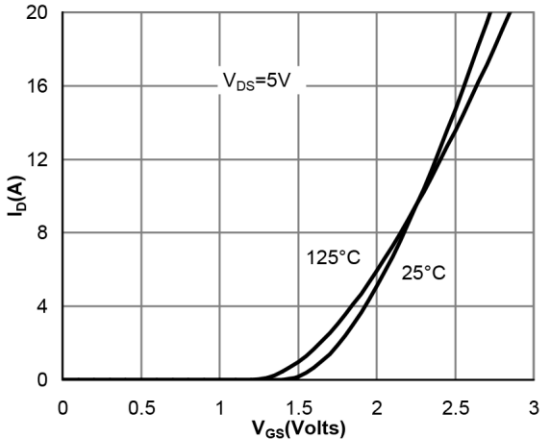


Figure 2: Transfer Characteristics

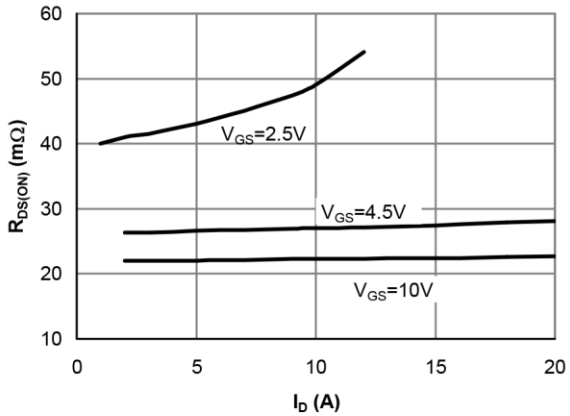


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

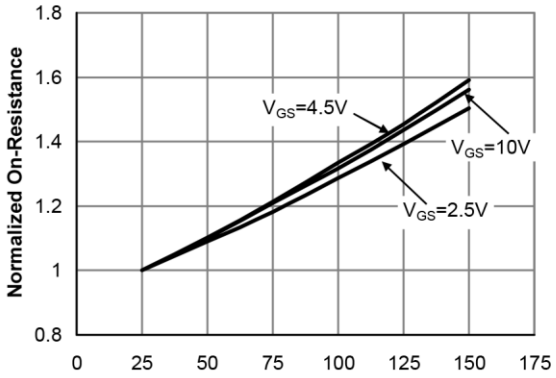


Figure 4: On-Resistance vs. Junction Temperature

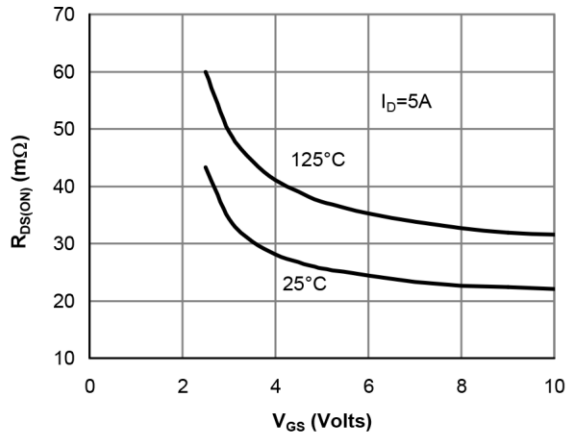


Figure 5: On-Resistance vs. Gate-Source Voltage

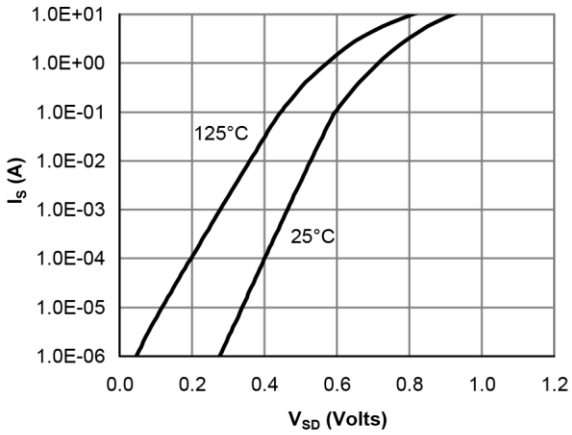


Figure 6: Body-Diode Characteristics

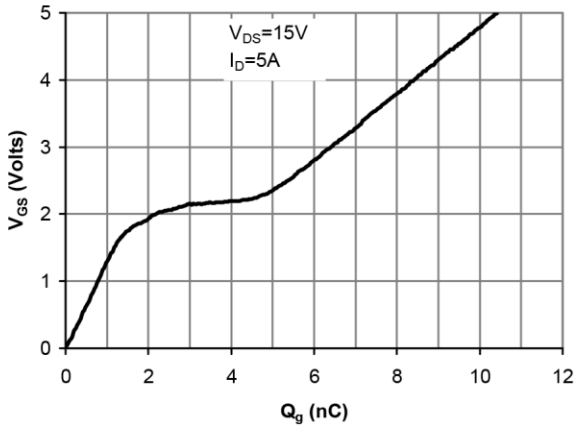


Figure 7: Gate-Charge Characteristics

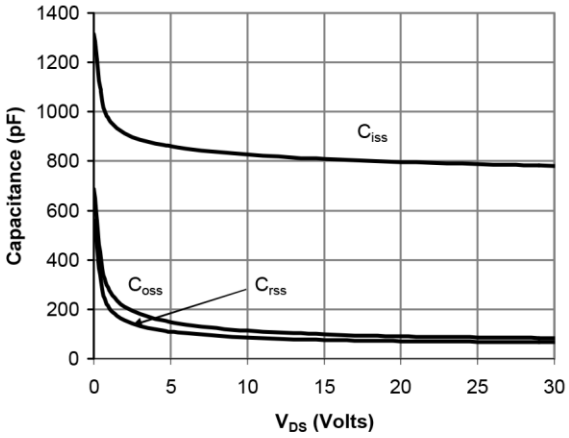


Figure 8: Capacitance Characteristics

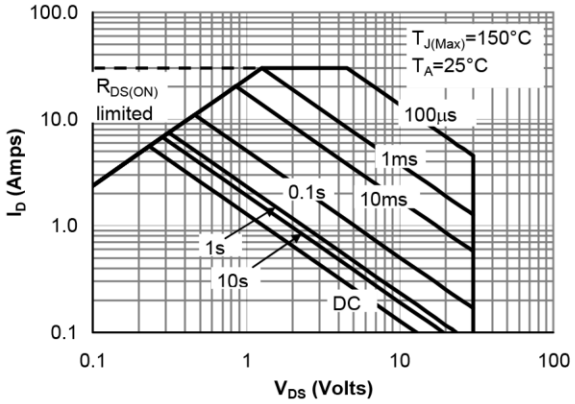


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

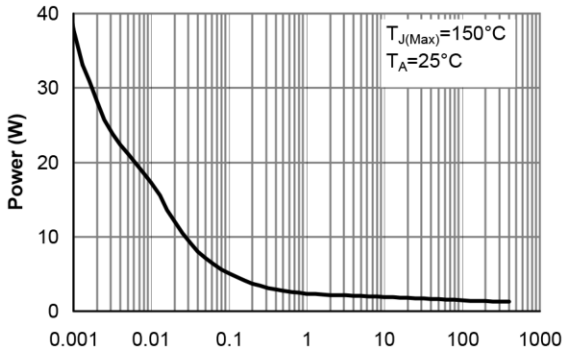


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

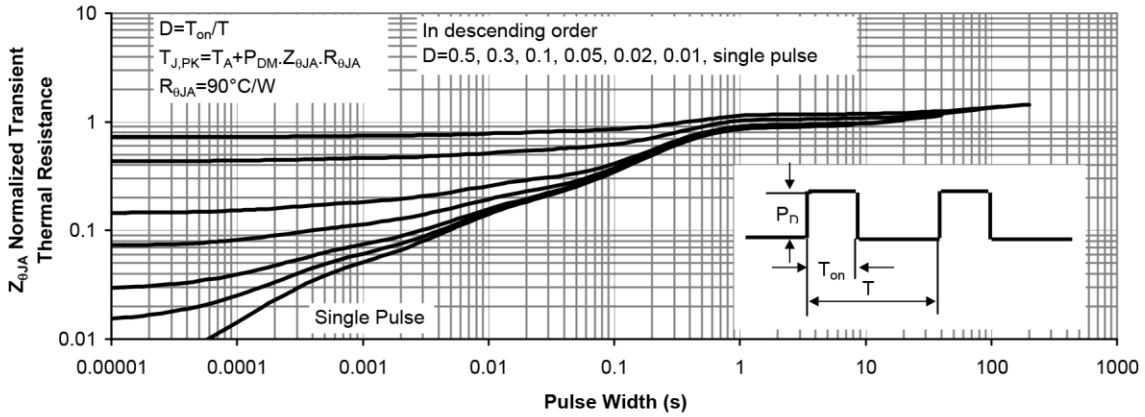
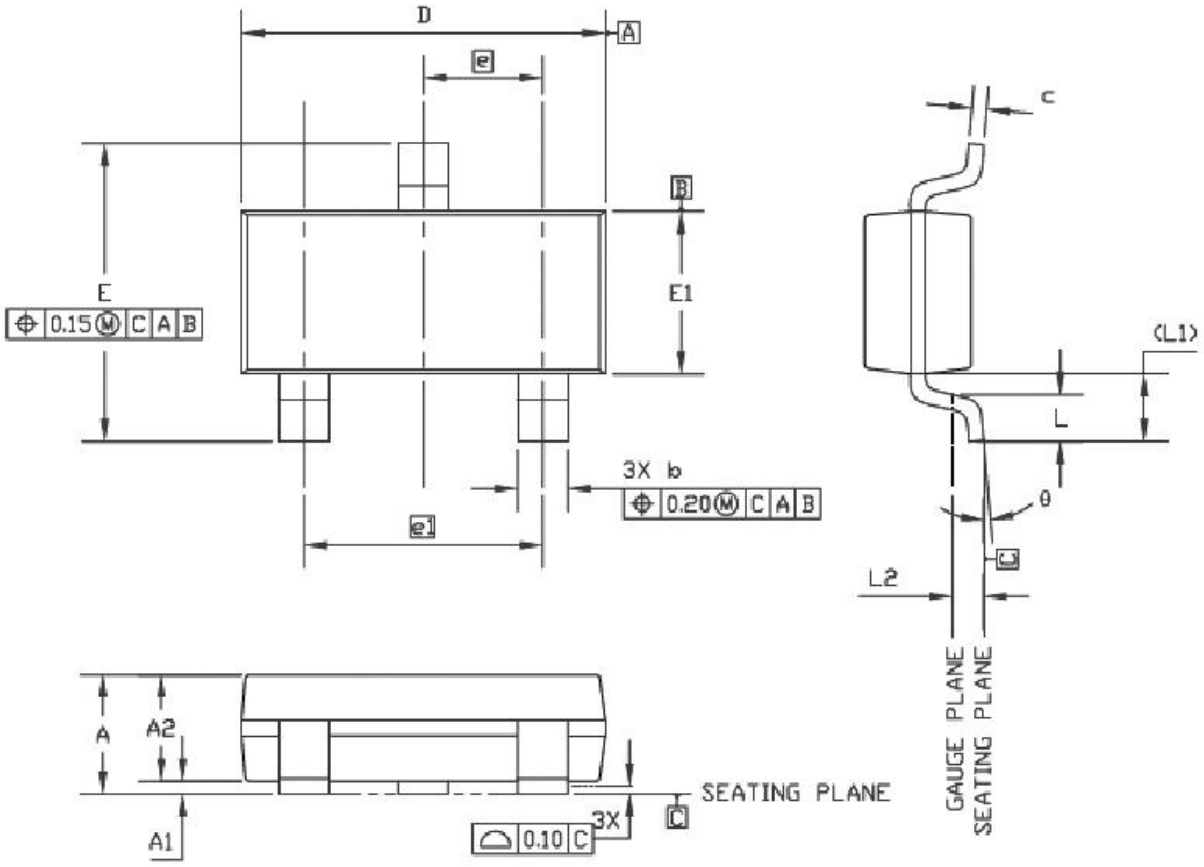


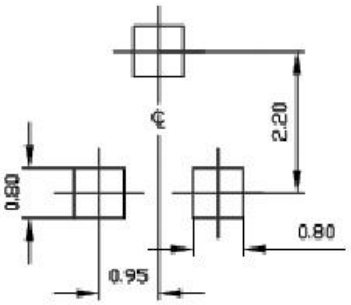
Figure 11: Normalized Maximum Transient Thermal Impedance

Packaging Information

SOT–23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°