

DIO1644

2:1 MIPI D-PHY (1.5Gbps) 4-Data Lane Switch

Features

Switch Type	SPDT (10x)
Signal Types	MIPI, D-PHY
V _{CC}	1.65 to 4.5V
Input Signals	0 to V _{CC}
R _{ON}	6Ω Typical HS MIPI 8Ω Typical LP MIPI
Δ R _{ON}	0.6Ω Typical HS & LP MIPI
R _{ON_FLAT}	0.3Ω Typical
I _{CCZ}	0.5μA Maximum
I _{CC}	45μA Maximum
O _{IRR}	-22dB Typical
X _{TALK}	-30dB Typical
Bandwidth	1500MHz Minimum
Channel-to-Channel Skew	6ps Typical
C _{ON}	4.2pF
Operating Temperature	-40 to +85°C
Package	36-Ball WLCSP

Descriptions

The DIO1644 is a four-data-lane, MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The DIO1644 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Applications

- Cellular Phones, Smart Phones
- Displays

Typical Application

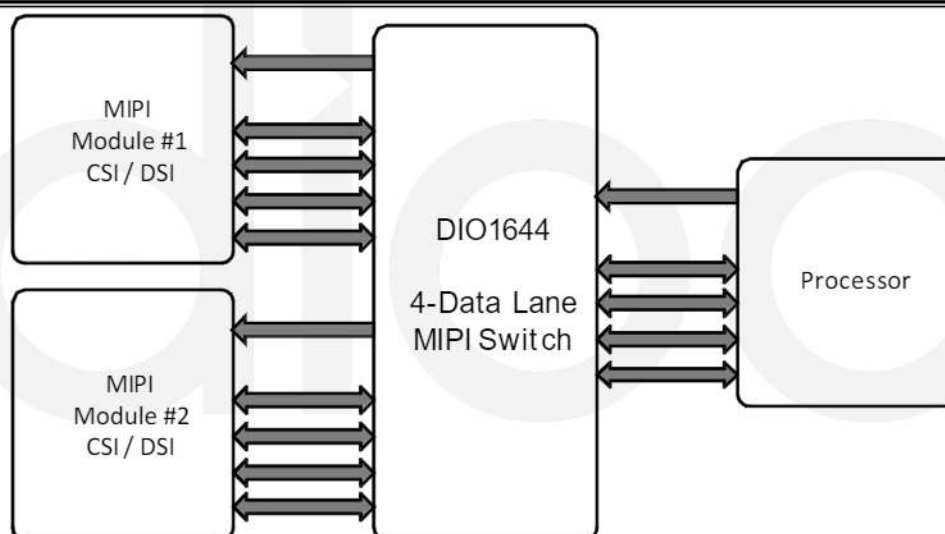


Figure 1 Typical Application

Ordering Information

Order Part Number	Top Marking		T _A	Package	
DIO1644WL36	1644	Green	-40 to +85°C	WLCSP-36 0.4mm pitch	Tape & Reel, 3000

Pin Descriptions

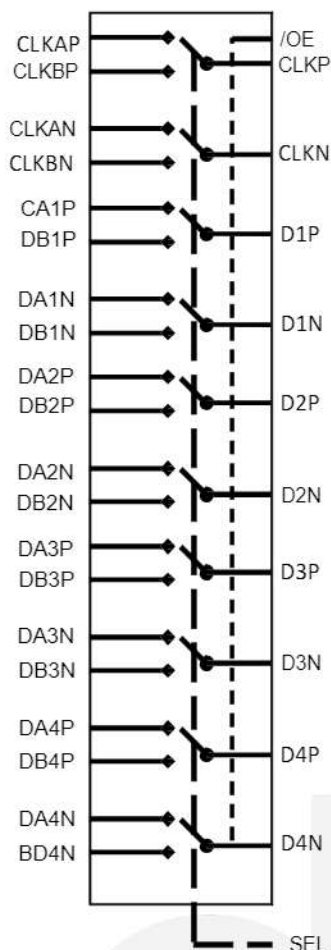


Figure 2 Analog Symbol

Pin Name		Description	
CLK _{P/N}		Common Clock Path	
D1 _{P/N}		Common Data Path 1	
D2 _{P/N}		Common Data Path 2	
D3 _{P/N}		Common Data Path 3	
D4 _{P/N}		Common Data Path 4	
CLKA _{P/N}		A-Side Clock Path	
DA1 _{P/N}		A-Side Data Path 1	
DA2 _{P/N}		A-Side Data Path 2	
DA3 _{P/N}		A-Side Data Path 3	
DA4 _{P/N}		A-Side Data Path 4	
CLKB _{P/N}		B-Side Clock Path	
DB1 _{P/N}		B-Side Data Path 1	
DB2 _{P/N}		B-Side Data Path 2	
DB3 _{P/N}		B-Side Data Path 3	
DB4 _{P/N}		B-Side Data Path 4	
SEL	Control Pin	SEL=0	CLKP=CLKAP, CLKN=CLKAN Dn(P/N)=DAn(P/N)
		SEL=1	CLKP=CLKBP, CLKN=CLKBN Dn(P/N)=DBn(P/N)
/OE	Output Enable		
V _{CC}	Power		
GND	Ground		
NC	No Connect		

Pin Definitions

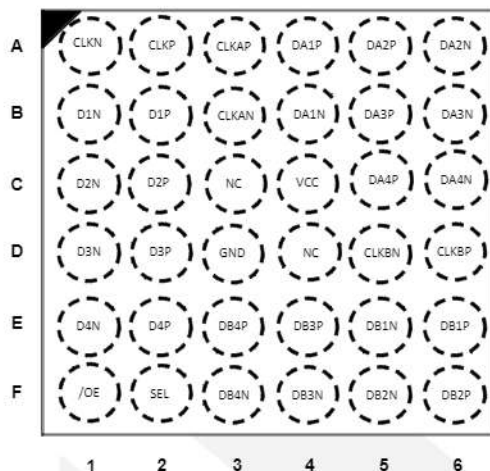


Figure 3 Top Through View

Ball	Pin Name	Ball	Pin Name
A1	CLK _N	D1	D3 _N
A2	CLK _P	D2	D3 _P
A3	CLKA _P	D3	GND
A4	DA1 _P	D4	NC
A5	DA2 _P	D5	CLKB _N
A6	DA2 _N	D6	CLKB _P
B1	D1 _N	E1	D4 _N
B2	D1 _P	E2	D4 _P
B3	CLKA _N	E3	DB4 _P
B4	DA1 _N	E4	DB3 _P
B5	DA3 _P	E5	DB1 _N
B6	DA3 _N	E6	DB1 _P
C1	D2 _N	F1	/OE
C2	D2 _P	F2	SEL
C3	NC	F3	DB4 _N
C4	V _{CC}	F4	DB3 _N
C5	DA4 _P	F5	DB2 _N
C6	DA4 _N	F6	DB2 _P

Truth Table

SEL	/OE	Function
LOW	LOW	CLK _P =CLKA _P , CLK _N =CLKA _N , D _n (P/N)=DA _n (P/N)
HIGH	LOW	CLK _P =CLKB _P , CLK _N =CLKB _N , D _n (P/N)=DB _n (P/N)
X	HIGH	DA _n (P/N), DB _n (P/N) Data Ports High Impedance

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		-0.5	+5.25	V
V _{CNTRL}	DC Input Voltage (/OE) ⁽¹⁾		-0.5	V _{CC}	V
V _{SW}	DC Switch I/O Voltage ⁽¹⁾		-0.5	5.25	V
I _{IK}	DC Input Diode Current		-50		mA
I _{OUT}	DC Output Current			50	mA
T _{STG}	Storage Temperature		-65	+150	°C
ESD	HBM	All Pins		3.5	kV
		I/O to GND		3.5	
		Power to GND		8.0	
	CDM			1.5	

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		1.65	4.50	V
V _{CNTRL}	Control Input Voltage (S, /OE) ⁽²⁾		0	V _{CC}	V
V _{SW}	Switch I/O Voltage (CLKn, CLKAn, CLKBn, Dn, DAn, DBn)	HS Mode	0.1	0.3	V
		LP Mode	0	1.2	
T _A	Operating Temperature		-40	+85	°C

Note:

- The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

Typical values are at $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	$V_{CC}(V)$	Min	Typ	Max	Unit
V_{IK}	Clamp Diode Volatge	$I_{IN}=-18\text{mA}$	2.8			-1.28	V
V_{IH}	Input Voltage High		1.65 to 4.50	1.0			V
V_{IL}	Input Voltage Low		1.65 to 4.50			0.4	V
I_{IN}	Control Input Leakage (SEL, /OE)	$V_{SW}=0$ to V_{CC}	1.65 to 4.50	-100		100	nA
$I_{NO(OFF)}$, $I_{NC(OFF)}$	Off Leakage Current of Port CLKA _n , DAn, CLKB _n , DB _n	CLK _n , Dn=0.3V; $V_{CC}=0.3V$; CLKA _n , DAn, or CLKB _n ; DB _n = $V_{CC}-0.3V$, 0.3V, or Floating; /OE=0V	1.65 to 4.50	-100		100	nA
$I_{A(ON)}$	On Leakage Current of Common Ports (CLK _n , Dn)	CLK _n , Dn=0.3V; $V_{CC}=0.3V$; CLKA _n , DAn, or CLKB _n ; DB _n = $V_{CC}-0.3V$, 0.3V, or Floating; /OE=0V	1.65 to 4.50	-100		100	nA
I_{OZ}	Off-State Leakage	$0 \leq \text{CLK}_n, \text{Dn}, \text{CLKA}_n, \text{CLKB}_n,$ DAn, DB _n $\leq 3.6V$, /OE=High	4.5	-100		100	nA
$R_{ON_MIPI_HS}$	Switch On Resistance for HS MIPI Applications ⁽³⁾	$I_{ON}=-10\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLK _{A,B} , DB _n or DAn=0.1, 0.2, 0.3	1.8		6	10	Ω
			2.5		6	9	
			3.6		6	9	
			4.5		6	9	
$R_{ON_MIPI_LP}$	Switch On Resistance for LP MIPI Applications ⁽³⁾	$I_{ON}=-10\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLK _{A,B} , DB _n or DAn=0, 0.6, 1.2V	1.8		6.4	11	Ω
			2.5		6.4	10	
			3.6		6.2	9	
			4.5		6.0	9	
$\Delta R_{ON_MIPI_HS}$	On Resistance Matching Between HS MIPI Channels ⁽⁴⁾	$I_{ON}=-10\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLK _{A,B} , DB _n or DAn=0.1, 0.2, 0.3	1.8		0.8		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$\Delta R_{ON_MIPI_LP}$	On Resistance Matching Between LP MIPI Channels ⁽⁴⁾	$I_{ON}=-10\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLK _{A,B} , DB _n or DAn=0, 0.6, 1.2V	1.8		1.0		Ω
			2.5		0.6		
			3.6		0.4		
			4.5		0.4		
$R_{ON_FLAT_MIPI_HS}$	On Resistance Flatness for HS MIPI Signals ⁽⁴⁾	$I_{ON}=-10\text{mA}$, /OE=0V, SEL= V_{CC} or 0V, CLK _{A,B} , DB _n or DAn=0.1, 0.2, 0.3	1.8		0.5		Ω
			2.5		0.5		
			3.6		0.3		
			4.5		0.2		



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DC Electrical Characteristics

Typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	$V_{CC}(V)$	Min	Typ	Max	Unit
$R_{ON_FLAT_M}$ I_{PI_LP}	On Resistance Flatness for LP MIPI Signals ⁽⁴⁾	$I_{ON}=-10\text{mA}$, $/OE=0V$, $SEL=V_{CC}$ or $0V$, $CLK_{A,B}$, DBn or $DAn=0$, 0.6 , $1.2V$	1.8		0.6		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
I_{CCZ}	Quiescent Hi-Z Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	4.5			0.5	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	2.5 to 4.5		32	45	μA
			1.8			31	
$I_{CC\Delta}$	Increase in I_{CC} Current Per Control Voltage and V_{CC}	$V_{SEL}/OE=1.65V$	4.5			3	μA
			2.5			0.1	

Note:

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
- Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for $V_{CC}=3.3V$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	$V_{CC}(V)$	Min	Typ	Max	Unit
t_{INIT}	Initialization Time V_{CC} to Output ⁽⁵⁾	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$	2.5 to 4.5			235	μs
			1.8			364	
t_{EN}	Enable Turn-On Time, $/OE$ to Output	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$	2.5 to 4.5		150	180	μs
			1.8		170	300	
t_{DIS}	Disable Turn-Off Time, $/OE$ to Output	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$	2.5 to 4.5		150	300	ns
			1.8		150	300	
t_{ON}	Turn-On Time, SEL to Output	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$	2.5 to 4.5		420	610	ns
			1.8		475	640	
t_{OFF}	Turn-Off Time, SEL to Output	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$	2.5 to 4.5		223	275	ns
			1.8		237	301	
t_{BBM}	Break-Before-Make Time	$R_L=50\Omega$, $C_L=5\text{pF}$, $V_{SW}=1.2V$		115	180		ns
O_{IRR}	Off Isolation for MIPI ⁽⁵⁾	$R_L=50\Omega$, $f=750\text{MHz}$, $/OE=V_{CC}$, $V_{SW}=-1\text{dBm}$ (200mVpp)	1.65 to 4.5		-22		dB
X_{TALK}	Crosstalk for MIPI ⁽⁵⁾	$R_L=50\Omega$, $f=750\text{MHz}$, $V_{SW}=-1\text{dBm}$ (200mVpp)	1.65 to 4.5		-30		dB
BW	-3dB Bandwidth ⁽⁵⁾	$R_L=50\Omega$, $C_L=0\text{pF}$	3.0	1500	2000		MHz
S_{DD21}	Differential Data Rate	Inter-operability Data Rate	3.0		1.5		Gbps

Note:

- Guaranteed by characterization.



DIO1644

2:1 MPI D-PHY (1.5Gbps) 4-Data Lane Switch

High-Speed-Related AC Electrical Characteristics

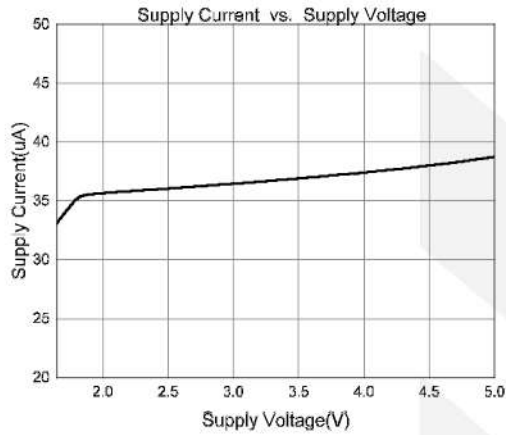
Symbol	Parameter	Test Conditions	V _{CC} (V)	Min	Typ	Max	Unit
t _{SK(O)}	Channel-to-Channel Single-Ended Skew ⁽⁶⁾	TDR-Based Method (V _{SW} =0.2V _{PP} , C _L =C _{ON})	3.3		6	20	ps
t _{SK(P)}	Skew of Opposite Transitions of the Same Output ⁽⁶⁾	TDR-Based Method (V _{SW} =0.2V _{PP} , C _L =C _{ON})	3.3		6	20	ps

Capacitance

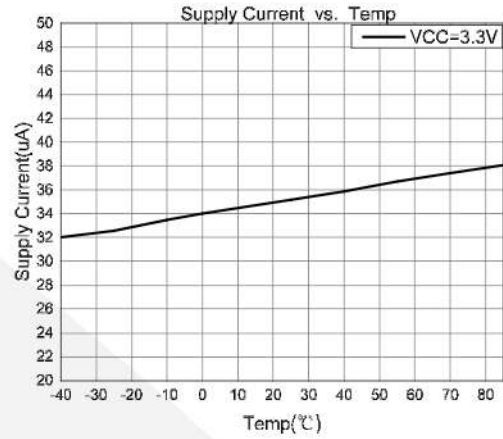
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{IN}	Control Pin Input Capacitance	V _{CC} =0V, f=1MHz		1.7		pF
C _{ON}	Out On Capacitance	V _{CC} =3.3V, /OE=0V, f=1MHz		4.2		
C _{OFF}	Out Off Capacitance	V _{CC} and /OE=3.3V, f=1MHz		1.6		

Typical Performance Characteristics

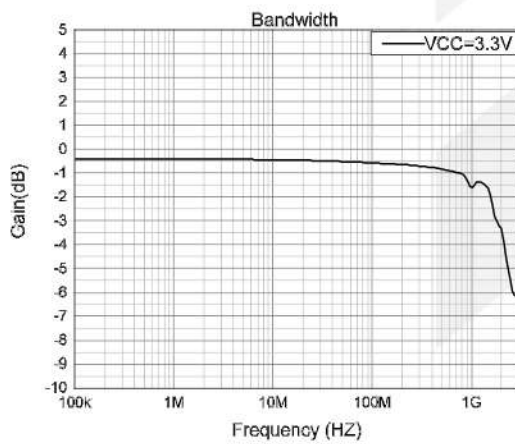
I_{CC} vs. V_{CC}



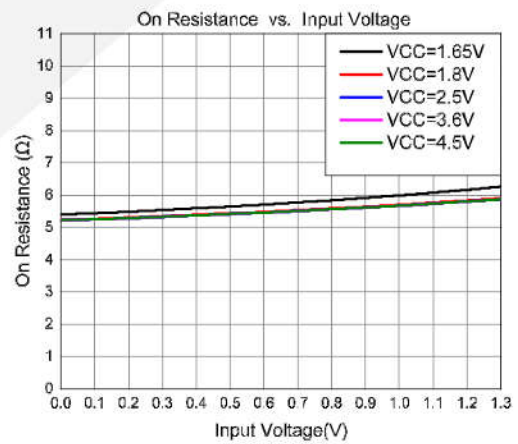
I_{CC} vs. Temperature



Bandwidth



On Resistance vs. Input Voltage





DIO1644

2:1 MIP1 D-PHY (1.5Gbps) 4-Data Lane Switch

CONTACT US

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