芯鼎盛®

TX15N10B

N channel 100V MOSFET

Description

The TX15N10B is the N-Channel logic enhancement mode power field effect transistorsare produced using high cell density, DMOS trench technology.This high density process isespecially tailored to minimize on-state resistance.These devices are particularly suited for lowvoltage application such as cellular phone, notebook computer power management and otherbattery powered circuits,and low in-line power loss that are needed in a very smalloutlinesurface mount package.

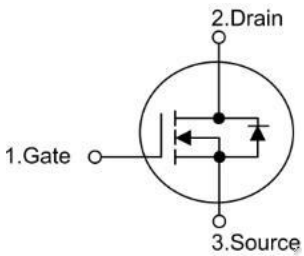
Features

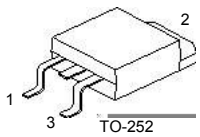
V_{DS}	100V
$R_{DS(on)}$Max.	100mΩ
I_D	15A

- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

Pin configuration

Order Number	Package
TX15N10B	TO-252





Maximum Ratings (Tc = 25℃ unless otherwise noted*)

Parameter		Symbol	Ratings	Units
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	15	A
	Tc=70℃		14	A
Pulsed Drain Current		I_{DM}	59	A
Power Dissipation	Tc=25℃	P_D	34.7	W
	Tc=70℃		22.2	
Operating Junction and Storage Temperature Range		T_J,T_{stg}	-55~+175	℃

* Dran current limited by maximum junction temperature.

Thermal Characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	RthCS	0.5	℃/W
Thermal resistance junction to case.	RthJC	3.6	℃/W
Thermal resistance junction to ambient.	RthJA	110	℃/W

Electrical characteristics (TA =25℃ Unless Otherwise Specified)

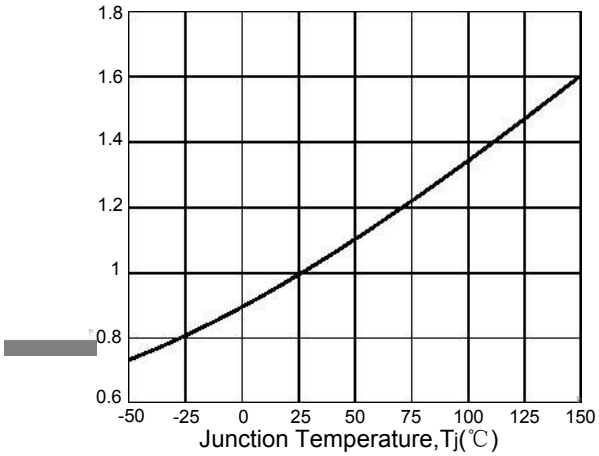
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	—	—	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	—	3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V	—	—	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V	—	—	1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=8A	—	80	100	mΩ
V_{SD}	Diode Forward Voltage	I_S=8A, V_{GS}=0V	—	0.9	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DD}=80V, V_{GS}=10V, I_D=10A		24		nC
Q_g	Total Gate Charge	V_{DD}=80V, V_{GS}=4.5V, I_D=10A	—	13	—	
Q_{gs}	Gate-Source Charge		—	4.6	—	
Q_{gd}	Gate-Drain Charge		—	7.6	—	
R_g	Gate Resistance	V_{DS}=0V,V_{GS}=0V, f=1MHz	—	0.9	—	Ω
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	—	890	—	pF
C_{oss}	Output Capacitance		—	58	—	
C_{rss}	Reverse Transfer Capacitance		—	23	—	
$t_{d(on)}$	Turn-On Delay Time	V_{DS} =50V, R_G=1Ω R_L=5Ω,V_{GEN}=10V,	—	14	—	ns
t_r	Turn-On Rise Time		—	33	—	
$t_{d(off)}$	Turn-Off Delay Time		—	39	—	
t_f	Turn-Off Fall Time		—	5	—	

Notes :a. Pulse test:pulse width 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

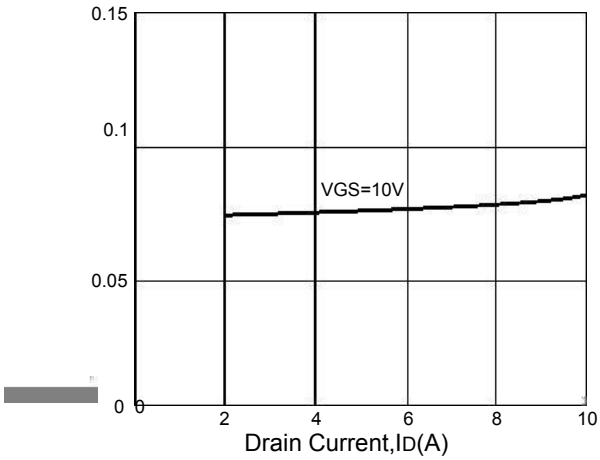
b. XDSSEMI reserves the right to improve product design,functions and reliability without notice.

Typical Characteristics (TJ =25℃ Noted)

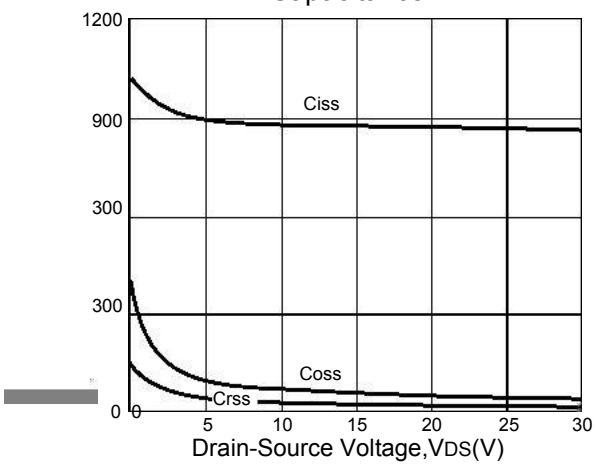
On Resistance vs.Junction Temperature



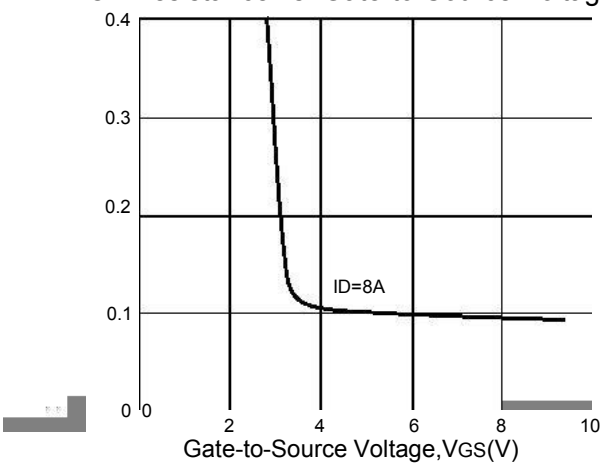
On Resistance vs. Drain Current



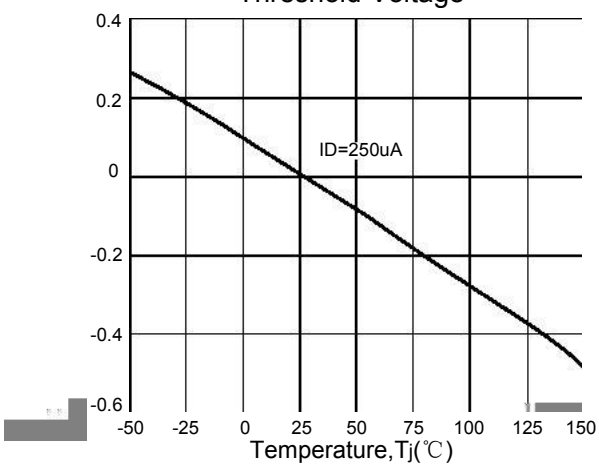
Capacitance



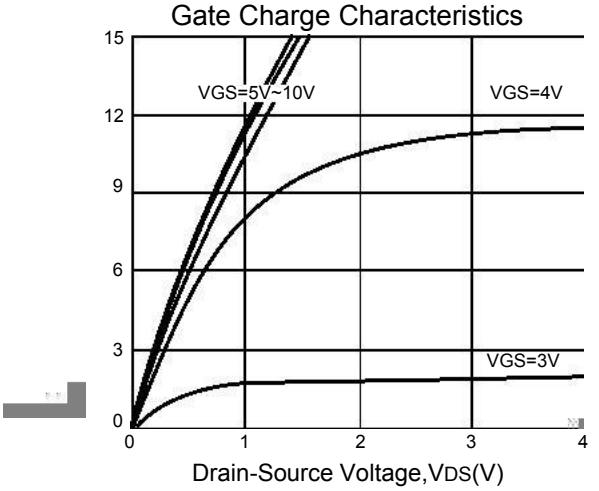
On Resistance vs. Gate-to-Source Voltage



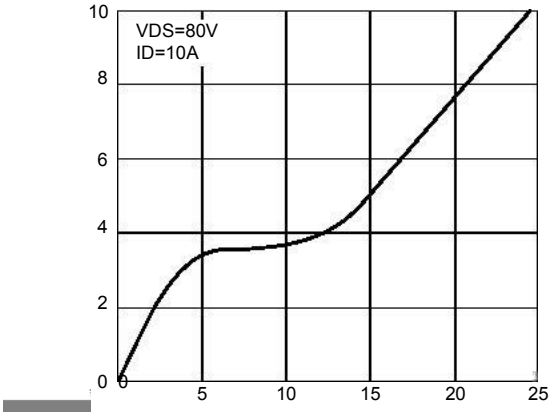
Threshold Voltage



Gate Charge Characteristics

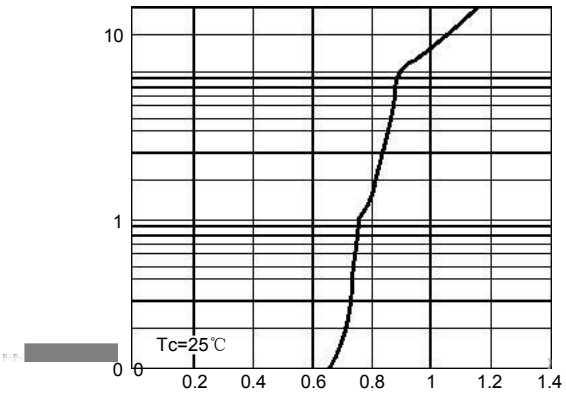


Typical Characteristics(TJ=25℃)



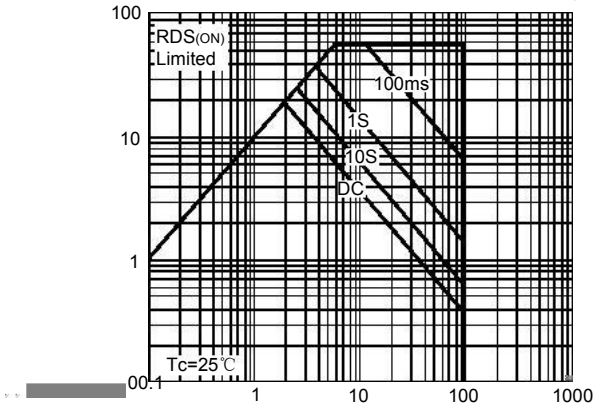
Total Gate Charge,Qg(nC)

Body diode characteristics



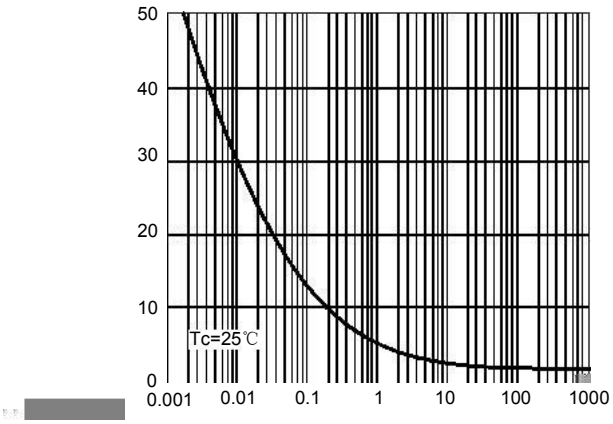
Source-Drain Voltage,VSD(V)

Maximum Forward Biased Safe Operating Area



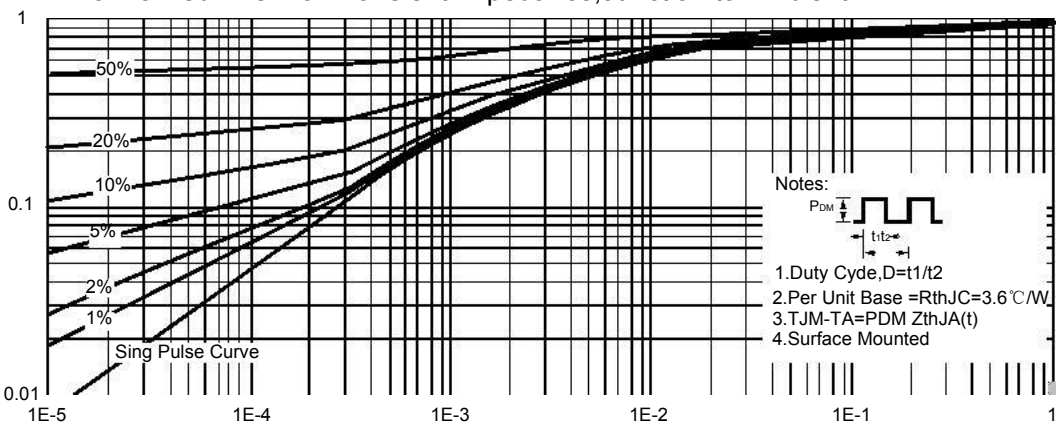
Drain-Source Voltage,VDS(V)

Single Pulse Maximum Power Dissipation



Time,t1(sec)

Normalized Thermal Transient Impedance,Junction to Ambient



Square Wave Pulse Duration(sec)

SOT-89

Unit：mm