华润微电子(重庆)有限公司

CRTM025N03L

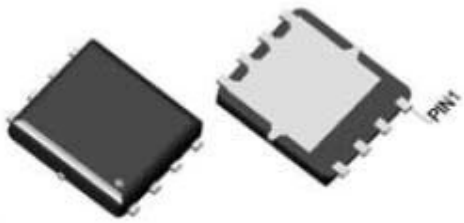
Features

- Lead free and Green Device Available
- Low Rds-on to Minimize Conductive Loss
- High avalanche Current

V_{DSS}	30V
$R_{DS(on)}$ Vgs=10V typ.	2.0mΩ
max.	2.5mΩ
$R_{DS(on)}$ Vgs=4.5V typ.	2.6mΩ
max.	3.3mΩ
I_D @ Vgs=10V (Silicon limited)	98A

Application

- Load Switch
- SPMS



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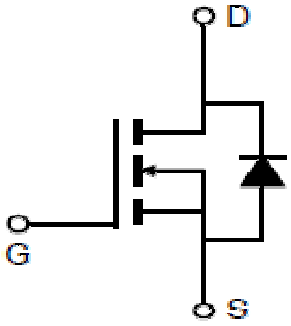


Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Param			Maximum	Unit
V_{DSS}	Drain-to-Source Voltage			30	V
V_{GSS}	Gate-to-Source Voltage			±20	V
I_D Vgs=10V	Continuous Drain Current	T_c=25°C		98	A
		T_c=100°C		62	
I_D Vgs=4.5V		T_c=25°C		85	
		T_c=100°C		54	
I_{DP}	Pulsed Drain Current	T_a=25°C		-	A
I_{AS}	Avalanche Current (L=0.3mH)			28	A
E_{AS}	Avalanche Energy (L=0.3mH)			117	mJ
P_D	Maximum Power Dissipation		T_a=25°C	2.5	W
			T_a=100°C	1	
T_J, T_{STG}	Junction & Storage Temperature Range			-55~150	°C

Thermal Characteristics

Symbol	Parameter	Max.	Unit
R_{thJC}	Thermal resistance, junction to case	3.2	℃/W
R_{thJA}	Thermal resistance, junction to ambient	50	℃/W

Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	30	—	—	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V,V_{GS}=0V	—	—	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	1.3	—	2.3	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	—	—	±100	nA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=50A	—	2.0	2.5	mΩ
		V_{GS}=4.5V, I_D=40A	—	2.6	3.3	
Gfs	Forward Transconductance	VDS=5V, ID=70A	—	153	—	S
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=70A,V_{GS}=0V	—	0.9	1.3	V
I_S	Diode Continuous Forward Current		—	—	24	A
t_{rr}	Reverse Recovery Time	IS=50A, di/dt=100A/us	—	27	—	nS
Q_{rr}	Reverse Recovery Charge		—	16	—	nC
Dynamic Characteristics						
R_G	Gate Resistance	V_{GS}=0V, V_{DS}=0V, Frequency=1MHz	—	2.5	—	Ω
C_{iss}	Input Capacitance	VGS=0V, VDS=15V, F=1MHz	—	6120	—	pF
C_{oss}	Output Capacitance		—	704	—	
C_{rss}	Reverse Transfer Capacitance		—	638	—	
$t_{d(on)}$	Turn-On Delay Time	VDS=15V, ID=20A, Rg=3 Ω, VGS=4.5V	—	51	—	nS
t_r	Rise Time		—	107	—	
$t_{d(off)}$	Turn-Off Delay Time		—	95	—	
t_f	Fall Time		—	73	—	
Gate Charge Characteristics						
Q_g	Total Gate Charge	VDS=15V，VGS=4.5V，ID=50A	—	52	—	nC
Q_{gs}	Gate-to-Source Charge		—	16	—	
Q_{gd}	Gate-to-Drain Charge		—	23	—	

Typical Operating Characteristics

Figure 1. Typ. Output Characteristics

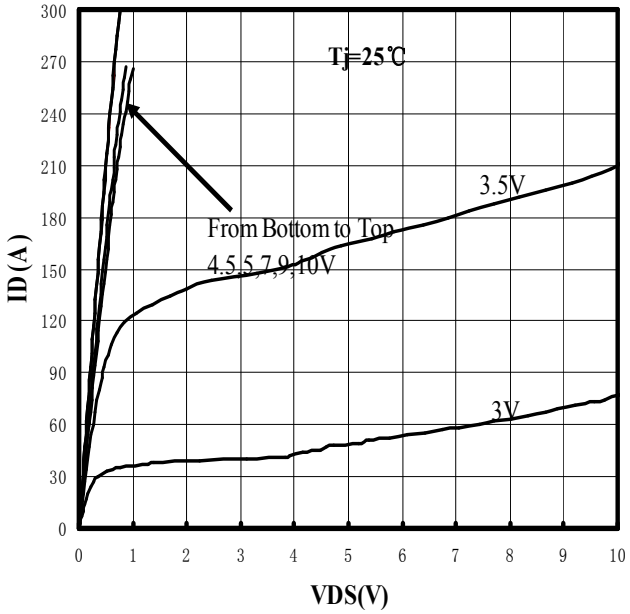


Figure 2. Typ. Output Characteristics

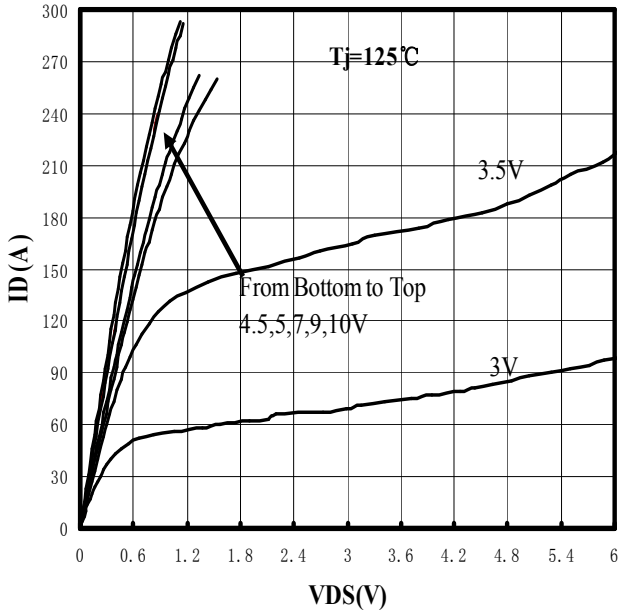


Figure 3. Transfer Characteristics

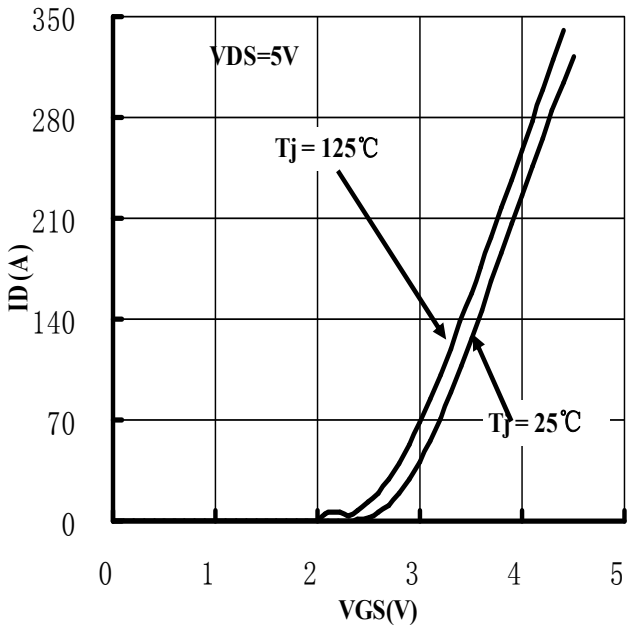
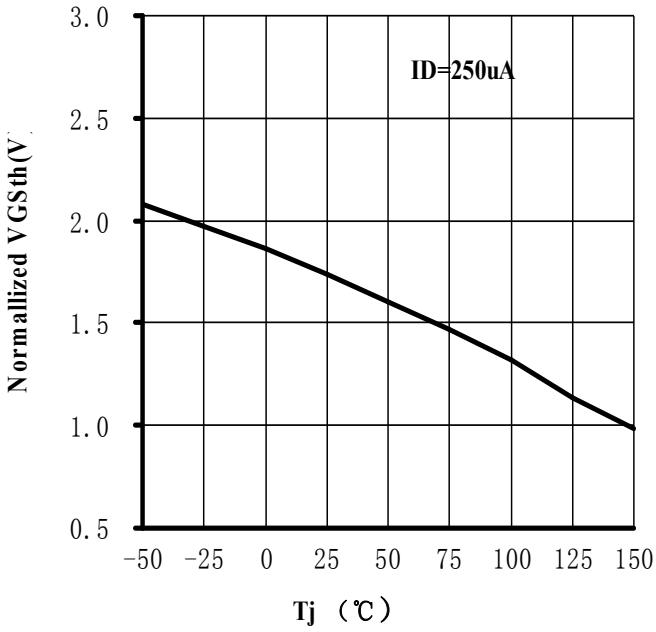


Figure 4. Gate Threshold Voltage Characteristics



Typical Operating Characteristics

Figure 5. Rdson vs. Drain Current Characteristics

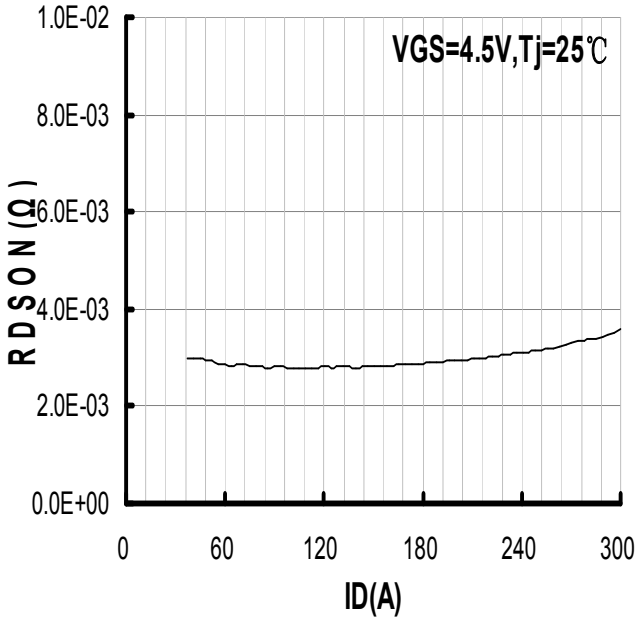


Figure 6. Rdson vs. Junction Tem Characteristics

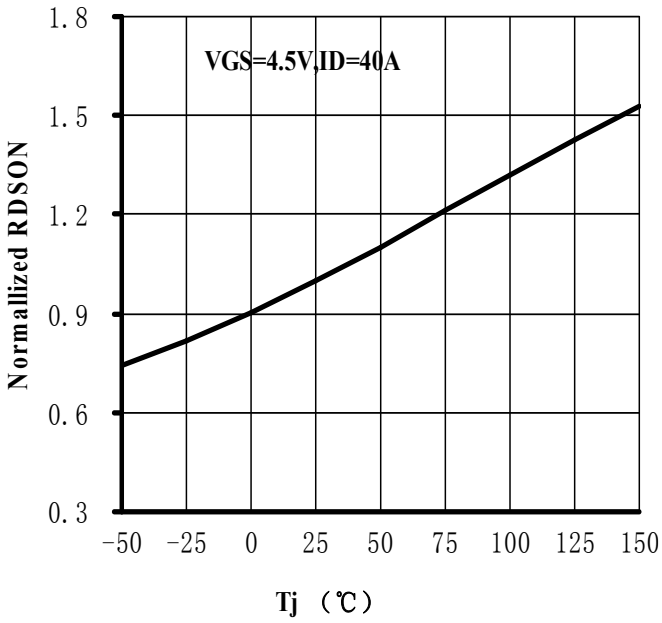


Figure 7. Rdson vs. VGS Characteristics

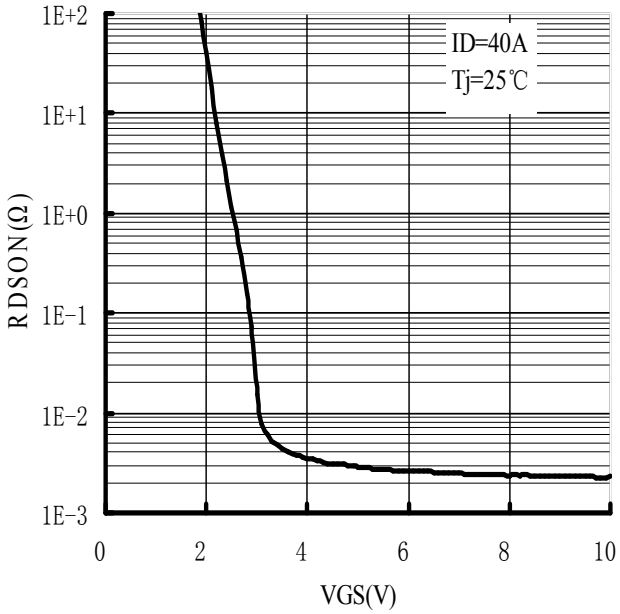
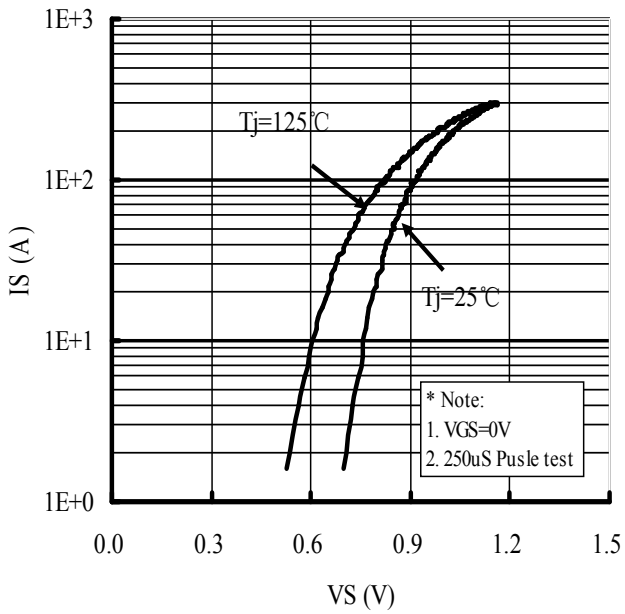


Figure 8. IS vs. VSD Characteristics



Typical Operating Characteristics

Figure 9. Gate Charge Characteristics

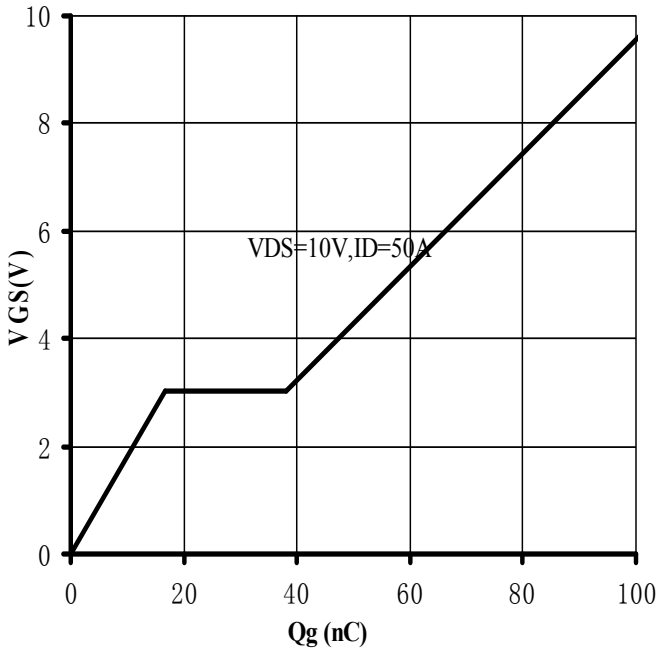


Figure 10. Capacitance Characteristics

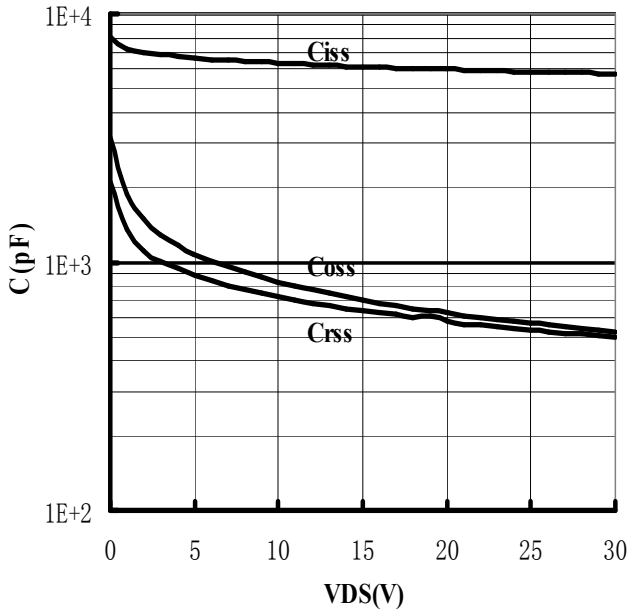


Figure 11. Thermal Resistance Characteristics

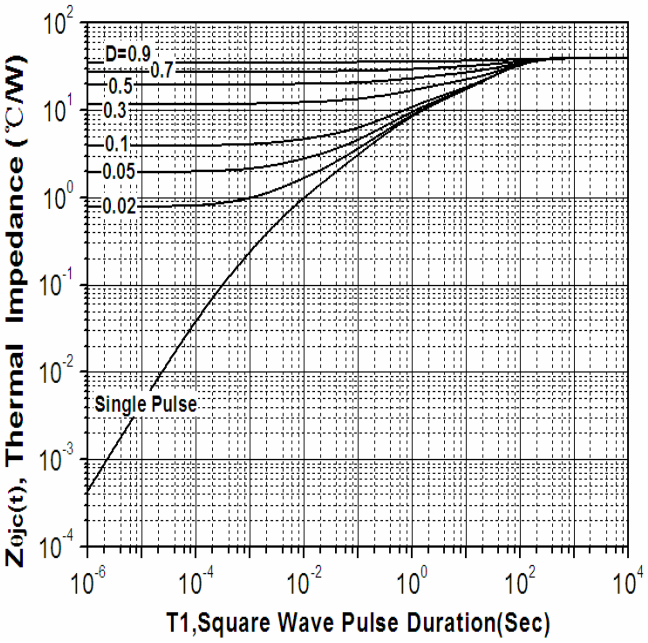
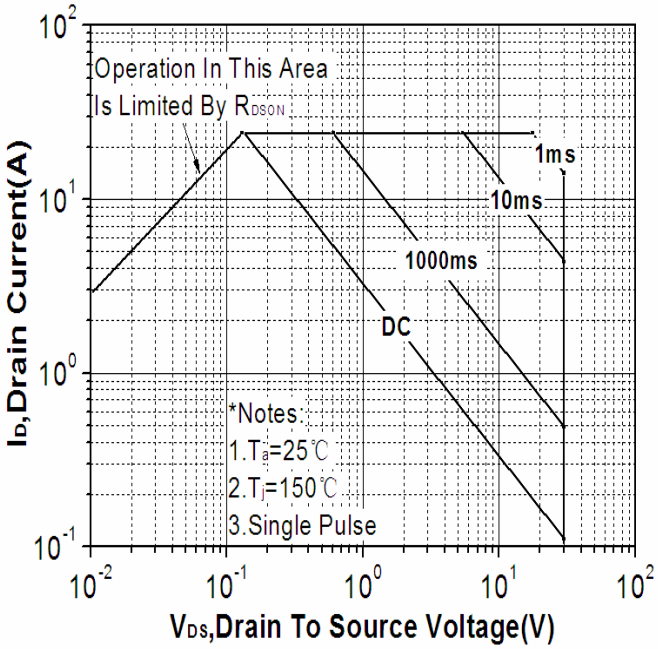
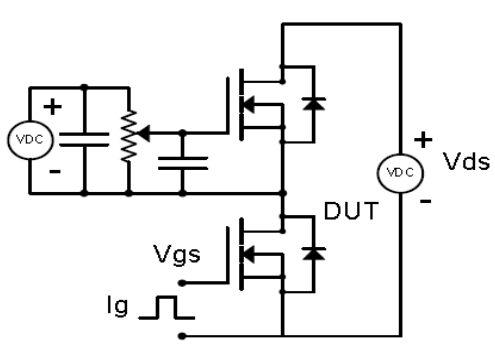


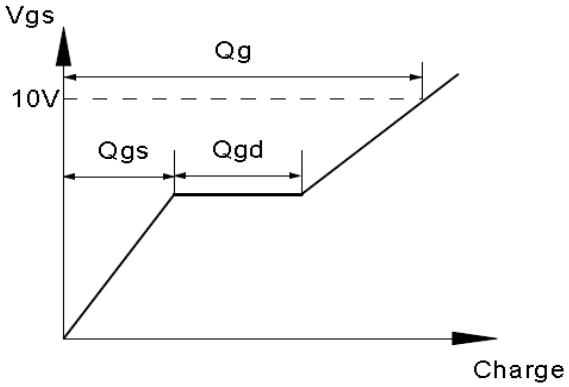
Figure12 SOA



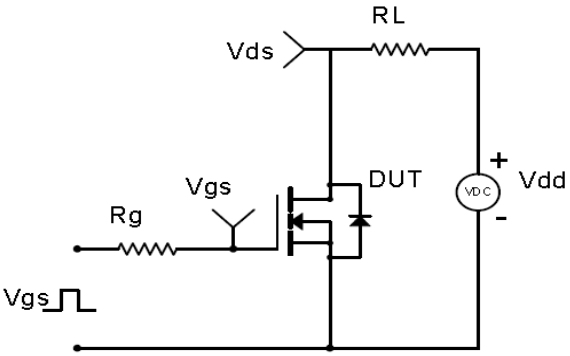
Test Circuit & Waveform

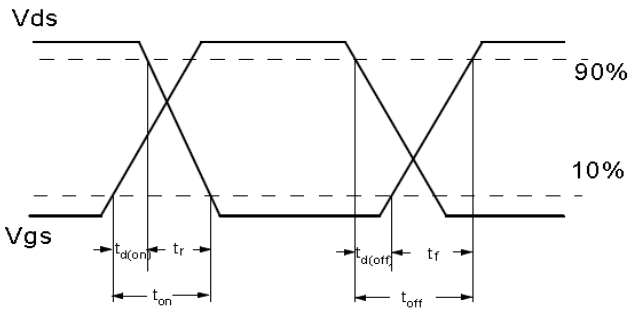
Gate Charge Test Circuit & Waveform



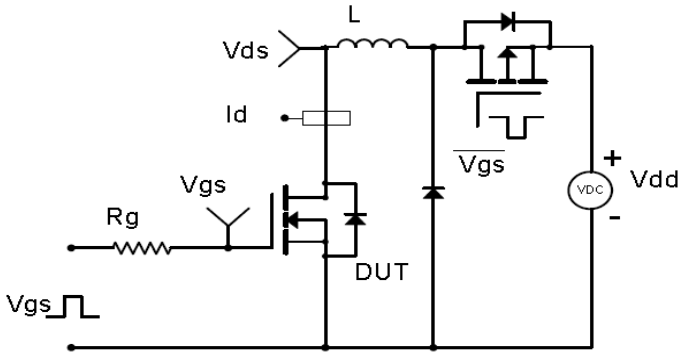


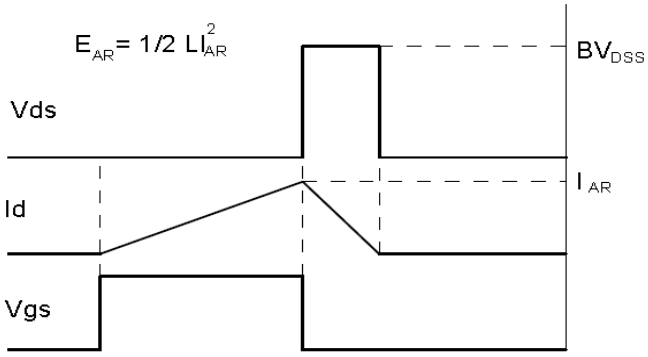
Resistive Switching Test Circuit & Waveforms



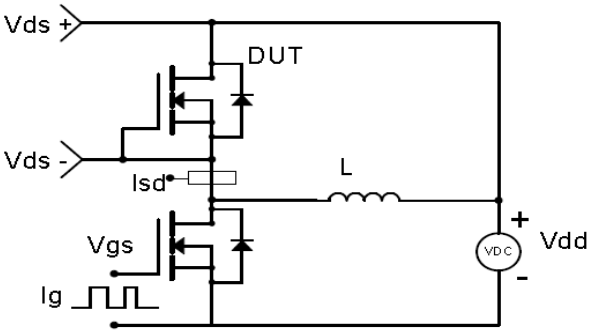


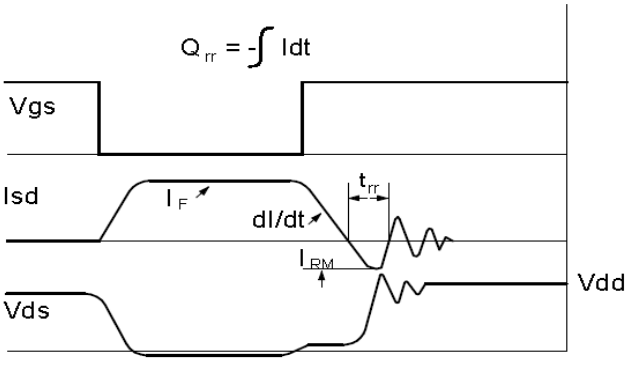
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



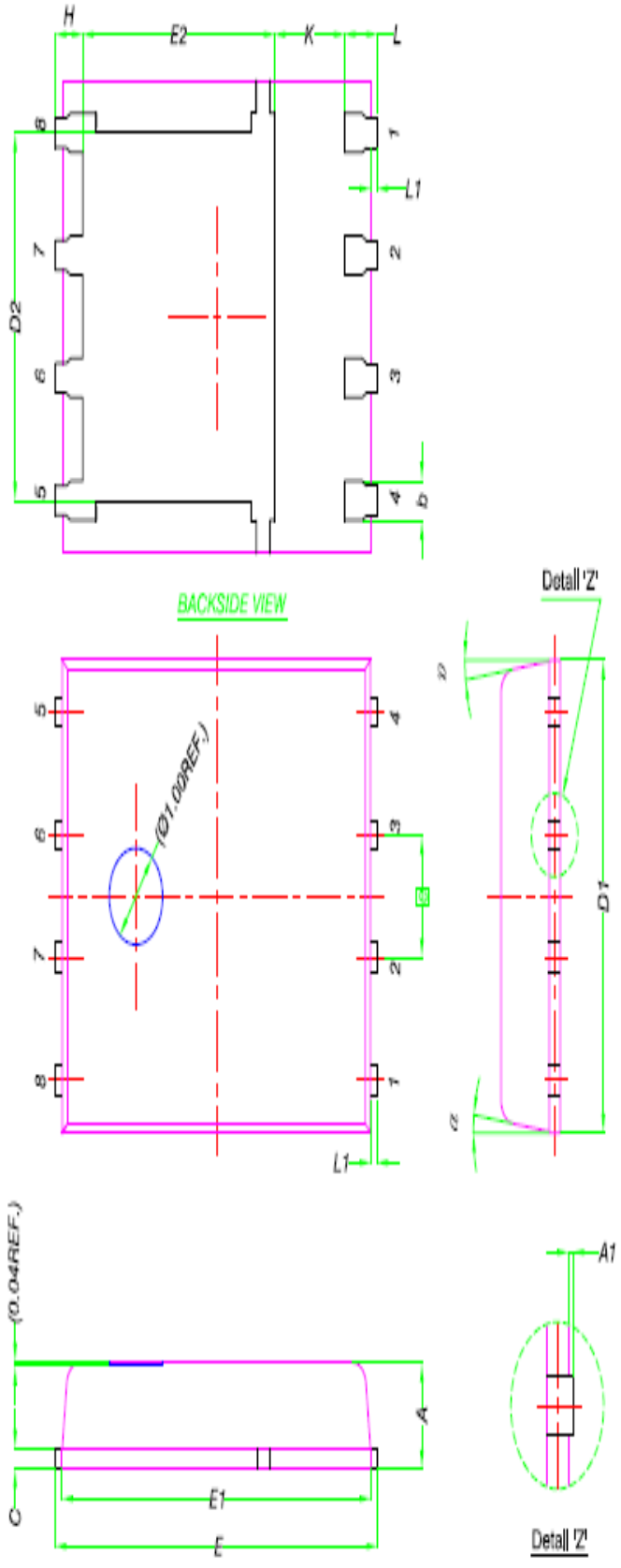


Diode Recovery Test Circuit & Waveforms

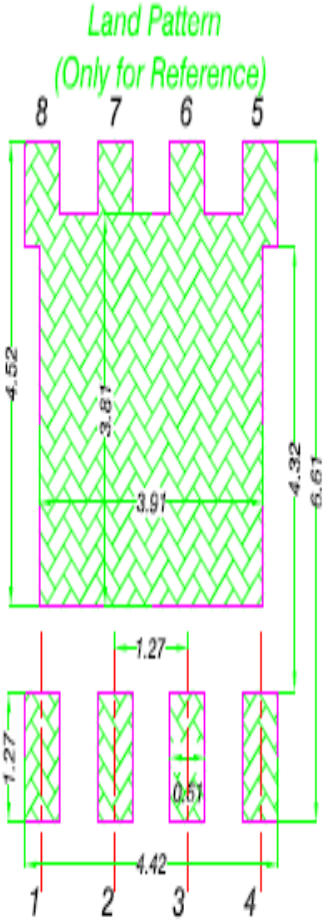




Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.