Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Hard disk and computing power management

1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|------------------------|----------------------------------|--|-----|-----|-----|------|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | - | -30 | V |
| V _{GS} | gate-source voltage | | | -20 | - | 20 | V |
| I _D | drain current | V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s | [1] | - | - | -8.8 | Α |
| Static characteristics | | | | | | | |
| R _{DSon} | drain-source on-state resistance | V_{GS} = -10 V; I_D = -6.1 A; T_j = 25 °C | | - | 24 | 29 | mΩ |

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



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2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|-----------------------|-----------------|
| 1 | D | drain | 1 6 | D |
| 2 | D | drain | 7 7 | |
| 3 | G | gate | | G T T |
| 4 | S | source | 3 8 4 | \$ 017aaa257 |
| 5 | D | drain | Transparent top view | |
| 6 | D | drain | DFN2020MD-6 (SOT1220) | |
| 7 | D | drain | | |
| 8 | S | source | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | | | | |
|-------------|-------------|--|---------|--|--|--|
| | Name | Description | Version | | | |
| PMPB27EP | DFN2020MD-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals | SOT1220 | | | |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMPB27EP | 1V |

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|------------------|-------------------------|--|-----|-----|------|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | -30 | V |
| V_{GS} | gate-source voltage | | | -20 | 20 | V |
| I _D | drain current | V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s | [1] | - | -8.8 | Α |
| | | V _{GS} = -10 V; T _{amb} = 25 °C | [1] | - | -6.1 | Α |
| | | V _{GS} = -10 V; T _{amb} = 100 °C | [1] | - | -3.9 | Α |
| I _{DM} | peak drain current | T_{amb} = 25 °C; single pulse; $t_p \le 10$ μs | | - | -25 | Α |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [1] | - | 1.7 | W |
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| Symbol | Parameter | Conditions | | Min | Max | Unit | |
|--------------------|----------------------|-----------------------------------|-----|-----|------|------|--|
| | | T _{amb} = 25 °C; t ≤ 5 s | [1] | - | 3.5 | W | |
| | | T _{sp} = 25 °C | | - | 12.5 | W | |
| Tj | junction temperature | | | -55 | 150 | °C | |
| T _{amb} | ambient temperature | | | -55 | 150 | °C | |
| T _{stg} | storage temperature | | | -65 | 150 | °C | |
| Source-drain diode | | | | | | | |
| I _S | source current | T _{amb} = 25 °C | [1] | - | -1.9 | Α | |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

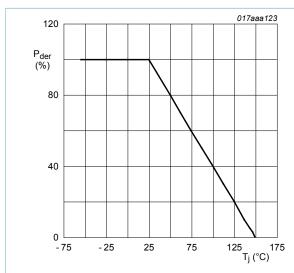


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

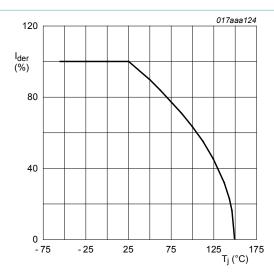


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

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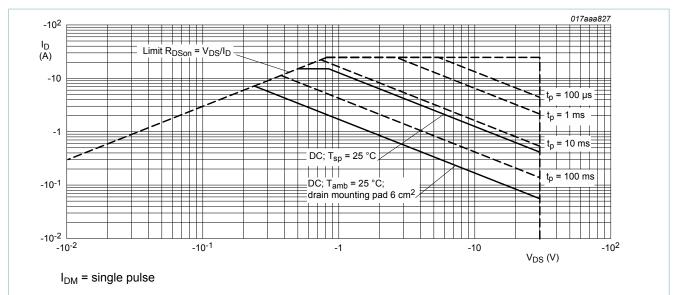


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|--|--|----------------------|-----|-----|-----|-----|------|
| R _{th(j-a)} thermal resistance from junction to ambient | | in free air | [1] | - | 235 | 270 | K/W |
| | | [2] | - | 67 | 74 | K/W | |
| | ambient | in free air; t ≤ 5 s | [2] | - | 33 | 36 | K/W |
| R _{th(j-sp)} | thermal resistance from junction to solder point | | | - | 5 | 10 | K/W |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

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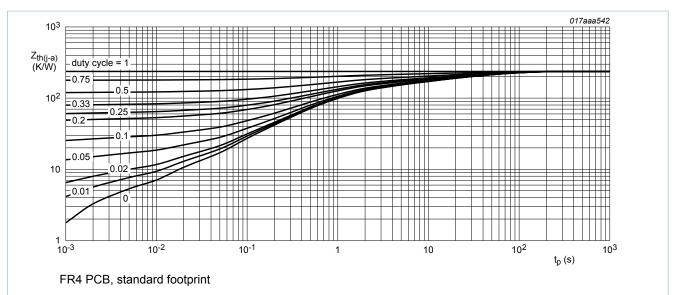
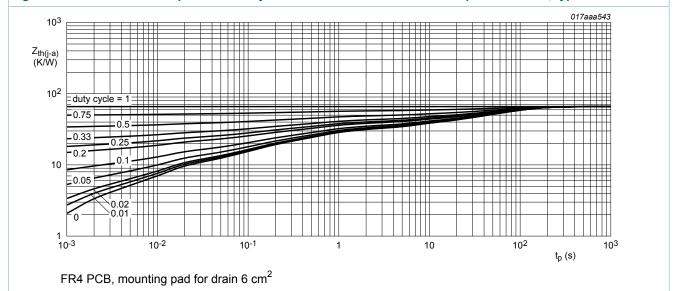


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

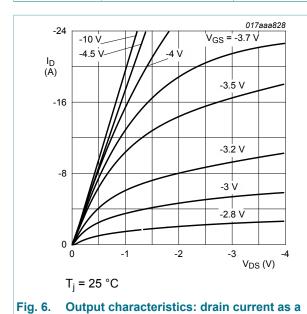
Table 7. Characteristics

Fig. 5.

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|----------------------|--------------------------------|--|--|-----|-----------|--------------|-----------------|
| Static chara | Static characteristics | | | | | | |
| V _{(BR)DSS} | drain-source breakdown voltage | $I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$ | | -30 | - | - | V |
| V _{GSth} | gate-source threshold voltage | $I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$ | | -1 | -1.5 | -2.5 | V |
| I _{DSS} | drain leakage current | V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C | | - | - | -1 | μA |
| I _{GSS} | gate leakage current | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$ | | - | - | -100 | nA |
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| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|---------------------|------------------------------|---|---|-----|------|------|------|
| | | V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C | | - | - | 100 | nA |
| R _{DSon} | drain-source on-state | V_{GS} = -10 V; I_{D} = -6.1 A; T_{j} = 25 °C | | - | 24 | 29 | mΩ |
| | resistance | V _{GS} = -10 V; I _D = -6.1 A; T _j = 150 °C | | - | 37 | 45 | mΩ |
| | | V_{GS} = -4.5 V; I_D = -5 A; T_j = 25 °C | | - | 32 | 43 | mΩ |
| 9 _{fs} | forward transconductance | V_{DS} = -10 V; I_{D} = -6.1 A; T_{j} = 25 °C | | - | 26 | - | S |
| R_G | gate resistance | f = 1 MHz | | - | 5.4 | - | Ω |
| Dynamic c | haracteristics | | | | | | |
| Q _{G(tot)} | total gate charge | V_{DS} = -15 V; I_{D} = -6.1 A; V_{GS} = -10 V; T_{j} = 25 °C | | - | 30 | 45 | nC |
| Q _{GS} | gate-source charge | | | - | 4.8 | - | nC |
| Q _{GD} | gate-drain charge | | | - | 6.3 | - | nC |
| C _{iss} | input capacitance | V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V; | | - | 1570 | - | pF |
| C _{oss} | output capacitance | T _j = 25 °C | | - | 170 | - | pF |
| C _{rss} | reverse transfer capacitance | | | - | 150 | - | pF |
| t _{d(on)} | turn-on delay time | V_{DS} = -15 V; I_{D} = -6.1 A; V_{GS} = -10 V; | | - | 10 | - | ns |
| t _r | rise time | $R_{G(ext)} = 6 \Omega; T_j = 25 °C$ | | - | 31 | - | ns |
| t _{d(off)} | turn-off delay time | | | - | 28 | - | ns |
| t _f | fall time | 1 | | - | 19 | - | ns |
| Source-dra | ain diode | - | 1 | 1 | 1 | 1 | |
| V _{SD} | source-drain voltage | I _S = -1.9 A; V _{GS} = 0 V; T _j = 25 °C | | - | -0.8 | -1.2 | V |



function of drain-source voltage; typical values

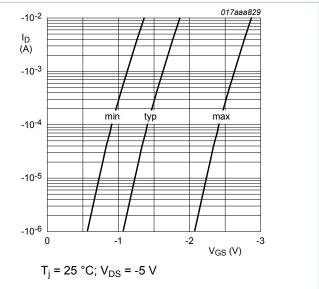


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

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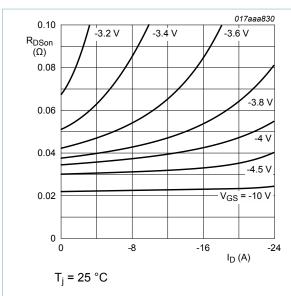


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

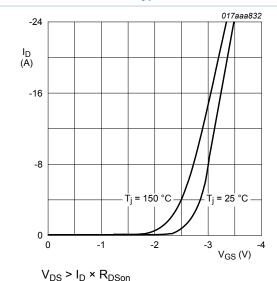


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

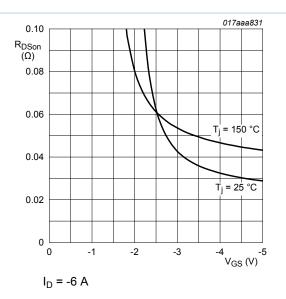


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

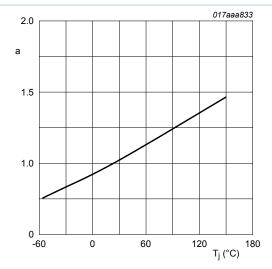


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

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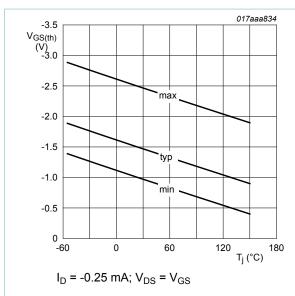


Fig. 12. Gate-source threshold voltage as a function of junction temperature

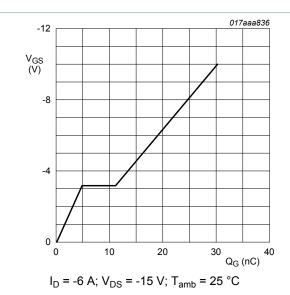


Fig. 14. Gate-source voltage as a function of gate charge; typical values

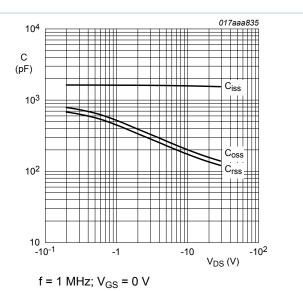


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

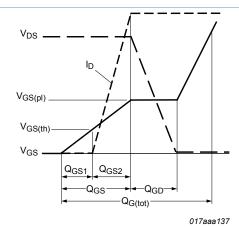
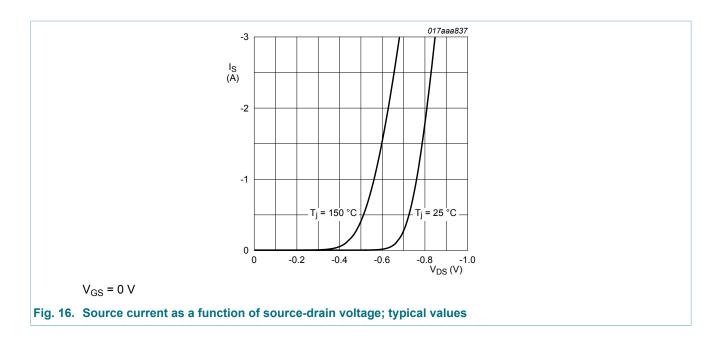
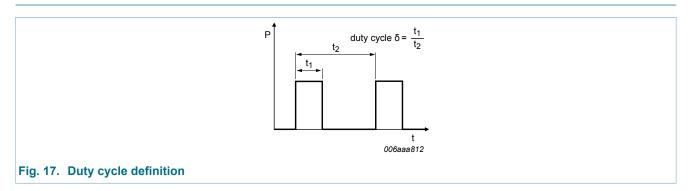


Fig. 15. Gate charge waveform definitions

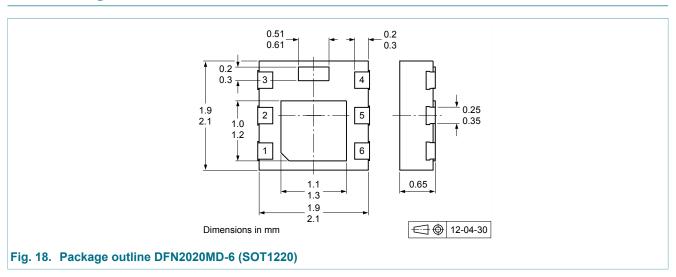
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8. Test information



9. Package outline



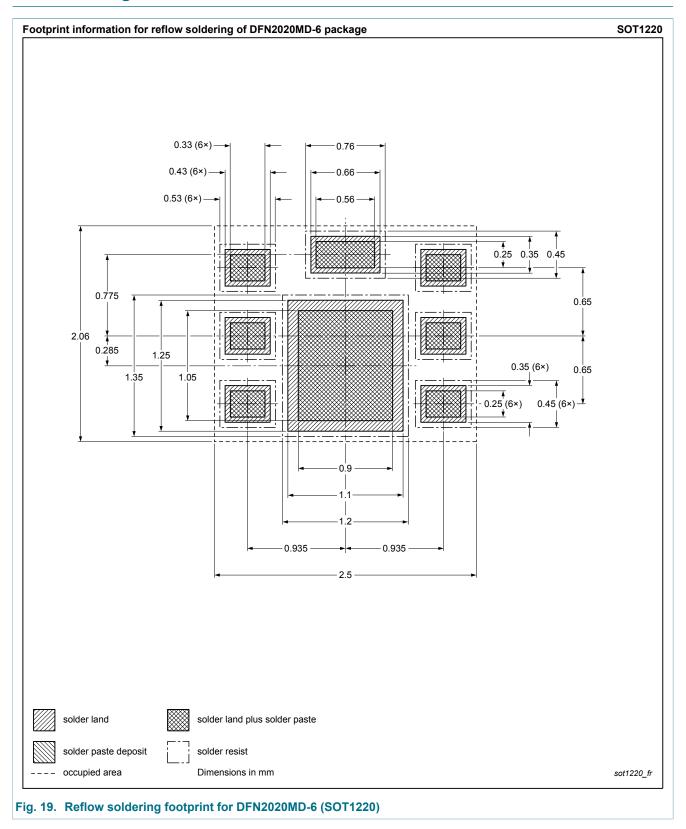
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10. Soldering



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11. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| PMPB27EP v.1 | 20120910 | Product data sheet | - | - |

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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