# 華 芯 www.wx.hxkl.com

#### HX6659 (T) Specifications

#### **CMOS Ratio-Metric Linear Hall Effect IC**

HX6659-B,HX6659-C,HX6659-D, a linear Hall-effect sensor, is composed of Hall sensor, linear amplifier and Totem-Pole output stage. It features low noise output, which makes it unnecessary to use external filtering. It also can provide increased temperature stability and accuracy. The linear Hall sensor has a wide operating temperature range of -40°C to +105°C, appropriate for commercial, consumer, and industrial environments.

The high sensitivity of Hall-effect sensor accurately tracks extremely weak changes in magnetic flux density. The linear sourcing output voltage is set by the supply voltage and in proportion of vary of the magnetic flux density. Typical operation current is 2.5 mA and operating voltage range is 2.8 volts to 6.0 volts. Trim version is available for an ultra low offset products.

The three package styles available provide magnetically optimized solutions for most applications. Package types SO is an SOT-23(1.1 mm nominal height), SQ is an QFN2020-3(0.5 mm nominal height), a miniature low-profile surface-mount package, while package UA is a three-lead ultra-mini SIP for through-hole mounting.

### Features and Benefits

- Operating Voltage Range: 2.8V~6.0V
- Power consumption of 2.5 mA at 5 V<sub>DC</sub> for energy efficiency
- Low-Noise Operation
- Linear output for circuit design flexibility
- Totem-Pole for a stable and accurate output
- Responds to either positive or negative gauss
- Magnetically Optimized Package for UA,SQ,SO
- Trim version is precise on offset
- Robust ESD performance

#### **Applications**

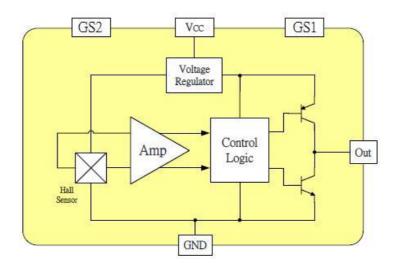
- Current sensing
- Motor control
- Position sensing
- Magnetic code reading
- Rotary encoder
- Ferrous metal detector
- Vibration sensing
- Liquid level sensing
- Weight sensing



## **CMOS Ratio-Metric Linear Hall Effect IC**

Part No.	Temperature Suffix	Package Type
HX6659IUA-B	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	UA (TO92-3L)
HX6659IUA-C	I $(-40^{\circ}\text{C to } +105^{\circ}\text{C})$	UA (TO92-3L)
HX6659IUA-D	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	UA (TO92-3L)
HX6659ISQ-B	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	SQ (QFN2020-3)
HX6659ISQ-C	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SQ (QFN2020-3)
HX6659ISQ-D	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SQ (QFN2020-3)
HX6659ISO-B	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	SO(SOT-23)
HX6659ISO-C	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SO(SOT-23)
HX6659ISO-D	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SO(SOT-23)
HX6659IUA-B-T	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	UA (TO92-3L)
HX6659IUA-C-T	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	UA (TO92-3L)
HX6659IUA-D-T	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	UA (TO92-3L)
HX6659ISQ-B-T	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	SQ (QFN2020-3)
HX6659ISQ-C-T	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	SQ (QFN2020-3)
HX6659ISQ-D-T	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SQ (QFN2020-3)
HX6659ISO-B-T	I ( $-40^{\circ}$ C to $+105^{\circ}$ C)	SO(SOT-23)
HX6659ISO-C-T	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SO(SOT-23)
HX6659ISO-D-T	$I (-40^{\circ}C \text{ to } +105^{\circ}C)$	SO(SOT-23)

# Functional Diagram





## **CMOS Ratio-Metric Linear Hall Effect IC**

**Absolute Maximum Ratings** At (Ta=25°C)

Characteristics		Values	Unit	
Supply Voltage (VDD)		8	V	
Reverse Voltage, (VDDR)		-0.5	V	
Output Voltage, (Vout)		8	V	
Output current, (Iovr)		5	mA	
Operating Temperature Range, (T <sub>A</sub> )		-40 ~ +125	°C	
Storage temperature Range, (Ts)		-65 ~ +150	°C	
Package Power Dissipation, (PD)	UA/SO/SQ	606/230/230	mW	

Note: Do not apply reverse voltage to V<sub>DD</sub> and V<sub>OUT</sub> Pin, It may be caused for Miss function or damaged device.

## **Electrical Specifications**

DC Operating Parameters: T<sub>A</sub>=+25°C, V<sub>CC</sub>=5.0V

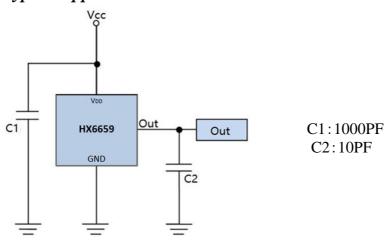
Parameters	<b>Test Conditions</b>	Min	Тур	Max	Units
Supply Voltage, $(V_{DD})$	Operating	2.8		6.0	V
Supply Current,(I <sub>DD</sub> )	B= 0 Gauss		3.3	5.0	mA
Output Current,(I <sub>O</sub> )	$V_{DD} > 3V$	1.0	1.5		mA
Null Output Voltage,(V <sub>NULL</sub> )	B= 0 Gauss, 2.375 (T type) (2.475		2.5	2.625 (2.525)	V
High Output Voltage, $(V_{OH})$	B> Max Magnetic Gauss		4.9	4.99	V
Low Output Voltage, (VoL)	B> Min Magnetic Gauss	0.01	0.1		V
Output Voltage Span,(Vos)			4.8		V
Output Referred Noise, (VoN)	Ta=25°C, output open		20		mV
Power-On Time, $(T_P)$				100	uS
Output Switch Time, $(T_{SW})$				150	uS
Output Switch Frequency, $(F_{SW})$		3			kHz
Magnetic Range Gauss	В	±1200			Gauss
	С	±960			Gauss
	D	±800			Gauss
Ratiometry Null output error,	Operating voltage range		±1.5		%



## **CMOS Ratio-Metric Linear Hall Effect IC**

$(R_{\text{VON}})$	relative to 5V					
Ratiometry Sensitivity error, $(R_{SEN})$	Operating voltage range relative to 5V			±1.5		%
Linearity, (LIN)	% of Span			±1.5		%
Sensitivity	В	Standard, (T type)	1.8 (1.9)	2.0	2.2 (2.1)	mV/G
	С	Standard, (T type)	2.250 (2.375)	2.5	2.750 (2.625)	mV/G
	D	Standard, (T type)	2.70 (2.85)	3.0	3.30 (3.15)	mV/G
Sensitivity Temperature Coefficient, ( <i>TC</i> <sub>Sens</sub> )	Ta=125°C, relative to Sens@25°C			±10		%/°C
Deka null vokage, $(\Delta V_{ m ON})$	Ta=125°C, relative to Von @25°C			20		mV
Electro-Static Discharge	НВМ		4			KV

# Typical application circuit



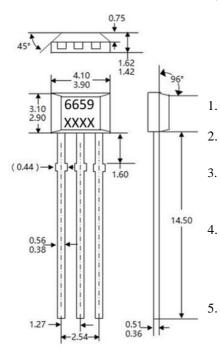


#### **CMOS Ratio-Metric Linear Hall Effect IC**

## Sensor Location, Package Dimension and Marking **Package**

#### **UA** package

#### **NOTES:**

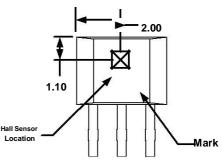


- Controlling dimension: mm
- Leads must be free of flash an plating voids
- Do not bend leads within 1 mm of lead to package interface.
- PINOUT:

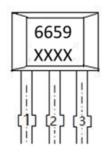
VCC Pin 1 **GND** Pin 2 Pin 3 Output

XXXX,  $1^{st} X = B/C/D$ 2<sup>nd</sup> -4<sup>th</sup> X=Date Code

#### **Hall Chip location**



## **Output Pin Assignment** (Top view)



#### **SQ Package**

# (Top View) Pin 1 dot 1.00 (Bottom View)

#### **NOTES:**

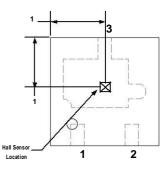
PINOUT (See Top View at left) Pin 1 Vcc

Pin 2 Output

**GND** Pin 3

- 2. Controlling dimension: mm;
- Chip rubbing will be 3. 10mil maximum;
- 4. Chip must be in PKG. center.
- 6659X, X = B/C/D5.
- 6. XX= Date code

## **Hall Plate Chip Location** (Top view)

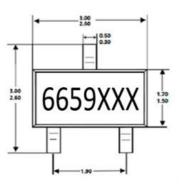


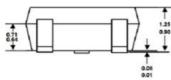


#### **CMOS Ratio-Metric Linear Hall Effect IC**

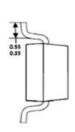
#### SO Package

(Top View)

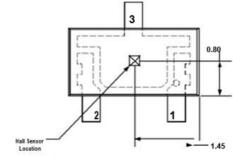




# Hall Plate Chip Location (Bottom view)



NOTES:



- 1. PINOUT (See Top View at left:)
  - Pin 1 V<sub>DD</sub>
  - Pin 2 Output
  - Pin 3 GND
- 2. Controlling dimension: mm
- 3. Lead thickness after solder plating will be 0.254mm maximum
- 4. Chip must be in PKG. center.
- 5. 6659XXX,  $1^{st}$  X = B/C/D  $2^{nd}$   $^{3}rd$   $^{1}$   $^{2}$ Date Code