

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE0130A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

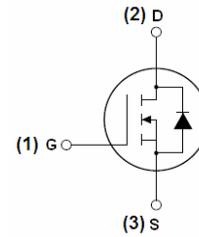
- $V_{DS} = 100V, I_D = 30A$
 $R_{DS(ON)} < 32m\Omega @ V_{GS}=10V$ (Typ:25m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0130A	NCE0130A	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	21	A
Pulsed Drain Current ^(Note 1)	I_{DM}	120	A
Maximum Power Dissipation	P_D	85	W
Derating factor		0.57	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	200	mJ
V_{DS} Spike ^(Note 6)	10 μs	120	V
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.8	$^\circ C/W$
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

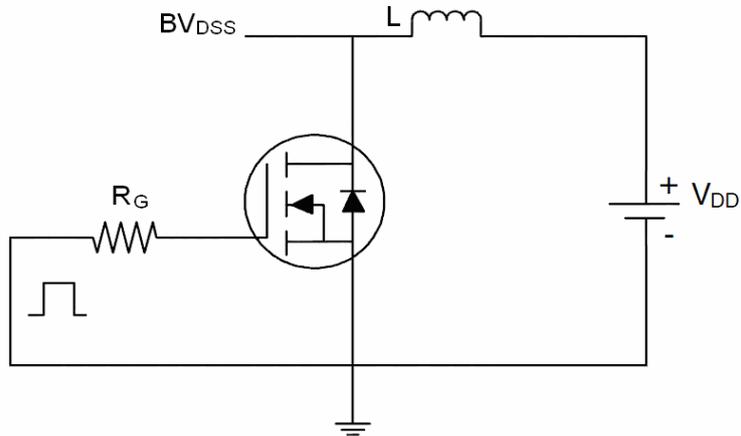
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	115	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.9	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	25	32	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	15	-	S
Dynamic Characteristics (Note 4)						
C_{iss}	Input Capacitance	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2479	-	PF
C_{oss}	Output Capacitance		-	96	-	PF
C_{rSS}	Reverse Transfer Capacitance		-	79	-	PF
Switching Characteristics (Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	9	-	nS
t_r	Turn-on Rise Time		-	9	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	32	-	nS
t_f	Turn-Off Fall Time		-	8	-	nS
Q_g	Total Gate Charge	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$	-	67.2	-	nC
Q_{gs}	Gate-Source Charge		-	9.4	-	nC
Q_{gd}	Gate-Drain Charge		-	15.5	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
I_S	Diode Forward Current (Note 2)	-	-	-	30	A
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 10A$ $di/dt = 100A/\mu\text{s}$ (Note 3)	-	32	-	nS
Q_{rr}	Reverse Recovery Charge		-	53	-	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

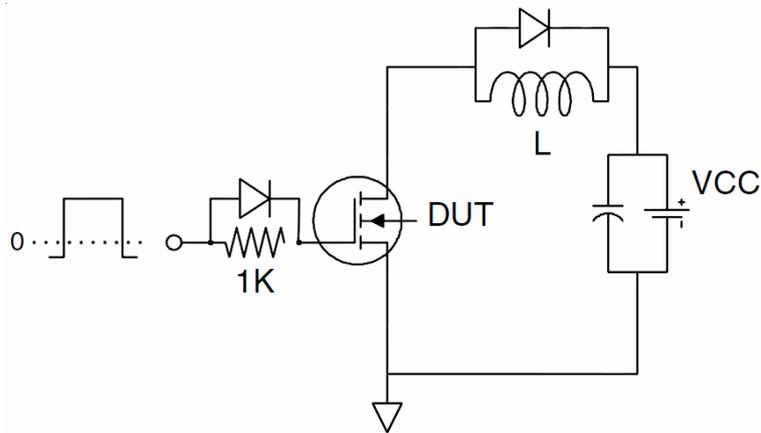
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS Condition : $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$
6. The spike duty cycle 5% max, limited by junction temperature $T_J(\text{MAX})=125^\circ\text{C}$

Test Circuit

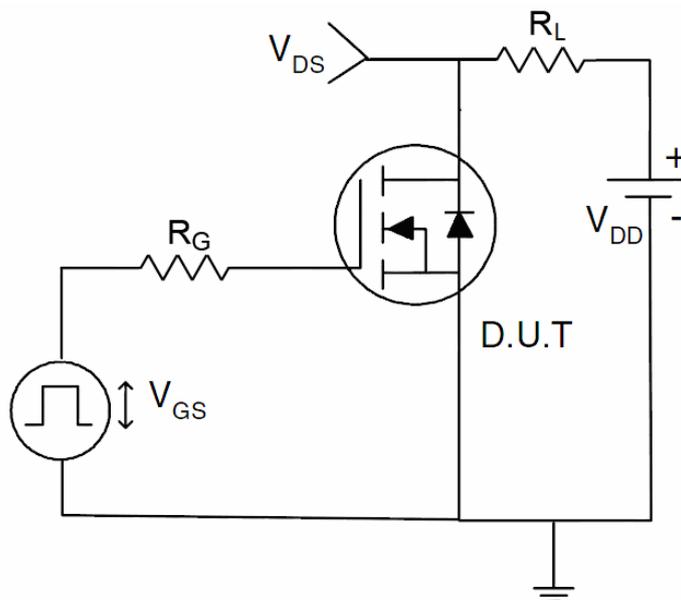
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

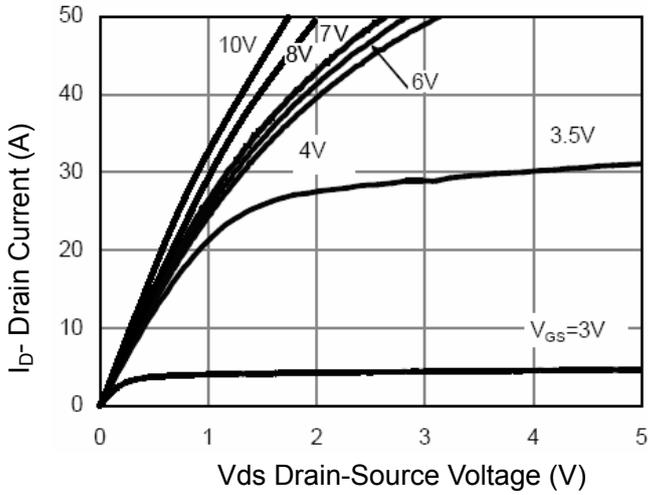


Figure 1 Output Characteristics

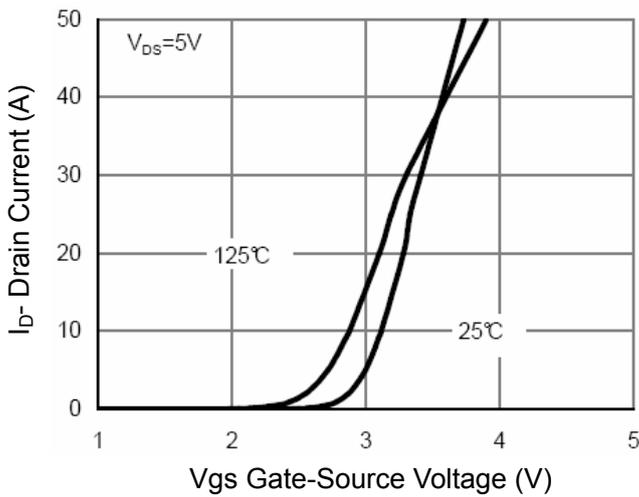


Figure 2 Transfer Characteristics

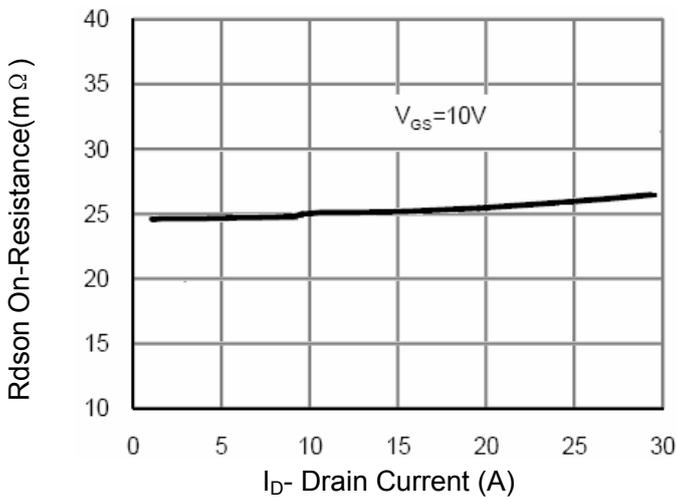


Figure 3 Rdson- Drain Current

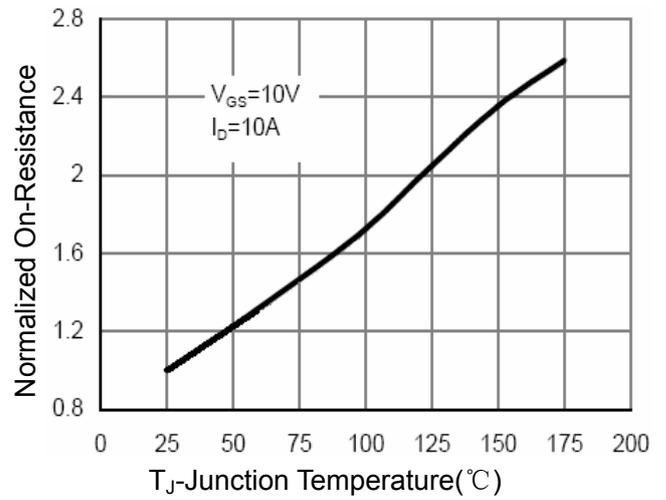


Figure 4 Rdson-Junction Temperature

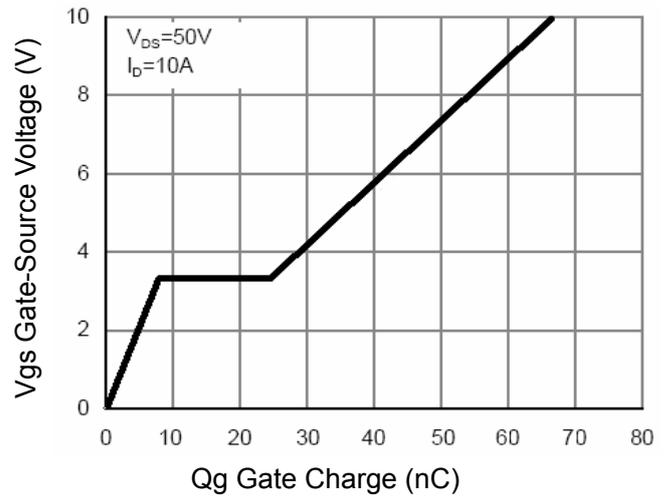


Figure 5 Gate Charge

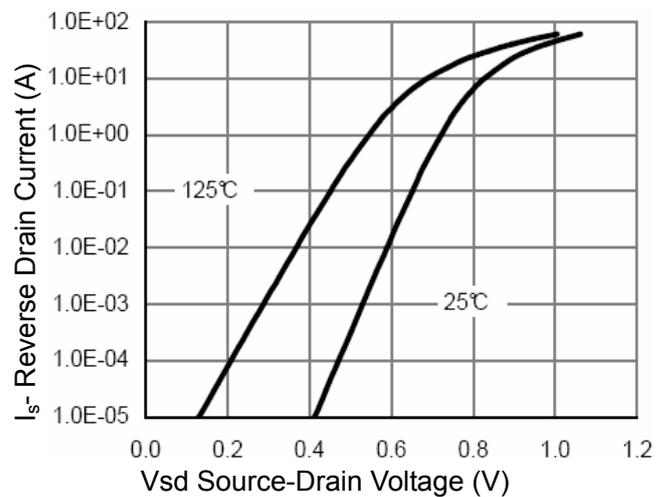


Figure 6 Source- Drain Diode Forward

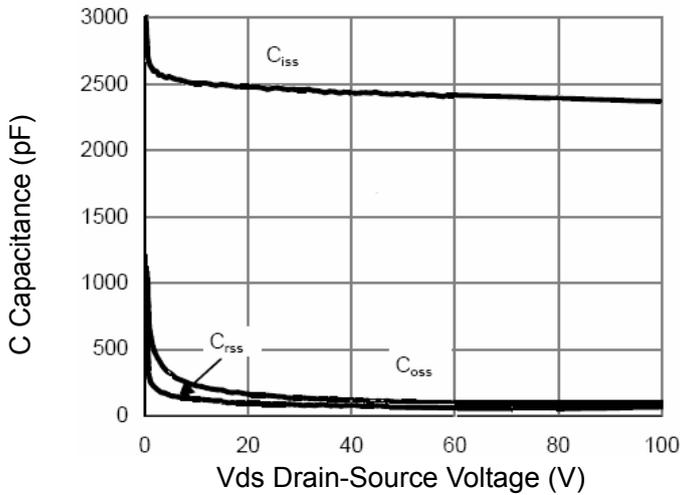


Figure 7 Capacitance vs Vds

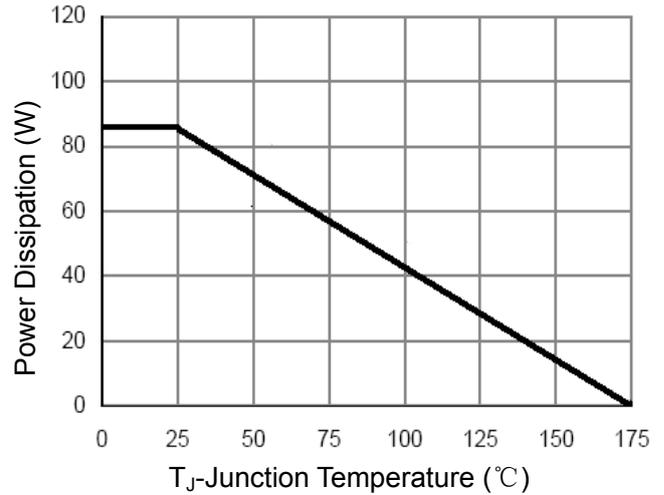


Figure 9 Power De-rating

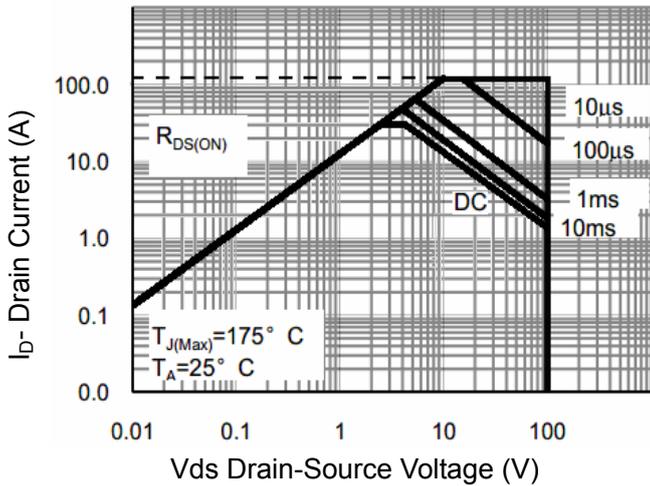


Figure 8 Safe Operation Area

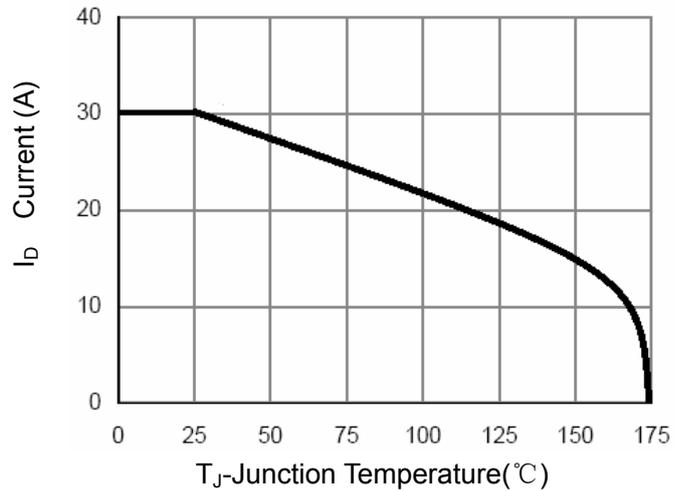


Figure 10 ID Current- Junction Temperature

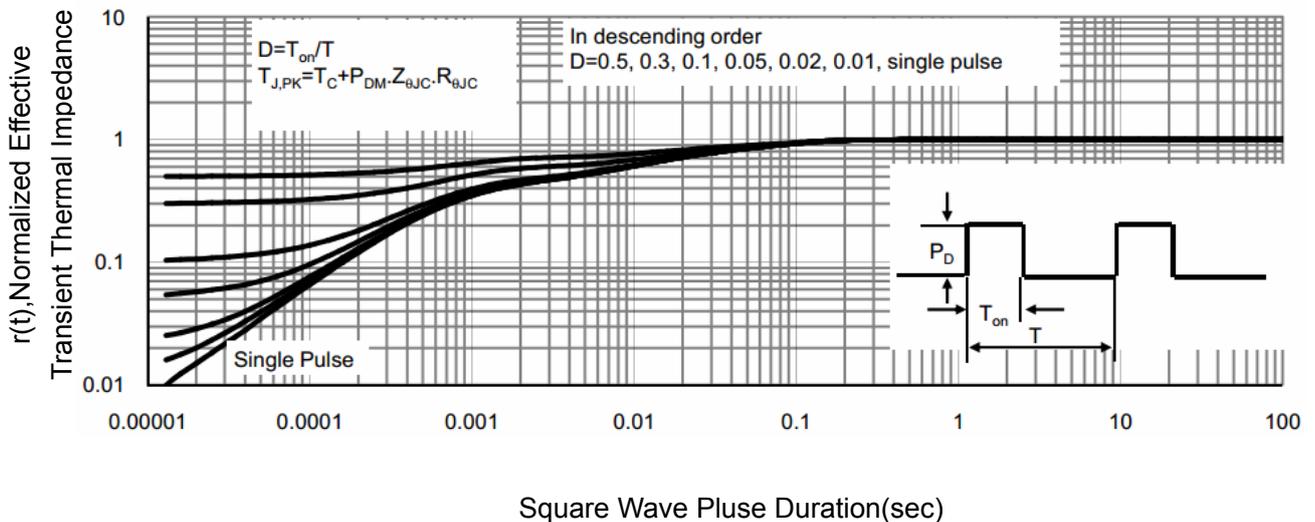
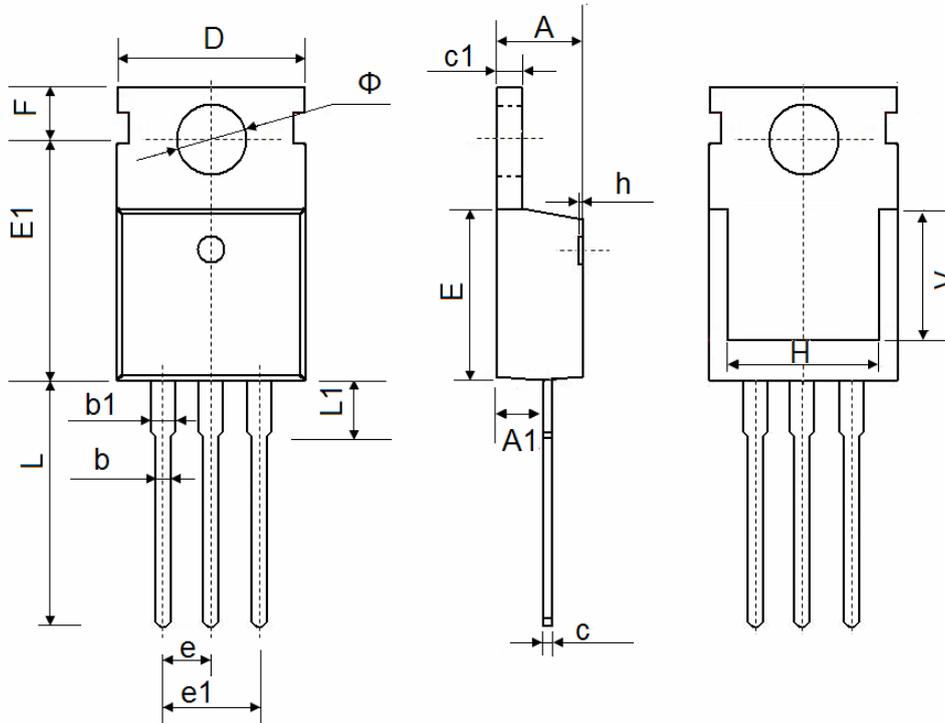


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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