Over-Voltage Protection Load Switch with Surge Protection

FEATURES

- Surge protection
  - IEC 61000-4-5: > 100V
- Integrated low R_{dson} nFET switch: typical 28mΩ
- 4.5A continuous current capability
- Default Over-Voltage Protection (OVP) threshold
  - AW32801: 5.95V
  - AW32805: 6.8V
  - AW32809: 9.98V
  - AW32812: 14V
- OVP threshold adjustable range: 4V to 20V
- Input system ESD protection
  - IEC 61000-4-2 Contact discharge: ±8kV
  - IEC 61000-4-2 Air gap discharge: ±15kV
- Input maximum voltage rating: $29V_{DC}$
- Fast turn-off response: typical 125ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)
- 1.34mm × 1.78mm WLCSP-12 package

APPLICATIONS

- Smartphones
- Tablets
- 5V to 20V Charging Ports

GENERAL DESCRIPTION

The AW328XX family OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to 100V.

The AW328XX features an ultra-low 28mΩ (typ.) R_{dson} nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to $29V_{DC}$.

The default OVP threshold is 5.95V (AW32801), 6.8V (AW32805), 9.98V (AW32809) and 14V (AW32812), the OVP threshold can be adjusted from 4V to 20V through external OVLO pin.

The device features an open-drain output $\overline{ACOK}$, when $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$ and the switch is on, $\overline{ACOK}$ will be driven low to indicate a good power input, otherwise it is high impedance.

This device features over-temperature protection that prevents itself from thermal damaging.

The AW328XX is available in a RoHS compliant 12-bump 1.34mm × 1.78mm WLCSP.

TYPICAL APPLICATION CIRCUIT

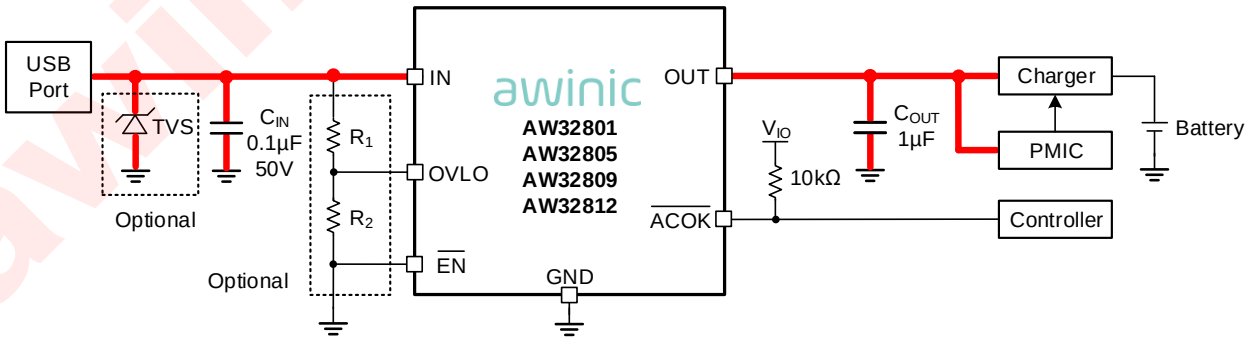


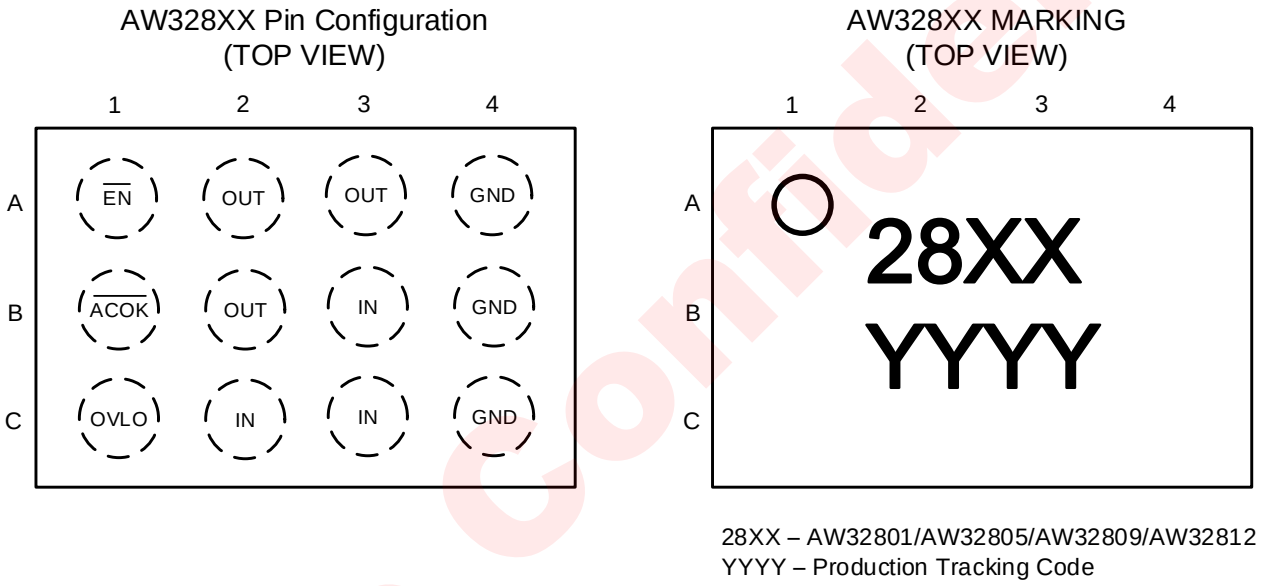
Figure 1 Typical Application Circuit of AW328XX

Note: R_1 and R_2 are used for OVP threshold adjustment, to use default OVP threshold, connect OVLO to ground.

DEVICE COMPARISON TABLE

Device	V_{IN_OVLO} (V)				V_{IN_OVLO} hysteresis (mV)
	Condition	Min.	Typ.	Max.	
AW32805	V_{IN} rising	6.66	6.80	6.94	150
AW32809	V_{IN} rising	9.78	9.98	10.18	210
AW32812	V_{IN} rising	13.7	14.0	14.3	300
AW32801	V_{IN} rising	5.83	5.95	6.07	100

PIN CONFIGURATION AND TOP MARK



28XX – AW32801/AW32805/AW32809/AW32812
YYYY – Production Tracking Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

PIN	NAME	DESCRIPTION
A1	$\overline{EN}$	Enable pin, active low
B1	$\overline{ACOK}$	Power good flag, active-low, open-drain
C1	OVLO	OVP threshold adjustment pin
C2, C3, B3	IN	Switch input and device power supply
A2, A3, B2	OUT	Switch output
A4, B4, C4	GND	Device ground

FUNCTIONAL BLOCK DIAGRAM

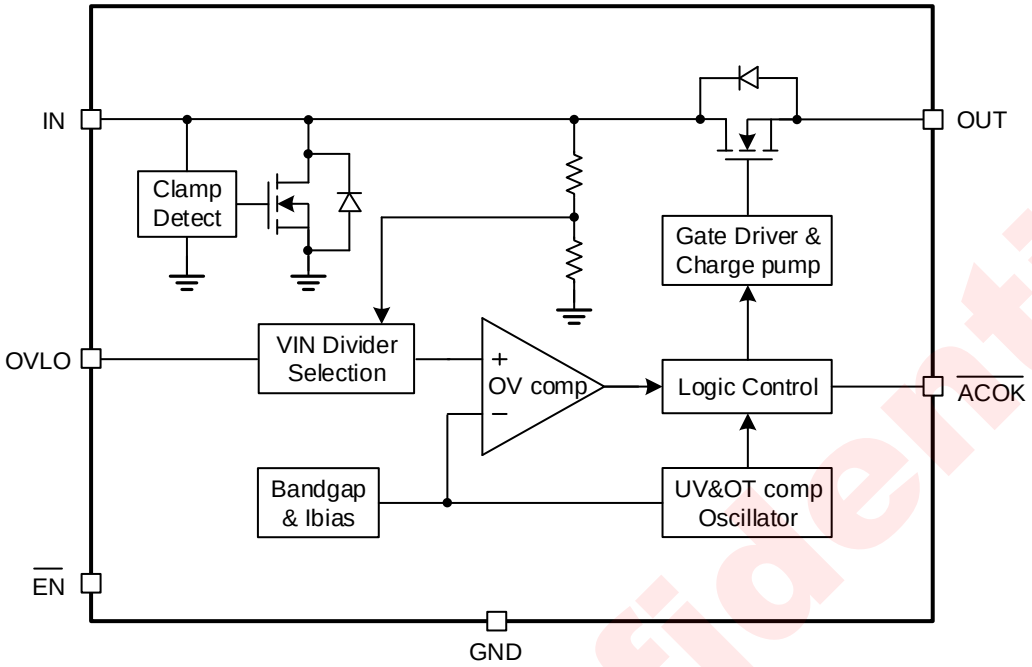


Figure 3 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

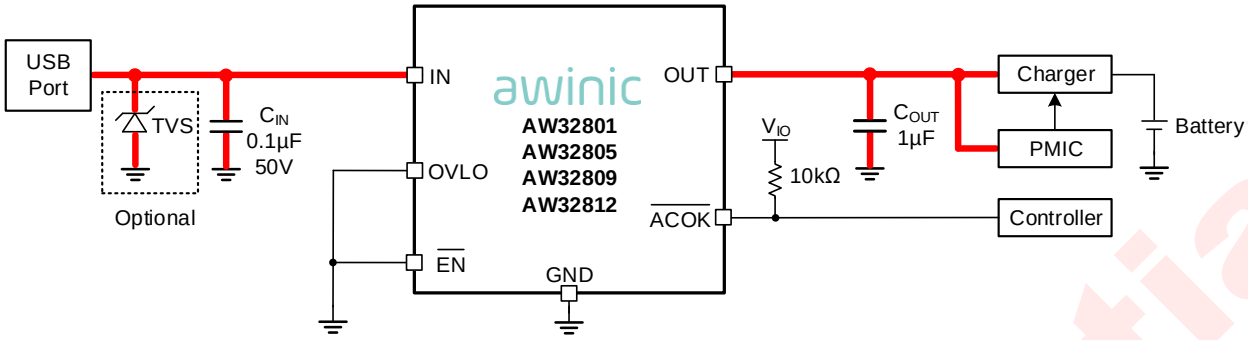


Figure 4 AW328XX Application Circuit
(Using default OVP threshold by connecting OVLO to ground)

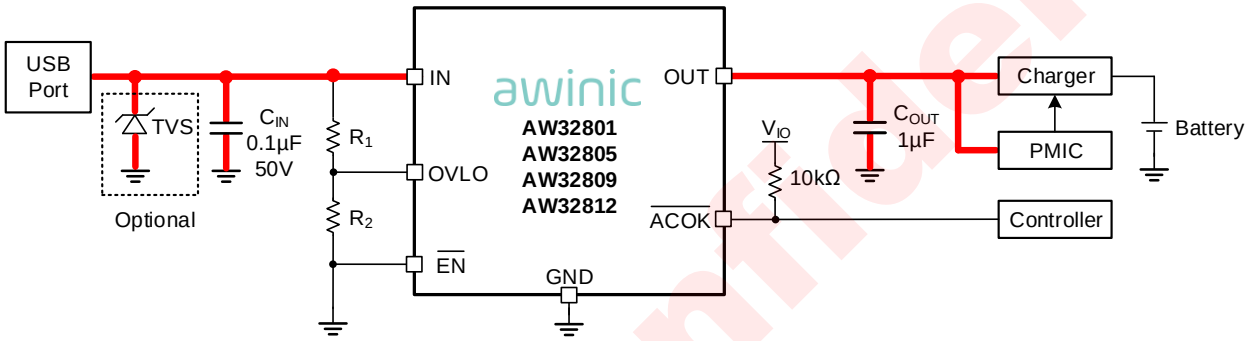


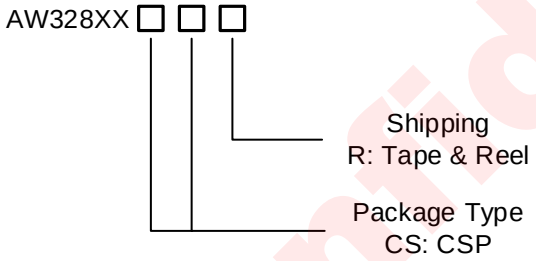
Figure 5 AW328XX Application Circuit
(Using external OVP threshold by connecting OVLO to R_1 and R_2)

Notice for Typical Application Circuits:

1. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. OVLO pin cannot be left floating.
2. If R_1 and R_2 are used to adjust the OVP threshold, in order to speed up the OVP response, $R_1 + R_2 <$ 100kΩ is recommended. It is better to use 1% precision resistors to improve the OVP threshold precision.
3. If $\overline{ACOK}$ is not used, it can be left floating, or short to GND.
4. C_{IN} = 0.1μF is recommended for typical application, larger C_{IN} is also acceptable. The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW328XX is used, the rated voltage of C_{IN} should be 50V.
5. C_{OUT} = 1μF is recommended for typical application, larger C_{OUT} is also acceptable. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 6.8V, the rated voltage of C_{OUT} should be 10V or higher.
6. If the input of AW328XX is required to pass surge voltage greater than 100V, external TVS is needed, the maximum clamping voltage of the TVS should be below 42V.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32801CSR	-40°C～85°C	WLCSP 1.34×1.78-12B	2801	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW32805CSR	-40°C～85°C	WLCSP 1.34×1.78-12B	2805	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW32809CSR	-40°C～85°C	WLCSP 1.34×1.78-12B	2809	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW32812CSR	-40°C～85°C	WLCSP 1.34×1.78-12B	2812	MSL1	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 29V
Input Voltage Range	OVLO	-0.3V to 29V
	$\overline{EN}$	-0.3V to 6V
Output Voltage Range	$\overline{ACOK}$	-0.3V to 6V
	OUT	See(NOTE 2)
Maximum Input Peak Pulse Voltage V_{IN_PUL} (20μs pulse width, repeat 100 times)		42V
Maximum Continuous Current From IN to OUT I_{SW}(NOTE 3)		4.5A
Peak Current From IN to OUT I_{PEAK} (10ms)		8A
Maximum Continuous Forward Current Through the Switch Body Diode I_{DIODE}		1.5A
Junction-to-ambient Thermal Resistance θ_{JA}(NOTE 4)		85°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		165°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
IEC61000-4-2 System ESD on IN (NOTE 5)	Contact Discharge	±8kV
	Air Gap Discharge	±15kV
Human Body Model (All pins, per MIL-STD-883J Method 3015.9) (NOTE 6)		±4kV
Charged Device Model (All pins, per JEDEC EIA/JESD22-C101F)		±1.5kV
Machine Model (All pins, per JEDEC EIA/JESD22-A115)		±400V
Latch-Up		
Test Condition: JEDEC STANDARD No.78C SEPTEMBER 2011		+IT：800mA -IT：-800mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: -0.3V to *29V or V_{IN} + 0.3V, whichever is smaller.*

NOTE3: *Limited by thermal design.*

NOTE4: *Thermal resistance from junction to ambient is highly dependent on PCB layout.*

NOTE5: Test is under C_{IN} = 1μF.

NOTE6: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.*

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, I_{IN}≤ 4.5A and T_A = 25°C.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN_CLAMP}	Input Clamp Voltage	I_{IN} = 10mA			30.3		V
V_{IN}	Input Voltage Range			2.5		28	V
R_{dson}	Switch On Resistance	V_{IN} = 5V, I_{OUT} = 1A, T_A = 25°C			28	37	mΩ
I_Q	Input Quiescent Current	V_{IN} = 5V, I_{OUT} = 0A			65	100	μA
I_{IN_OVLO}	Input Current at Over-voltage Condition	V_{OVLO} = 3V, V_{IN} = 5V, V_{OUT} = 0V			69	110	μA
V_{OVLO_TH}	OVLO Set Threshold	2.5V < V_{IN} < 20V		1.16	1.20	1.24	V
V_{OVLO_RNG}	OVP Threshold Adjustable Range	2.5V < V_{IN} < 20V		4		20	V
V_{OVLO_SEL}	External OVLO Select Threshold	V_{IN} Rising		0.3	0.42	0.50	V
		Hysteresis			0.1		
I_{OVLO}	OVLO Pin Leakage Current	V_{OVLO} = V_{OVLO_TH}		-0.1		0.1	μA
C_{OUT}	Output Load Capacitance					100	μF
Protection							
V_{IN_OVLO}	Default OVP Trip Level	AW32805	V_{IN} Rising	6.66	6.80	6.94	V
			V_{IN} Falling	6.51	6.65		
		AW32809	V_{IN} Rising	9.78	9.98	10.18	
			V_{IN} Falling	9.57	9.77		
		AW32812	V_{IN} Rising	13.7	14.0	14.3	
			V_{IN} Falling	13.4	13.7		
		AW32801	V_{IN} Rising	5.83	5.95	6.07	
			V_{IN} Falling	5.73	5.85		
V_{IN_UVLO}	UVLO Trip Level	V_{IN} Rising			2.25	2.40	V
		V_{IN} Falling			2.10	2.20	
T_{SDN}	Shutdown Temperature				130		°C
T_{SDN_HYS}	Shutdown Temperature Hysteresis				20		°C
Digital Logical Interface							
V_{OL}	$\overline{ACOK}$ Output Low Voltage	I_{SINK} = 1mA				0.4	V
$I_{LEAK\_\overline{ACOK}}$	$\overline{ACOK}$ Leakage Current	V_{IO} = 5V, $\overline{ACOK}$ De-asserted		-0.5		0.5	μA
V_{IH}	$\overline{EN}$ Input High Voltage			1.2			V
V_{IL}	$\overline{EN}$ Input Low Voltage					0.5	V
$I_{LEAK\_\overline{EN}}$	$\overline{EN}$ Leakage Current	$V_{\overline{EN}}$ = 5V		-1		10	μA

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, I_{IN}≤ 4.5A and T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Timing Characteristics (Figure 6)						
t_{DEB}	Debounce Time	From V_{IN} > V_{IN_UVLO} to 10% V_{OUT}, $\overline{EN}$ Low		15		ms
t_{STAT}	Start-up Time	From V_{IN} > V_{IN_UVLO} to $\overline{ACOK}$ low, $\overline{EN}$ Low		30		ms
t_{ON}	Switch Turn-on Time	R_L = 100Ω, C_L = 22μF, V_{OUT} from 10% V_{IN} to 90% V_{IN}		1		ms
t_{OFF}	Switch Turn-off Time	R_L = 100Ω, C_L = 0μF, V_{IN} > V_{IN_OVLO} to V_{OUT} Stop Rising		125		ns

TIMING DIAGRAM

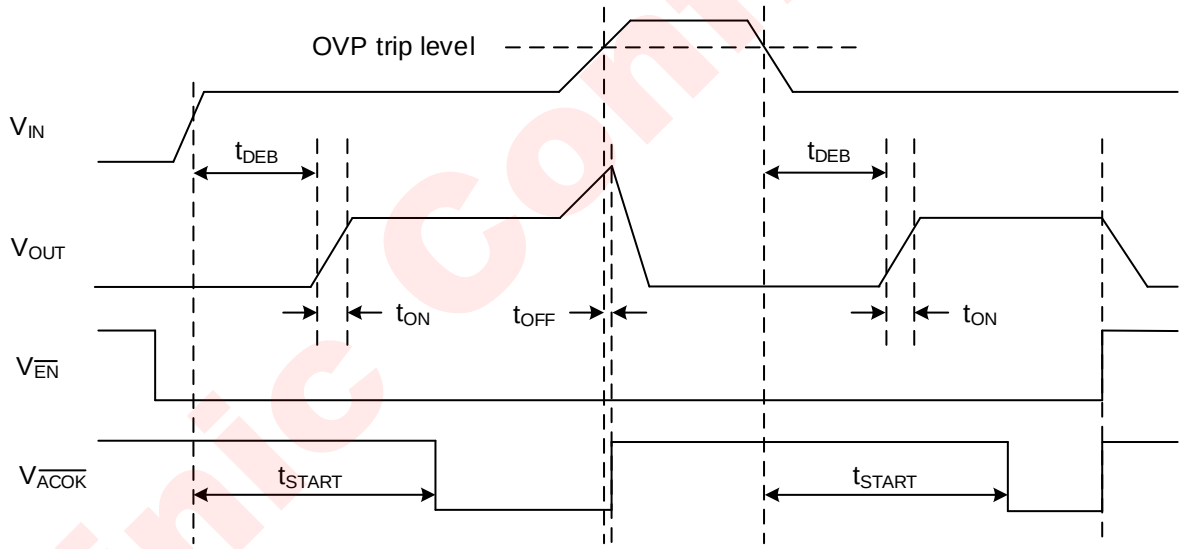


Figure 6 AW328XX Timing Diagram

TYPICAL CHARACTERISTICS

Table 1 TABLE OF FIGURES

V_{IN} = 5V, $V_{\overline{EN}}$ = 0V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25℃ unless otherwise specified.

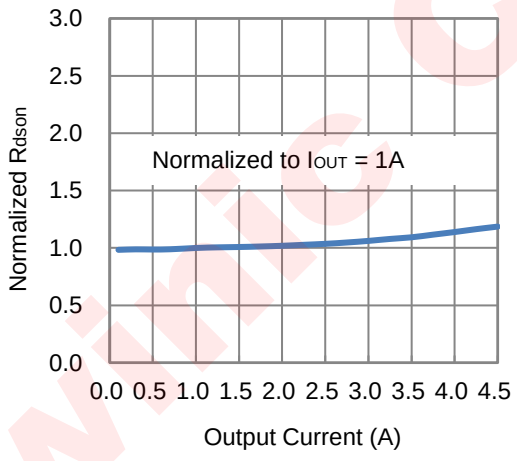


Figure 7. Normalized R_{dson} vs. Output Current

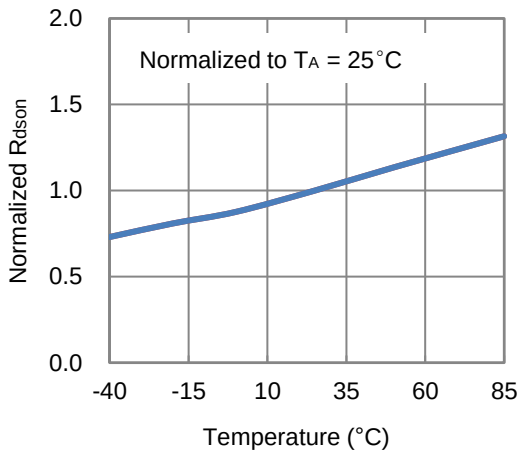


Figure 8. Normalized R_{dson} vs. Temp. (I_{OUT} = 1A)

TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, $V_{\overline{EN}}$ = 0V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25℃ unless otherwise specified.

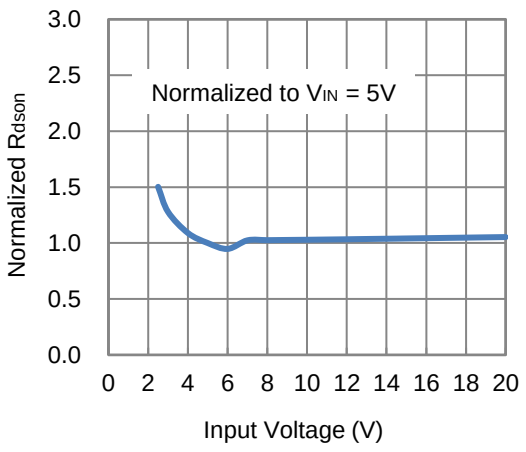


Figure 9. Normalized R_{dson} vs. Input Voltage (I_{OUT} = 1A)

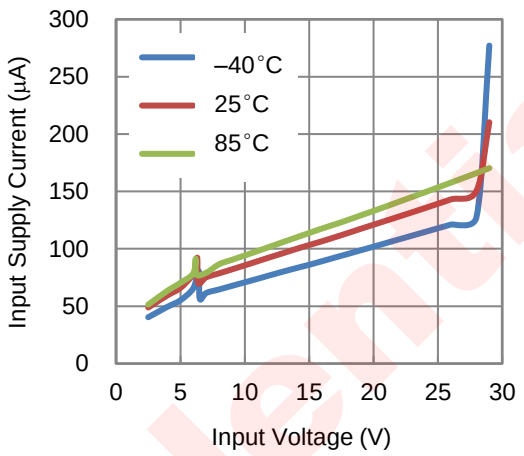


Figure 10. Input Supply Current vs. Supply Voltage

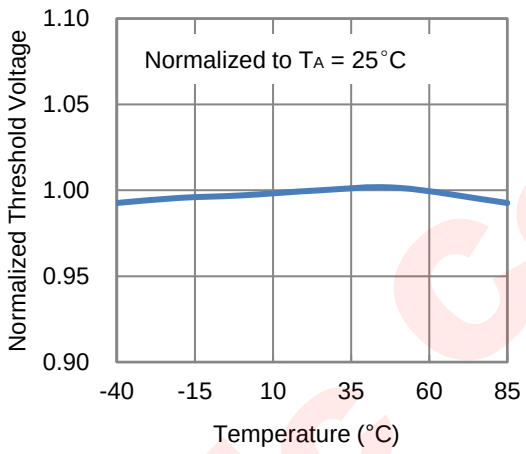


Figure 11. Normalized Internal OVP Threshold vs. Temp.

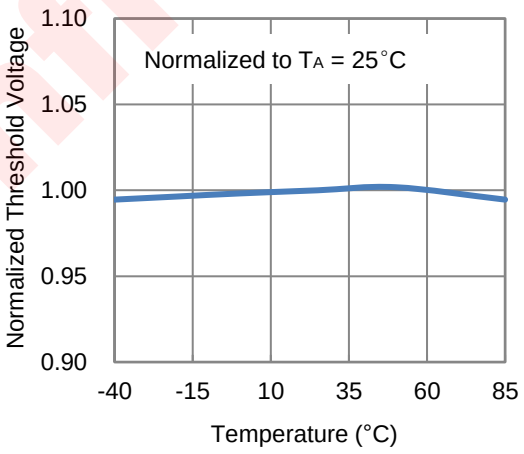


Figure 12. Normalized External OVLO Set OVP Threshold vs. Temp.

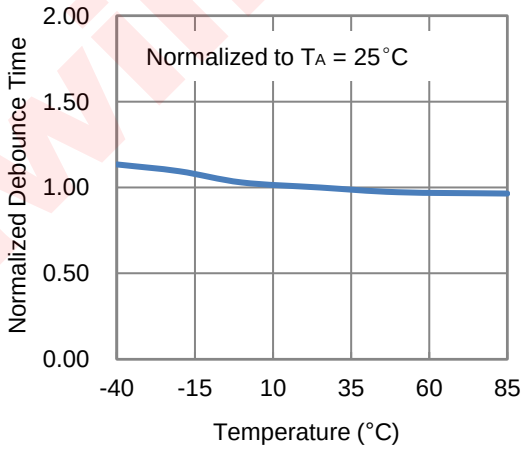


Figure 13. Normalized Debounce Time vs. Temp.

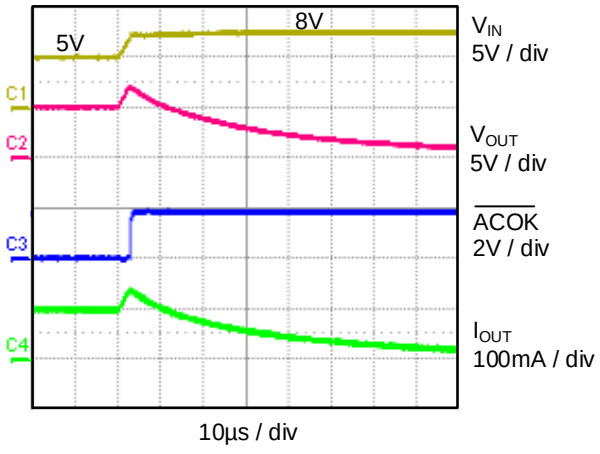


Figure 14. Over-Voltage Response (AW32805)

TYPICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V, $V_{\overline{EN}}$ = 0V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25℃ unless otherwise specified.

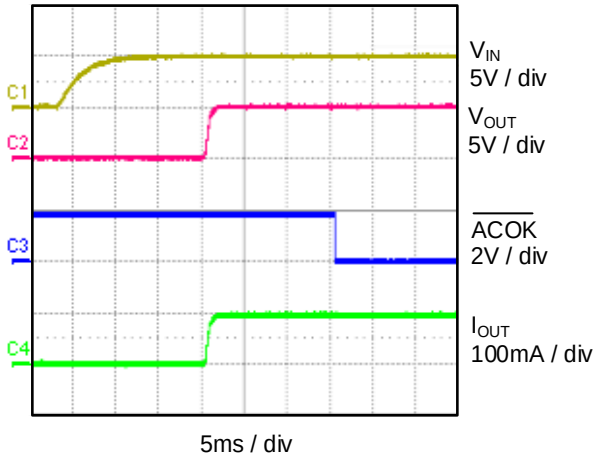


Figure 15. Power-up (C_{OUT} = 1μF, 100mA load)

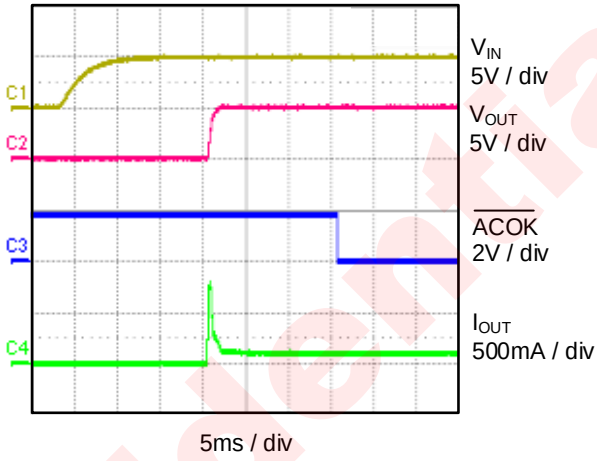


Figure 16. Power-up (C_{OUT} = 100μF, 100mA load)

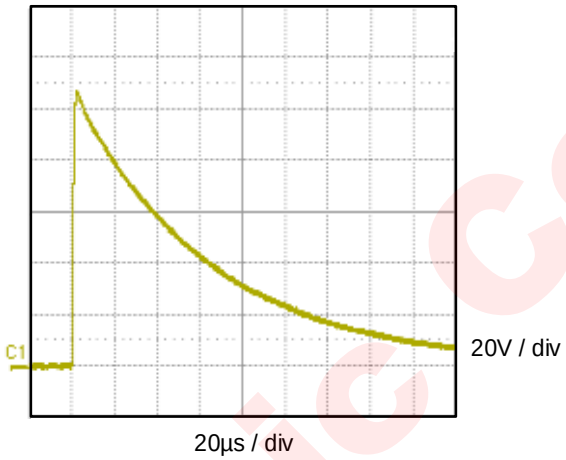


Figure 17. 108V Surge Without Device

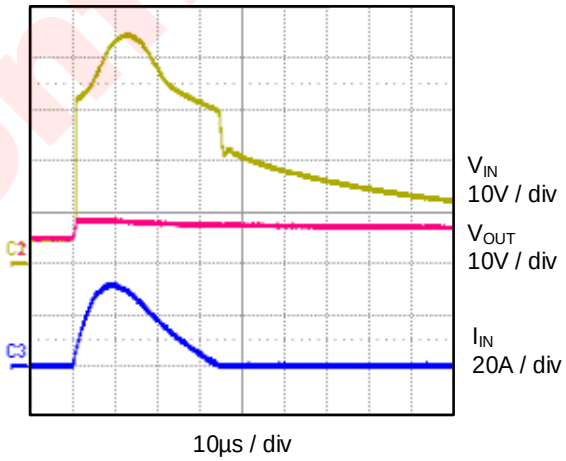


Figure 18. 108V Surge With Device (AW32805)

DETAILED FUNCTIONAL DESCRIPTION

Device Operation

If the AW328XX is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. $\overline{ACOK}$ will be driven low about 30ms after V_{IN} valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 125ns. If $\overline{EN}$ is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Surge Protection

The AW328XX integrates a clamp circuit to suppress input surge voltage. For surge voltages between V_{IN_OVLO} and V_{IN_CLAMP}, the switch will be turned off but the clamp circuit will not work. For surge voltages greater than V_{IN_CLAMP}, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 125ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

OVP Threshold Adjustment

If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

The adjustment range is 4V to 20V. When the OVLO pin voltage V_{OVLO} exceeds V_{OVLO_SEL}(0.42V typical), V_{OVLO} is compared with the reference voltage V_{OVLO_TH} (1.2V typical) to judge whether input supply is over-voltage. For example, if we select R_1 = 51kΩ and R_2 = 12.4kΩ, then the new OVP threshold calculated from the above formula is 6.14V.

$\overline{ACOK}$ Output

The device features an open-drain output $\overline{ACOK}$, it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, $\overline{ACOK}$ will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, or $\overline{EN}$ is pulled high, the switch will be turned off and $\overline{ACOK}$ will be pulled high.

USB On-The-Go (OTG) Operation

If V_{IN} = 0V and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When $V_{IN} > V_{IN\_UVLO}$, internal charge pump begins to open the load switch after debounce time. After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

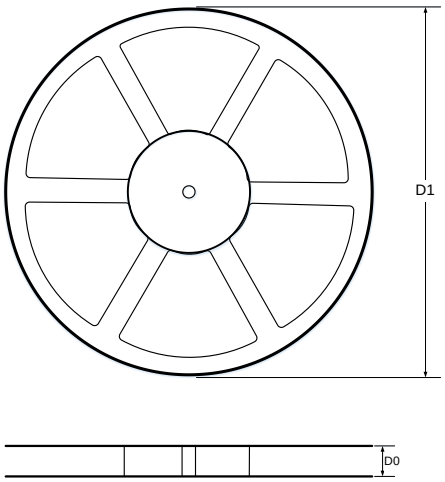
PCB LAYOUT CONSIDERATION

To make full use of the performance of AW328XX, the guidelines below should be followed.

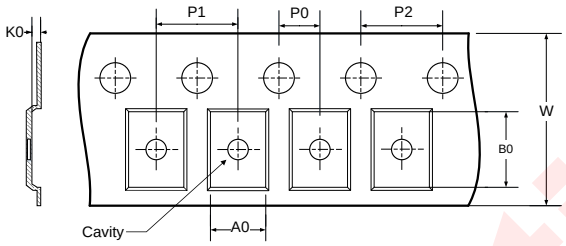
1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW328XX) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW328XX) and close to OUT pin.
2. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.
3. If R_1 and R_2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.
4. The power trace from USB connector to AW328XX may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.
5. Use rounded corners on the power trace from USB connector to AW328XX to decrease EMI coupling.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

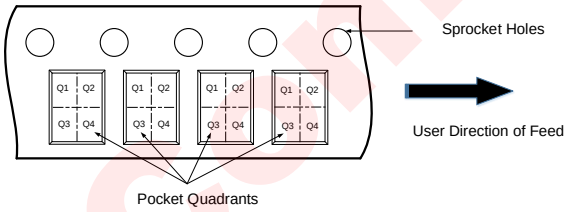


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

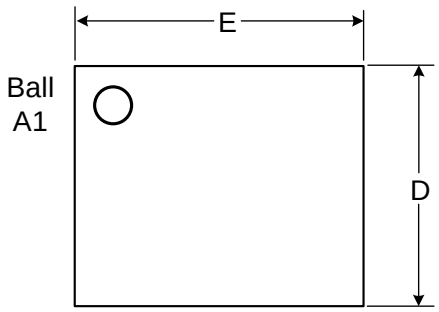


All Dimensions are normal

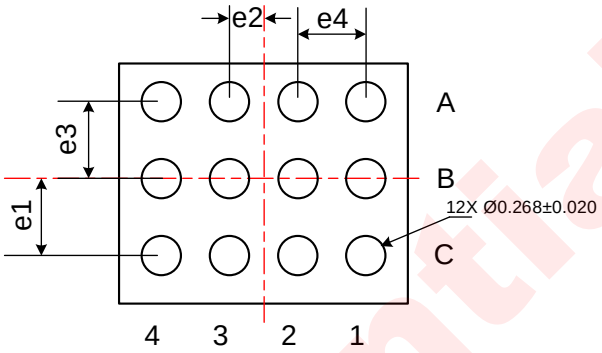
Device	Package(mm)	Pins	Quantity Per Reel	D1：Reel Diameter (mm)	D0：Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
AW328XXCSR	WLCSP 1.34x1.78	12	3000	178.00	9.00	1.46	1.90	0.81	2.00	4.00	4.00	8.00	Q2

PACKAGE DESCRIPTION

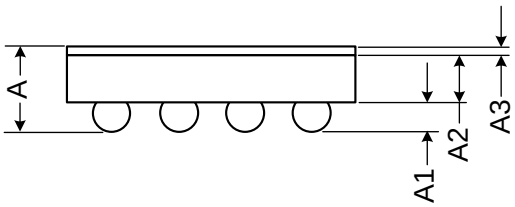
TOP VIEW



BOTTOM VIEW



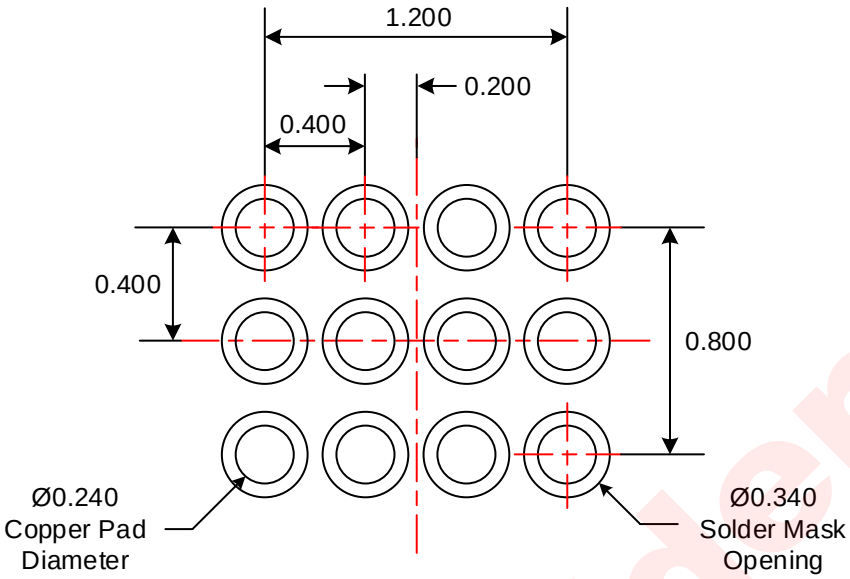
SIDE VIEW



Symbol	NOM	Tolerance
A	0.575	±0.055
A1	0.195	±0.020
A2	0.340	±0.025
A3	0.040	±0.010
D	1.340	±0.025
E	1.780	±0.025
e1	0.400	NA
e2	0.200	NA
e3	0.400	NA
e4	0.400	NA

Unit: mm

LAND PATTERN DATA



NSMD Pad Type
Unit: mm

REFLOW

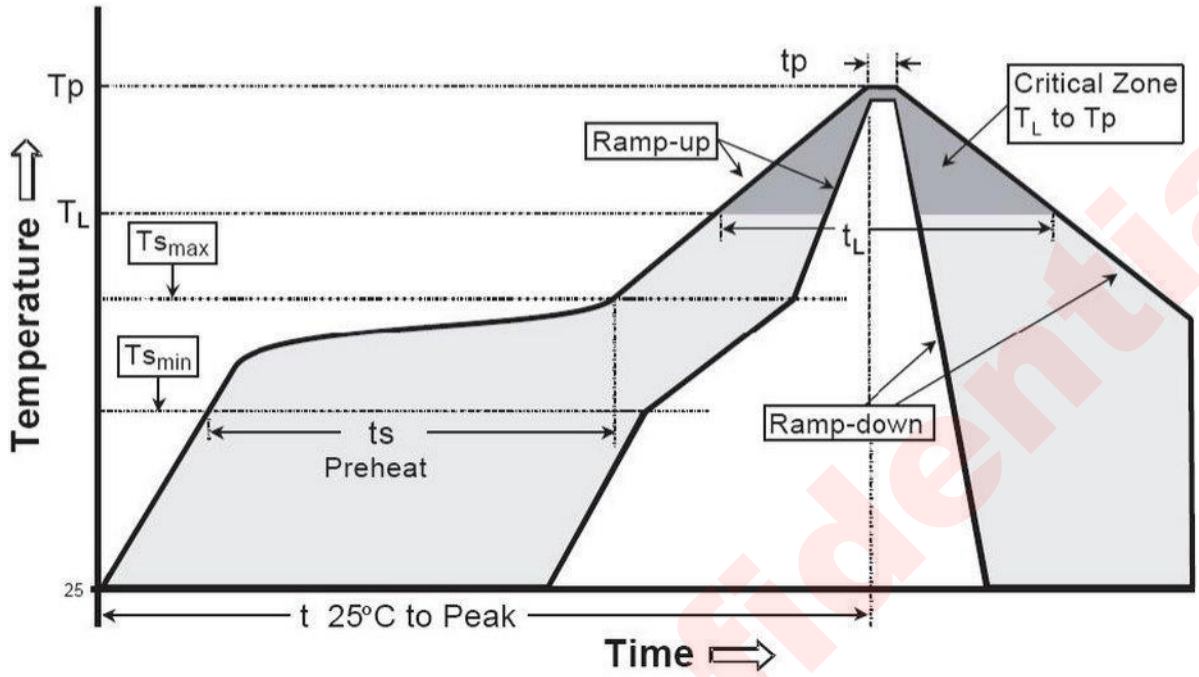


Figure 19 Package Reflow Standard Profile

Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	250-260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 4°C /sec
Time from 25°C to peak temp	Max. 8min

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW328XX adopted the Pb-Free assembly.

REVISION HISTORY

Version	Date	Change Record
V0.9	November 2016	Datasheet v0.9 released.
V1.0	October 2016	Datasheet v1.0 released.
V1.1	February 2018	1. Datasheet template changed. 2. Input voltage range modified. 3. Notice for typical application circuits added. 4. V_{IN_PUL}, I_{PEAK}, I_{DIODE} added in absolute maximum ratings table 5. PCB layout consideration added. 6. Land pattern data added. 7. Reflow information added.
V1.2	June 2018	1. Typical application circuit modified. 2. Notice for typical application circuits #6 added. 3. Package information in ordering information modified. 4. Tape and reel information modified. 5. Package description modified. 6. Reflow curve and spec modified.

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