

N-Channel Enhancement Mode Field Effect Transistor with Schottky Diode

General Description

The VBA1310S uses advanced trench technology to provide excellent $R_{DS(ON)}$, shoot-through immunity and body diode characteristics. This device is suitable for use as a synchronous switch in PWM applications. The co-packaged Schottky Diode boosts efficiency further.

Features

 $V_{DS}(V) = 30V$

 $I_D = 12 \text{ A } (V_{GS} = 10 \text{V})$

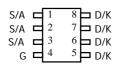
 $R_{DS(ON)} < 11.5 m\Omega (V_{GS} = 10V)$

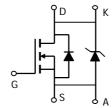
 $R_{DS(ON)} < 13m\Omega (V_{GS} = 4.5V)$

SCHOTTKY

VDS (V) = 30V, IF = 3A, VF<0.5V@1A

SOIC-8





Absolute Maximum Ratings T _A =25°C unless otherwise noted									
Parameter		Symbol	MOSFET	Schottky	Units				
Drain-Source Voltage		V_{DS}	30		V				
Gate-Source Voltage		V_{GS}	±12		V				
	T _A =25°C	1	12						
Continuous Drain Current ^A	T _A =70°C	- I _D	10.4		Α				
Pulsed Drain Current ^B		I _{DM}	40						
Schottky reverse voltage		V_{KA}		30	V				
	T _A =25°C	I_		4.4					
Continuous Forward Current ^A	T _A =70°C	- I _F		3.2	Α				
Pulsed Diode Forward Current ^B		I _{FM}		30					
	T _A =25°C	P _D	3.1	3.1	W				
Power Dissipation	T _A =70°C] 'D	2	2					
Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 150	-55 to 150	°C				

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Thermal Characteristics						
Parameter		Symbol	Тур	Max	Units	
Maximum Junction-to-Ambient ^A	t ≤ 10s	$R_{\theta JA}$	28	40	°C/W	
Maximum Junction-to-Ambient ^A	Steady-State	⊢ N _θ JA	54	75	°C/W	
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	21	30	°C/W	

Thermal Characteristics: Schottky						
Parameter		Symbol	Тур	Max	Units	
Maximum Junction-to-Ambient ^A	t ≤ 10s	$R_{\theta JA}$	36	40	°C/W	
Maximum Junction-to-Ambient ^A	Steady-State	N _θ JA	67	75	°C/W	
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	25	30	°C/W	

A: The value of R_{BJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T $_A$ =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t \leq 10s thermal resistance rating. B: Repetitive rating, pulse width limited by junction temperature.

- C. The R $_{\theta JA}$ is the sum of the thermal impedence from junction to lead R $_{\theta JL}$ and lead to ambient.
- D. The static characteristics in Figures 1 to 6 are obtained using 80 $\,\mu s$ pulses, duty cycle 0.5% max.
- E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T $_A$ =25°C. The SOA curve provides a single pulse rating.

 F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop,
- F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately.



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Тур	Max	Units
STATIC P	PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		30			V
	Zone Cote Veltore Ducin Comment	V _R =30V			0.007		
	Zero Gate Voltage Drain Current. (Set by Schottky leakage)	V _R =30V, T _J =125°C			3.2		mA
		V _R =30V, T _J =150°C		12			
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_{D}=250\mu A$		0.5		2.0	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V		40			Α
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, ID=13A			8.0		m0
			T _J =125°C		11.0		mΩ
		V _{GS} =4.5V, I _D =12.2A			9.0		mΩ
g FS	Forward Transconductance	V _{DS} =5V, I _D =13A		30	37		S
V_{SD}	Diode + Schottky Forward Voltage	I _S =1A,V _{GS} =0V			0.45	0.5	V
Is	Maximum Body-Diode + Schottky Continuous Current					5	Α
DYNAMIC	PARAMETERS		<u> </u>				
C _{iss}	Input Capacitance				3656		pF
Coss	Output Capacitance (FET+Schottky)	V _{GS} =0V, V _{DS} =15V, f=1MHz			322		pF
C _{rss}	Reverse Transfer Capacitance				168		pF
R_g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz			0.86	1.1	Ω
SWITCHI	NG PARAMETERS		<u> </u>				
Q _g (4.5V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =13A			30.5	36	nC
Q_{gs}	Gate Source Charge				4.6		nC
Q_{gd}	Gate Drain Charge				8.6		nC
t _{D(on)}	Turn-On DelayTime				6.2	9	ns
t _r	Turn-On Rise Time	V_{GS} =10V, V_{DS} =15V, R_L =1.1 Ω , R_{GEN} =0 Ω			4.8	7	ns
t _{D(off)}	Turn-Off DelayTime				55	75	ns
t _f	Turn-Off Fall Time				7.3	11	ns
t _{rr}	Body Diode+Schottky Reverse Recovery Time	I _F =13A, dI/dt=100A/μs			20.3	25	ns
Q _{rr}	Body Diode+Schottky Reverse Recovery Charge	I _F =13A, dI/dt=100A/μs			8.4	12.5	nC

A: The value of R_{0JA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T $_A$ =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t $_1$ ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R $_{\theta JA}$ is the sum of the thermal impedence from junction to lead R $_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80 $\,\mu s$ pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with T _A=25°C. The SOA curve provides a single pulse rating.

F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop, capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately Rev5: August 2005.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

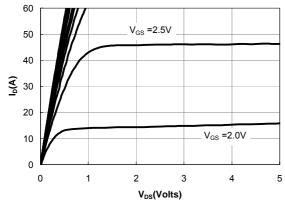


Figure 1: On-Regions CharacteristiCS

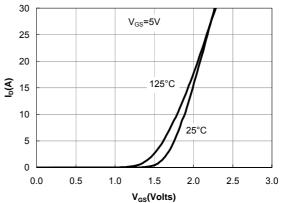


Figure 2: Transfer Characteristics

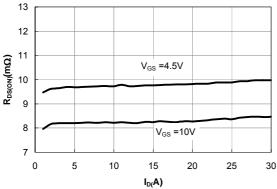


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

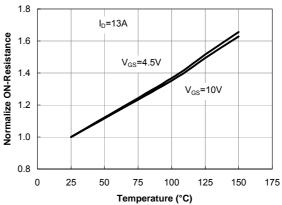


Figure 4: On-Resistance vs. Junction Temperature

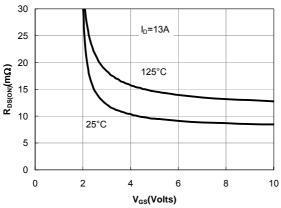


Figure 5: On-Resistance vs. Gate-Source Voltage

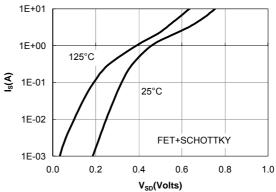


Figure 6: Body-Diode Characteristics (Note F)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

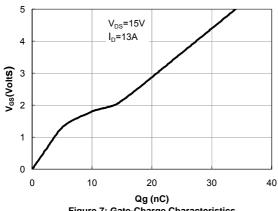


Figure 7: Gate-Charge Characteristics

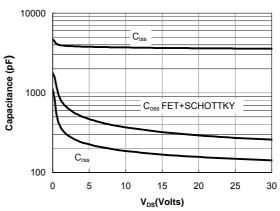


Figure 8: Capacitance Characteristics

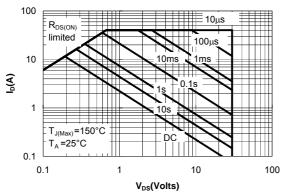


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

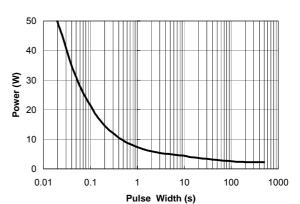


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

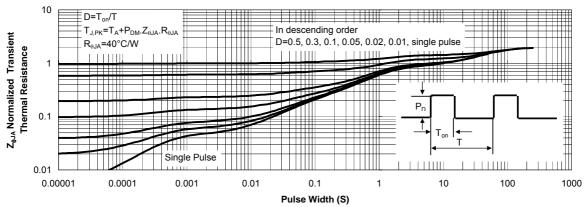
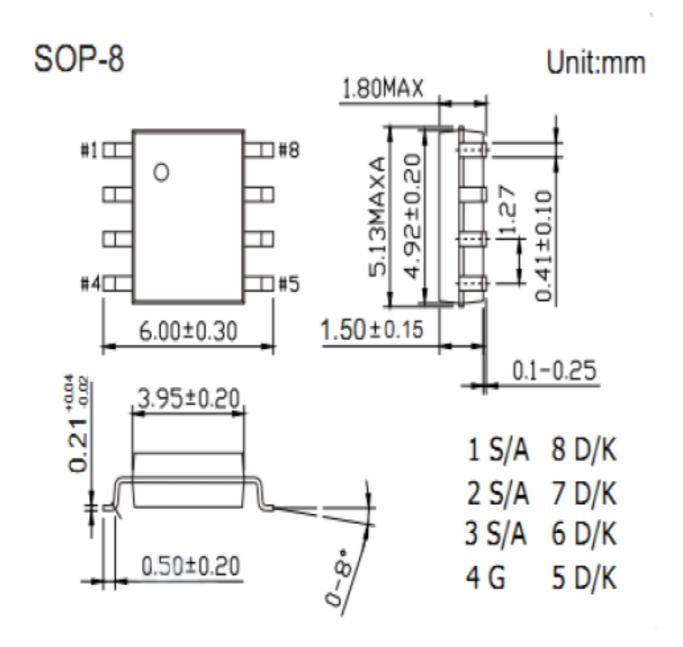


Figure 11: Normalized Maximum Transient Thermal Impedence



SOIC (NARROW): 8-LEAD





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