74HC32; 74HCT32

Quad 2-input OR gate Rev. 7 — 30 September 2019

Product data sheet

1. General description

The 74HC32; 74HCT32 is a quad 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of $V_{\rm CC}$.

2. Features and benefits

- Complies with JEDEC standard JESD7A
- Input levels:
 - For 74HC32: CMOS level
 - For 74HCT32: TTL level
- · Symmetrical output impedance
- · High noise immunity
- · Low power dissipation
- · Balanced propagation delays
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

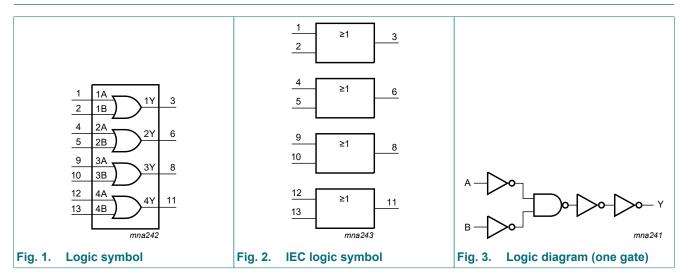
3. Ordering information

Table 1. Ordering information

Type number	Package				
	Temperature range	Name	Description	Version	
74HC32D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1	
74HCT32D			body width 3.9 mm		
74HC32DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads;	SOT337-1	
74HCT32DB			body width 5.3 mm		
74HC32PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package;	SOT402-1	
74HCT32PW			14 leads; body width 4.4 mm		
74HC32BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal	SOT762-1	
74HCT32BQ			enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm		

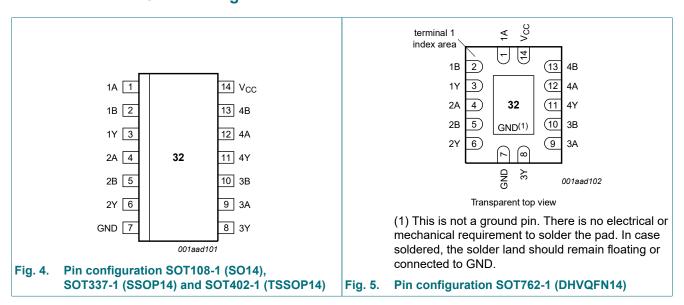


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Table 2. Fill description		
Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10,13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

Input		Output
nA	nB	nY
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT337-1 (SSOP14) packages: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT402-1 (TSSOP14) packages: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) packages: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC32			Unit		
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For SOT108-1 (SO14) packages: Ptot derates linearly with 10.1 mW/K above 100 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC32	1									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	_	3.7	-	V
		I_{O} = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
	I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V	
		I_{O} = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74НСТ3	2			ı		'		l	'	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	8.0	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	l _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι _Ο = 20 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA	-	0.15	0.25	-	0.33	-	0.4	V

Symbol	Parameter	Conditions		25 °C		-40 °C to	+85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
II	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	430	-	540	-	590	μА
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 7.

Symbol	Parameter	Conditions			25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Min	Тур	Max	Max	Max		
74HC32								'	
t _{pd}	propagation delay	nA, nB to nY; see Fig. 6	[1]						
		V _{CC} = 2.0 V		-	22	90	115	135	ns
		V _{CC} = 4.5 V		-	8	18	23	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	6	-	-	-	ns
		V _{CC} = 6.0 V		-	6	15	20	23	ns
t _t	transition time	see Fig. 6	[2]						
		V _{CC} = 2.0 V		-	19	75	95	110	ns
		V _{CC} = 4.5 V		-	7	15	19	22	ns
		V _{CC} = 6.0 V		-	6	13	16	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	[3]	-	16	-	-	-	pF
74HCT3	2							'	
t _{pd}	propagation delay	nA, nB to nY; see Fig. 6	[1]						
		V _{CC} = 4.5 V		-	11	24	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	9	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 6</u>	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[3]	-	28	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH}.
 [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

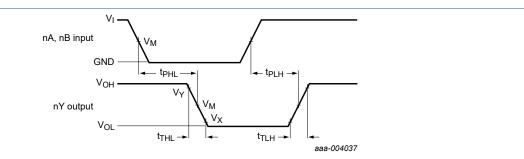
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

10.1. Waveforms



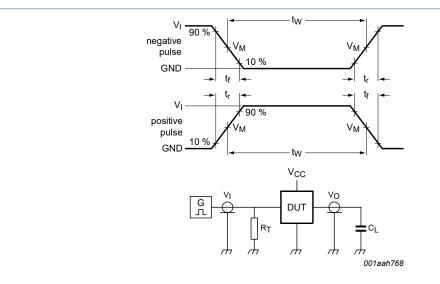
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Input to output propagation delays and output transition times

Table 8. Measurement points

Туре	Input	Output	Output						
	V _M	V _M	V _X	V _Y					
74HC32	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}					
74HCT32	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}					



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

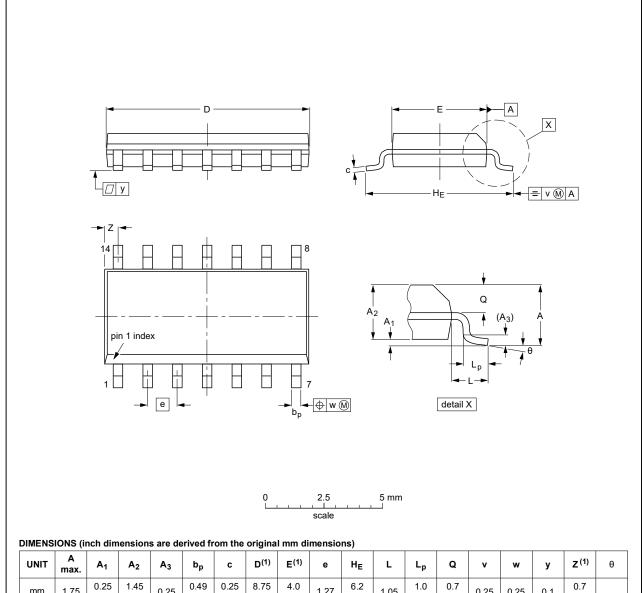
Table 9. Test data

Туре	Input		Load	Test
	V _I	t _r , t _f	CL	
74HC32	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT32	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	Α3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	OUTLINE REFERENCES					ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

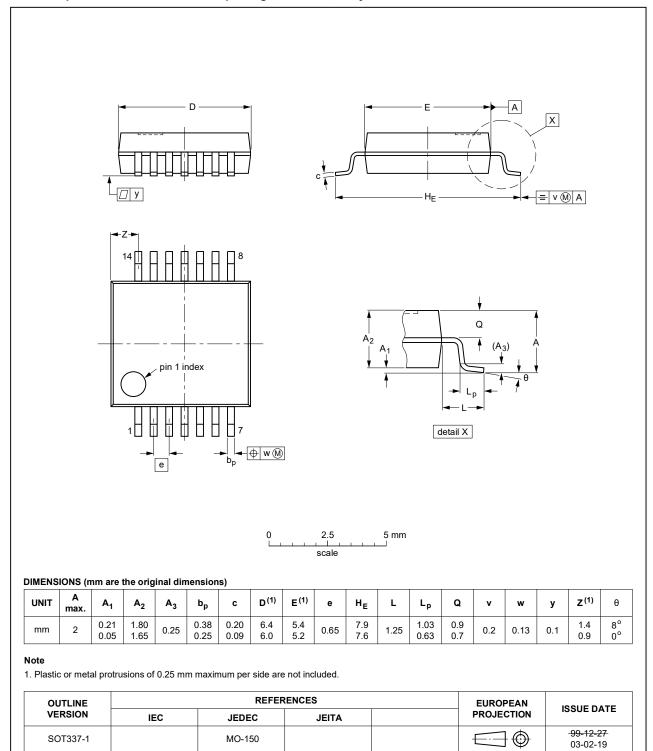
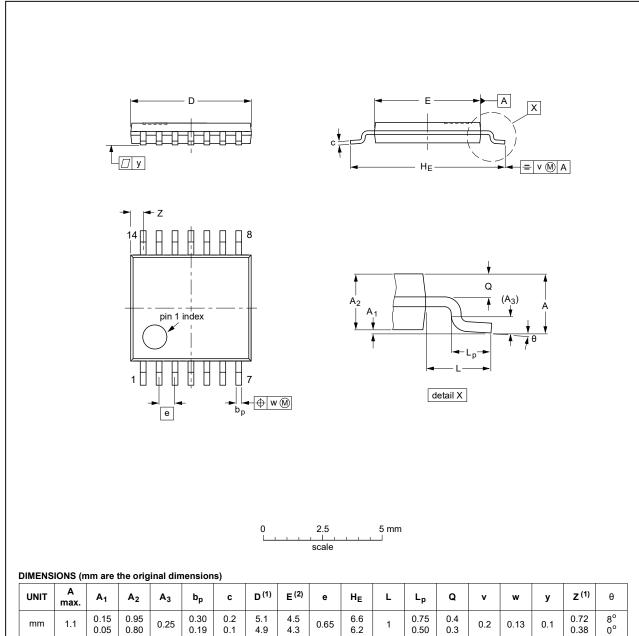


Fig. 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig. 10. Package outline SOT402-1 (TSSOP14)

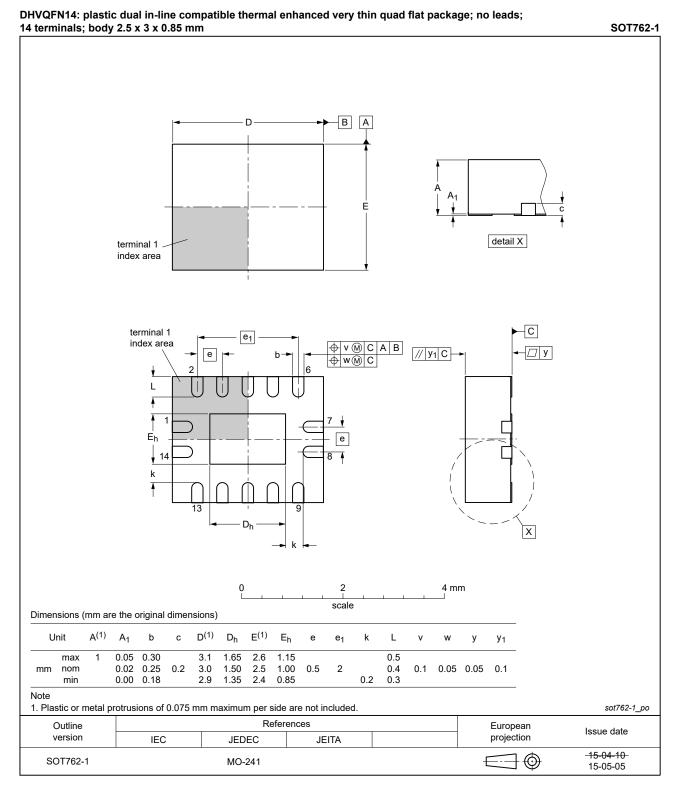


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC_HCT32 v.7	20190930	Product data sheet	-	74HC_HCT32 v.6				
Modifications:	guidelines o Legal texts	of this data sheet has beer of Nexperia. have been adapted to the rating values for P _{tot} total p	new company nar	ne where appropriate.				
74HC_HCT32 v.6	20151203	Product data sheet	-	74HC_HCT32 v.5				
Modifications:	Type number	Type numbers 74HC32N and 74HCT32N (SOT27-1) removed.						
74HC_HCT32 v.5	20120904	Product data sheet	-	74HC_HCT32 v.4				
Modifications:	guidelines of NXP Sen	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 						
74HC_HCT32 v.4	20031212	Product specification	-	74HC_HCT32 v.3				
74HC_HCT32 v.3	20030829	Product specification	-	74HC_HCT32_CNV v.2				
74HC_HCT32_CNV v.2	19970827	Product specification	-	-				

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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