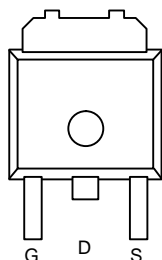


## N-Channel 40-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a, e</sup>	$Q_g$ (Typ)
40	0.013 at $V_{GS} = 10$ V	55	42 nC
	0.018 at $V_{GS} = 4.5$ V	45	

TO-252



Top View

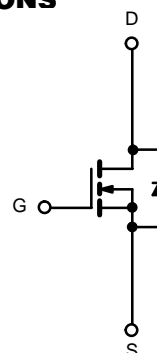
### FEATURES

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2011/65/EU


**RoHS**  
 COMPLIANT

### APPLICATIONS

- OR-ing
- Server
- DC/DC



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$ 55 <sup>a, e</sup>	A
		$T_C = 70^\circ\text{C}$ 45 <sup>e</sup>	
		$T_A = 25^\circ\text{C}$ 15.8 <sup>b, c</sup>	
		$T_A = 70^\circ\text{C}$ 12 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	200	
Avalanche Current Pulse	$I_{AS}$	39	
Single Pulse Avalanche Energy	$E_{AS}$	94.8	mJ
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$ 90 <sup>a, e</sup>	A
		$T_A = 25^\circ\text{C}$ 3.13 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$ 100 <sup>a</sup>	W
		$T_C = 70^\circ\text{C}$ 75	
		$T_A = 25^\circ\text{C}$ 3.75 <sup>b, c</sup>	
		$T_A = 70^\circ\text{C}$ 2.63 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	32	40	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{thJC}$	0.5	0.6	

Notes:

a. Based on  $T_C = 25^\circ\text{C}$ .

b. Surface mounted on 1" x 1" FR4 board.

c.  $t = 10$  sec.d. Maximum under steady state conditions is  $90^\circ\text{C/W}$ .

e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		35		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 7.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	90			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 38.8 A		0.012		Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 37 A		0.014		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 38.8 A		160		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1801		pF
Output Capacitance	C <sub>oss</sub>			725		
Reverse Transfer Capacitance	C <sub>rss</sub>			570		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 38.8 A		85	120	nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 28.8 A		42	62	
Gate-Source Charge	Q <sub>gs</sub>			17		
Gate-Drain Charge	Q <sub>gd</sub>			14		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.625 Ω I <sub>D</sub> ≅ 24 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		10	20	ns
Rise Time	t <sub>r</sub>			11	17	
Turn-Off Delay Time	t <sub>d(off)</sub>			35	55	
Fall Time	t <sub>f</sub>			10	15	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.67 Ω I <sub>D</sub> ≅ 22.5 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		25	43	
Rise Time	t <sub>r</sub>			80	150	
Turn-Off Delay Time	t <sub>d(off)</sub>			26	42	
Fall Time	t <sub>f</sub>			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			120	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				120	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		52	78	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			70.2	105	nC
Reverse Recovery Fall Time	t <sub>a</sub>			27		ns
Reverse Recovery Rise Time	t <sub>b</sub>			25		

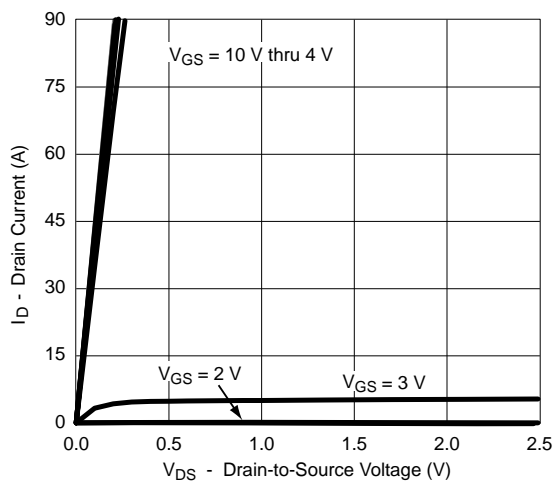
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

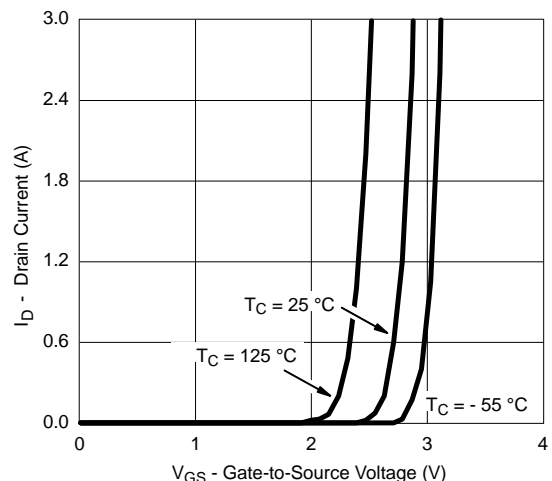
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

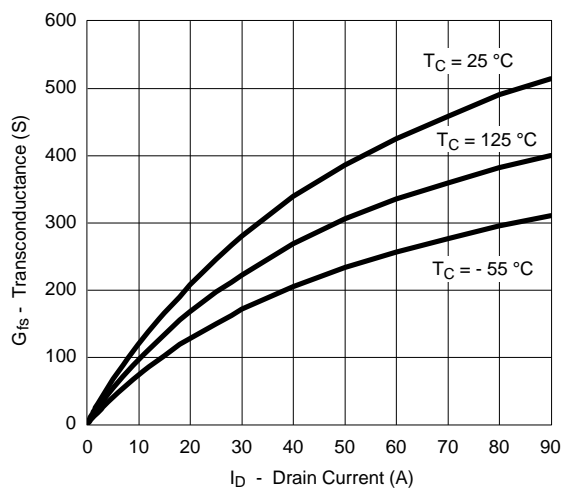
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



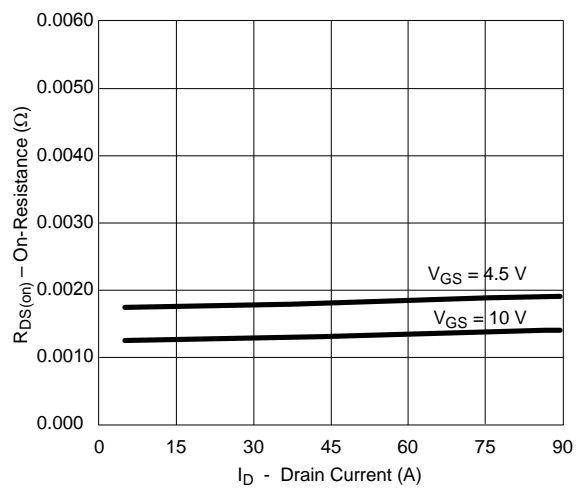
**Output Characteristics**



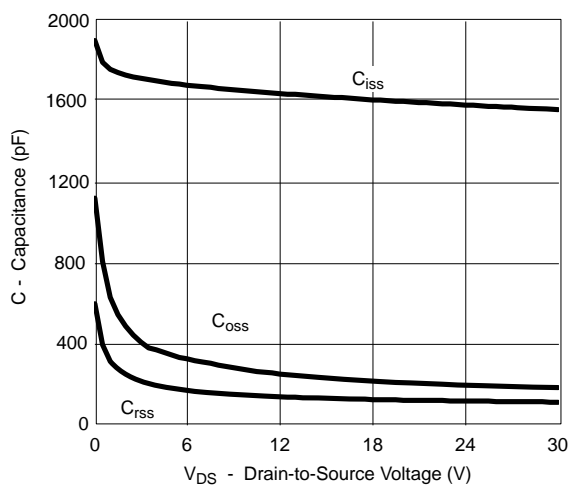
**Transfer Characteristics**



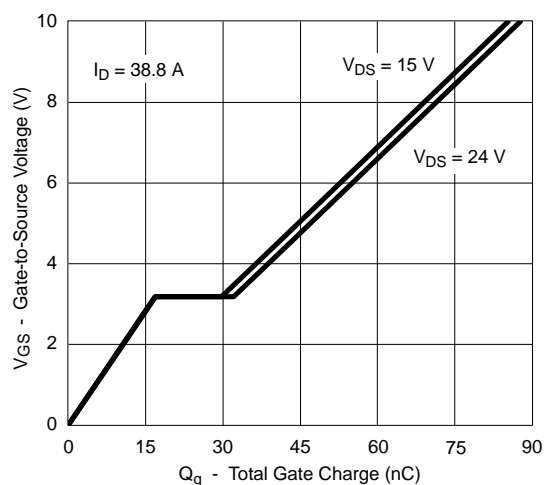
**Transconductance**



**$R_{DS(on)}$  vs. Drain Current**

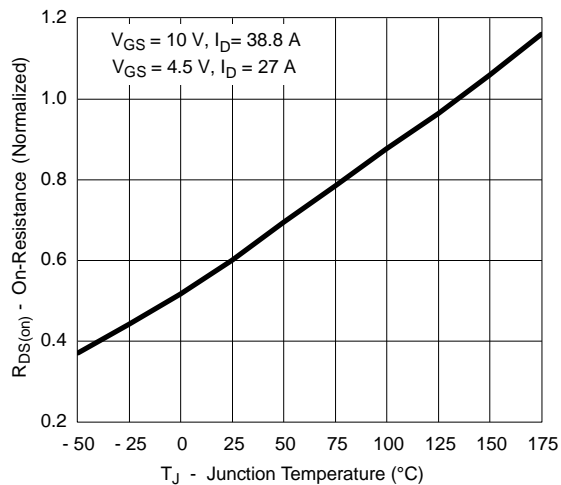


**Capacitance**

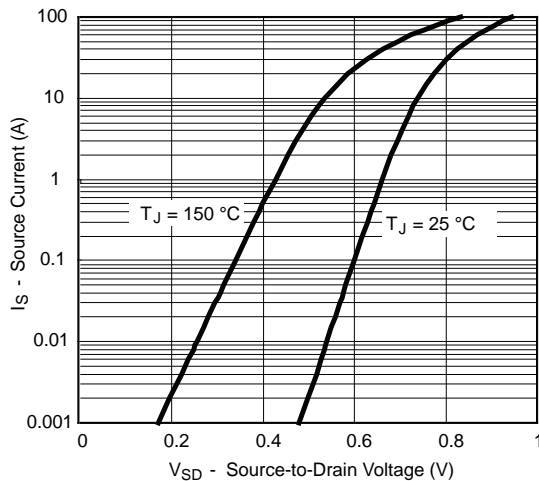


**Gate Charge**

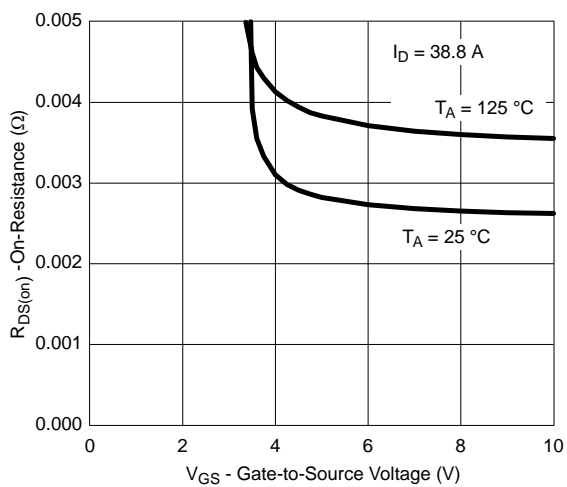
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**On-Resistance vs. Junction Temperature**



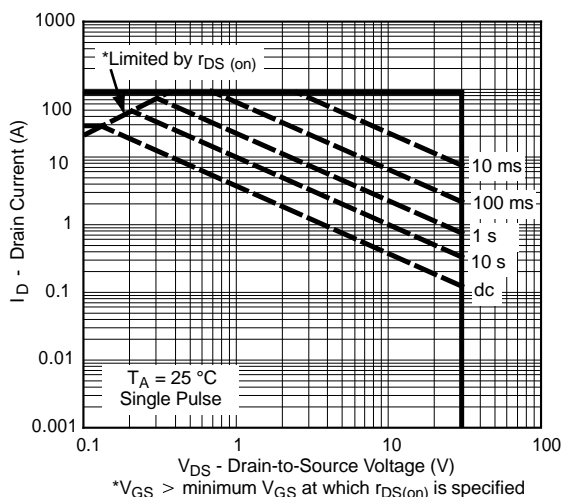
**Forward Diode Voltage vs. Temperature**



**$R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature**

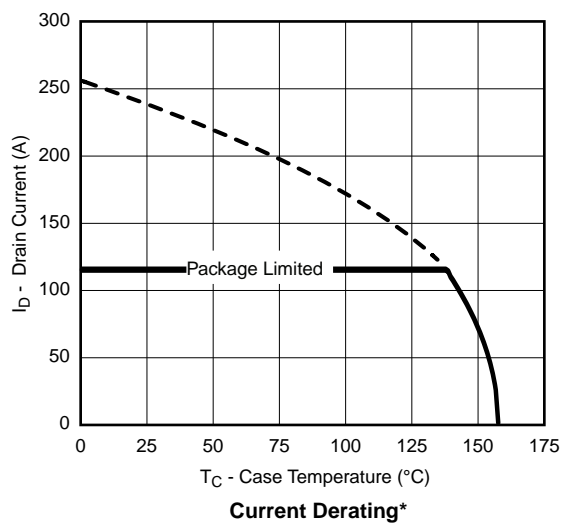


**Threshold Voltage**

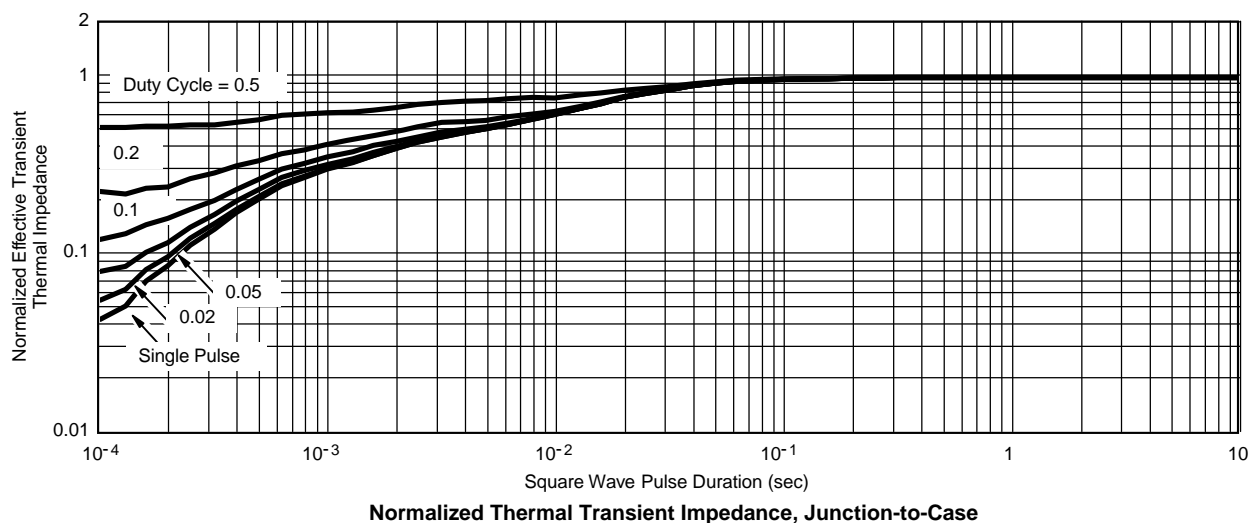


**Safe Operating Area, Junction-to-Ambient**

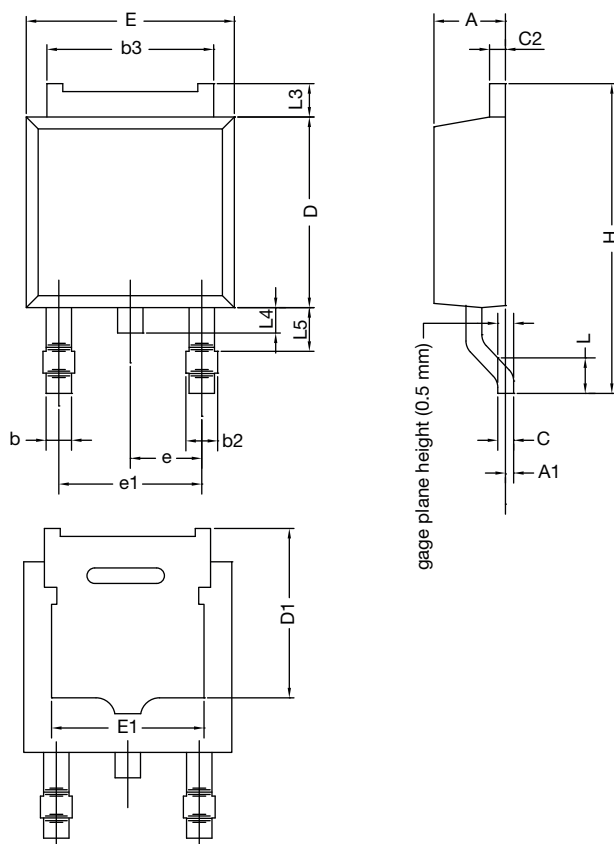
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 175\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



## TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

### Note

- Dimension L3 is for reference only.

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