

Description

GT68N12 use advanced technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in motor control applications.

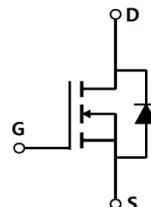
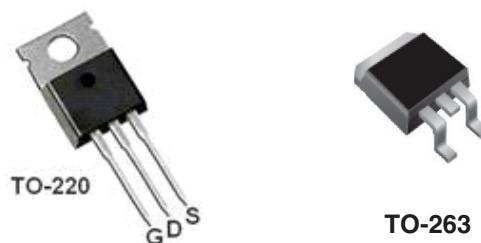
General Features

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- RoHS Compliant

Application

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

VDSS	RDS(ON) @10V (typ)	ID
120V	5 mΩ	110A

**Schematic diagram**

TO-220

TO-263

Ordering Information

Part Number	Marking	Case	Packaging
GT68N12M	GT68N12	TO-263	50pcs/Tube
GT68N12T	GT68N12	TO-220	50pcs/Tube

■ Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	120	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	110	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, \text{pulse}}$	330	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	192	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	400	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.65	°C/W
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	°C/W

■ Electrical Characteristics at $T_j=25$ °C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	120			V	$V_{GS}=0$ V, $I_D=250$ μA
Gate threshold voltage	$V_{GS(th)}$	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_D=250$ μA
Drain-source on-state resistance	$R_{DS(ON)}$		5.0	6.5	mΩ	$V_{GS}=10$ V, $I_D=30$ A
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20$ V
				-100		$V_{GS}=-20$ V
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=120$ V, $V_{GS}=0$ V

■ Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		5823.0		pF	$V_{GS}=0$ V, $V_{DS}=50$ V, $f=100$ kHz
Output capacitance	C_{oss}		778.8		pF	
Reverse transfer capacitance	C_{rss}		17.5		pF	
Turn-on delay time	$t_{d(on)}$		30.3		ns	$V_{GS}=10$ V, $V_{DS}=50$ V, $R_G=2$ Ω, $I_D=25$ A
Rise time	t_r		33.0		ns	
Turn-off delay time	$t_{d(off)}$		59.5		ns	
Fall time	t_f		11.7		ns	

■ Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		68.9		nC	$I_D=25$ A, $V_{DS}=50$ V, $V_{GS}=10$ V
Gate-source charge	Q_{gs}		18.1		nC	
Gate-drain charge	Q_{gd}		15.9		nC	
Gate plateau voltage	$V_{plateau}$		4.8		V	

■ Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward current	I _S			110	A	V _{GS} <V _{th}
Pulsed source current	I _{SP}			330		
Diode forward voltage	V _{SD}			1.3	V	I _S =30 A, V _{GS} =0 V
Reverse recovery time	t _{rr}		85.0		ns	I _S =25 A, di/dt=100 A/μs
Reverse recovery charge	Q _{rr}		240.0		nC	
Peak reverse recovery current	I _{rrm}		4.6		A	

■ Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5) V_{DD}=50 V, R_G=50 Ω, L=0.3 mH, starting T_j=25 °C.

■ Electrical Characteristics Diagrams

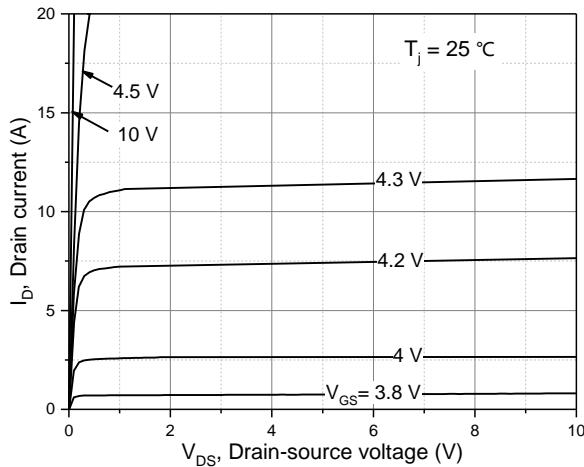


Figure 1, Typ. output characteristics

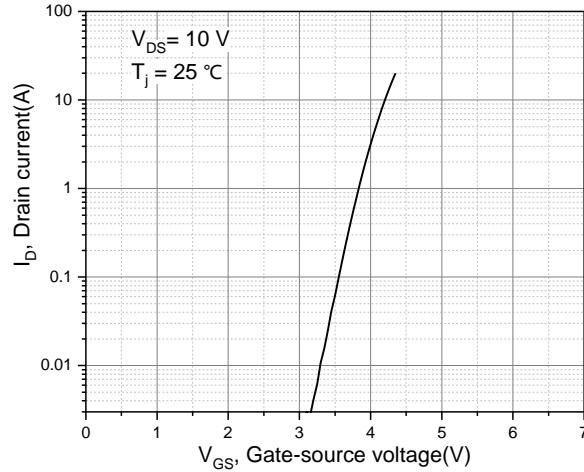


Figure 2, Typ. transfer characteristics

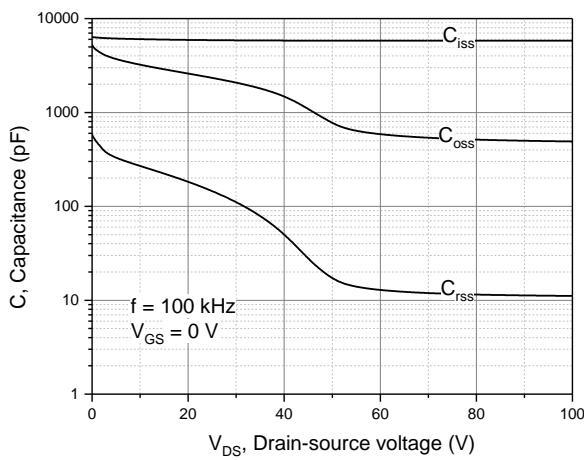


Figure 3, Typ. capacitances

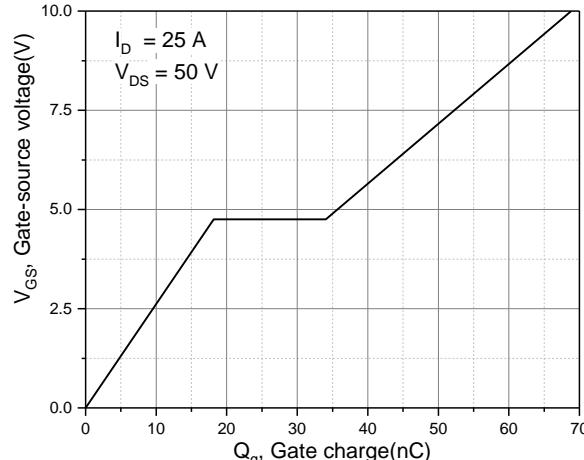


Figure 4, Typ. gate charge

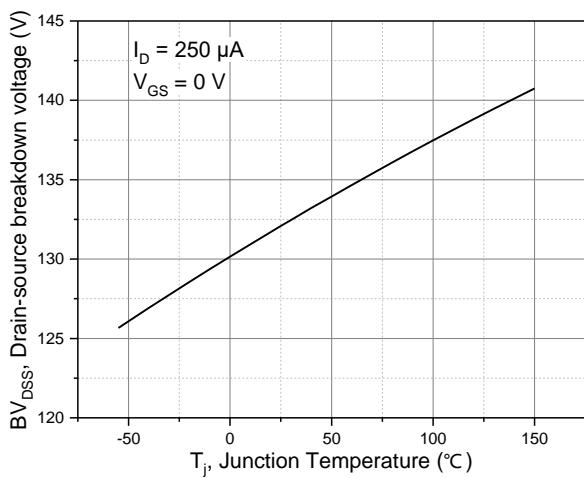


Figure 5, Drain-source breakdown voltage

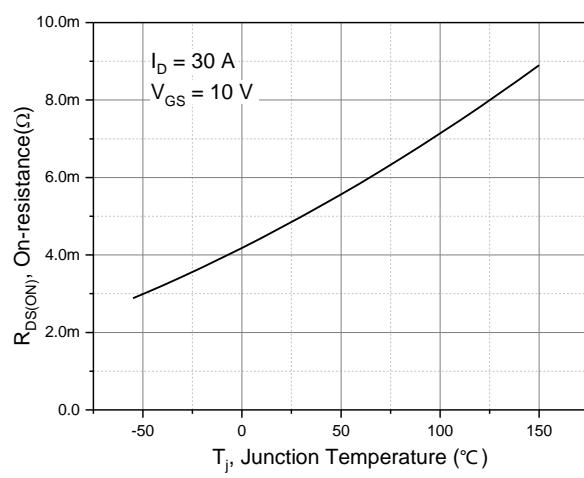


Figure 6, Drain-source on-state resistance

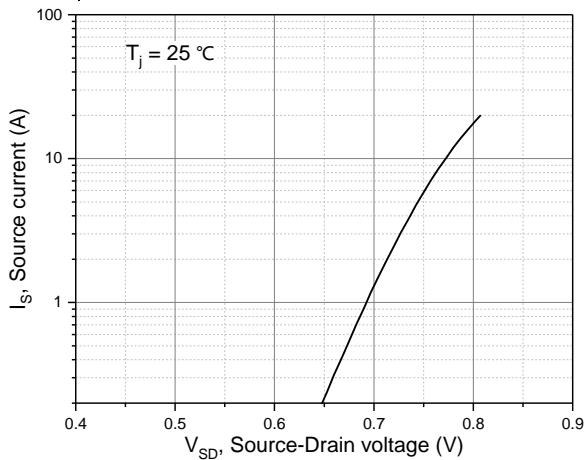


Figure 7, Forward characteristic of body diode

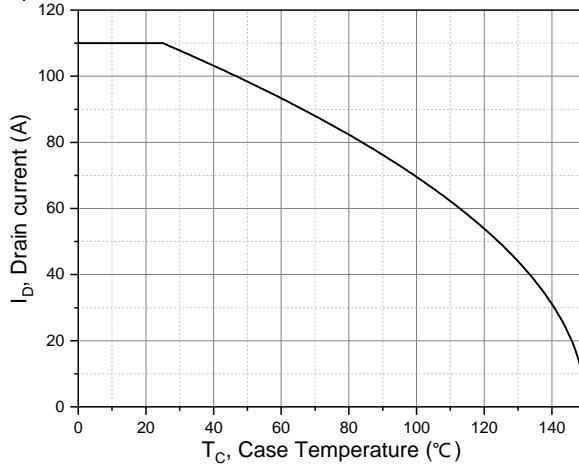
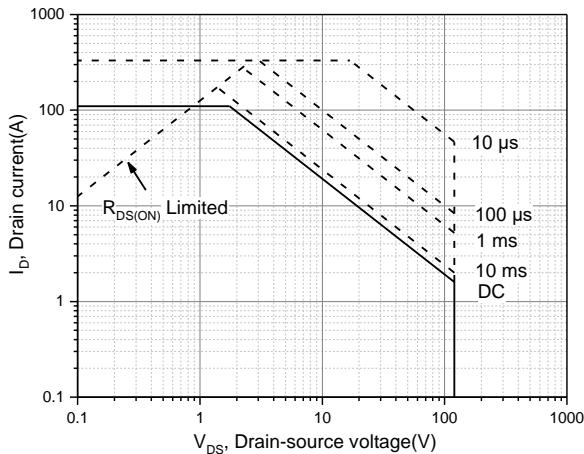


Figure 8, Drain current

Figure 9, Safe operation area $T_c=25 \text{ } ^\circ\text{C}$

■ Test circuits and waveforms

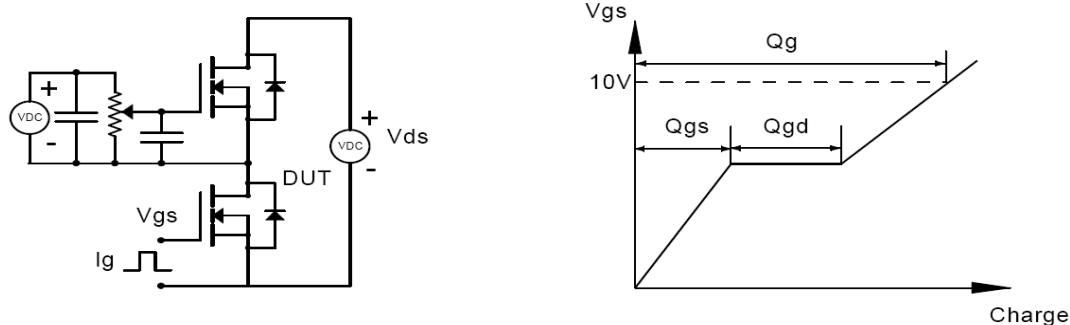


Figure 1, Gate charge test circuit & waveform

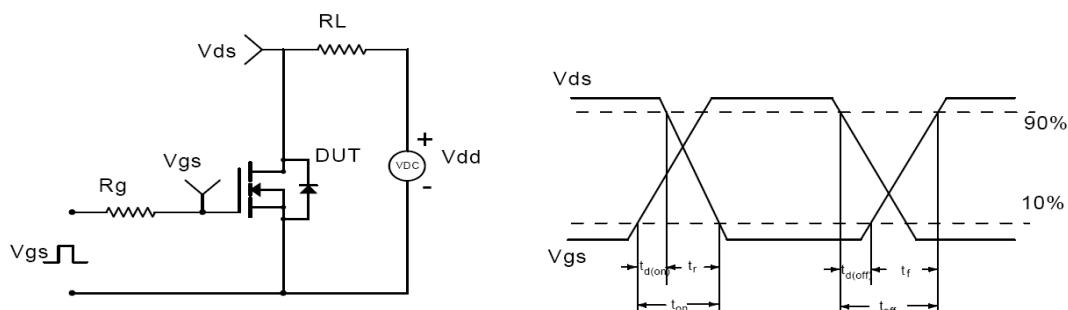


Figure 2, Switching time test circuit & waveforms

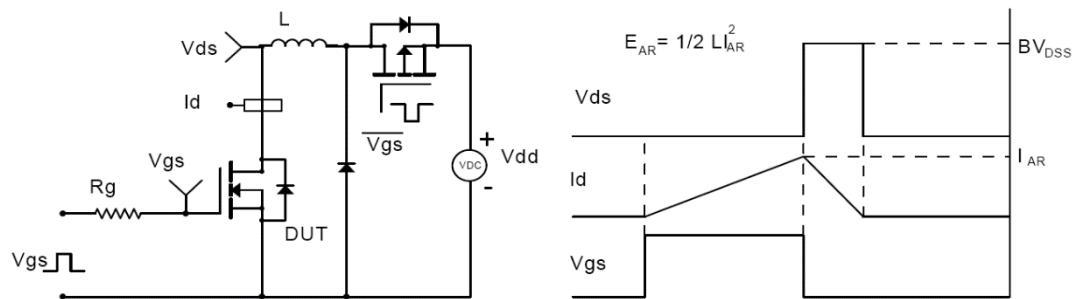


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

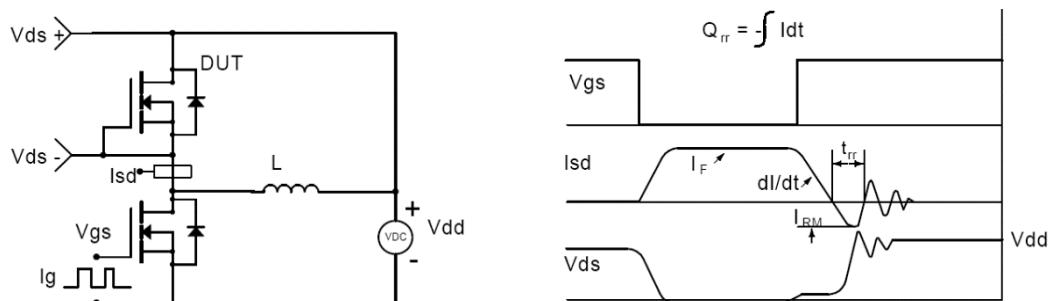
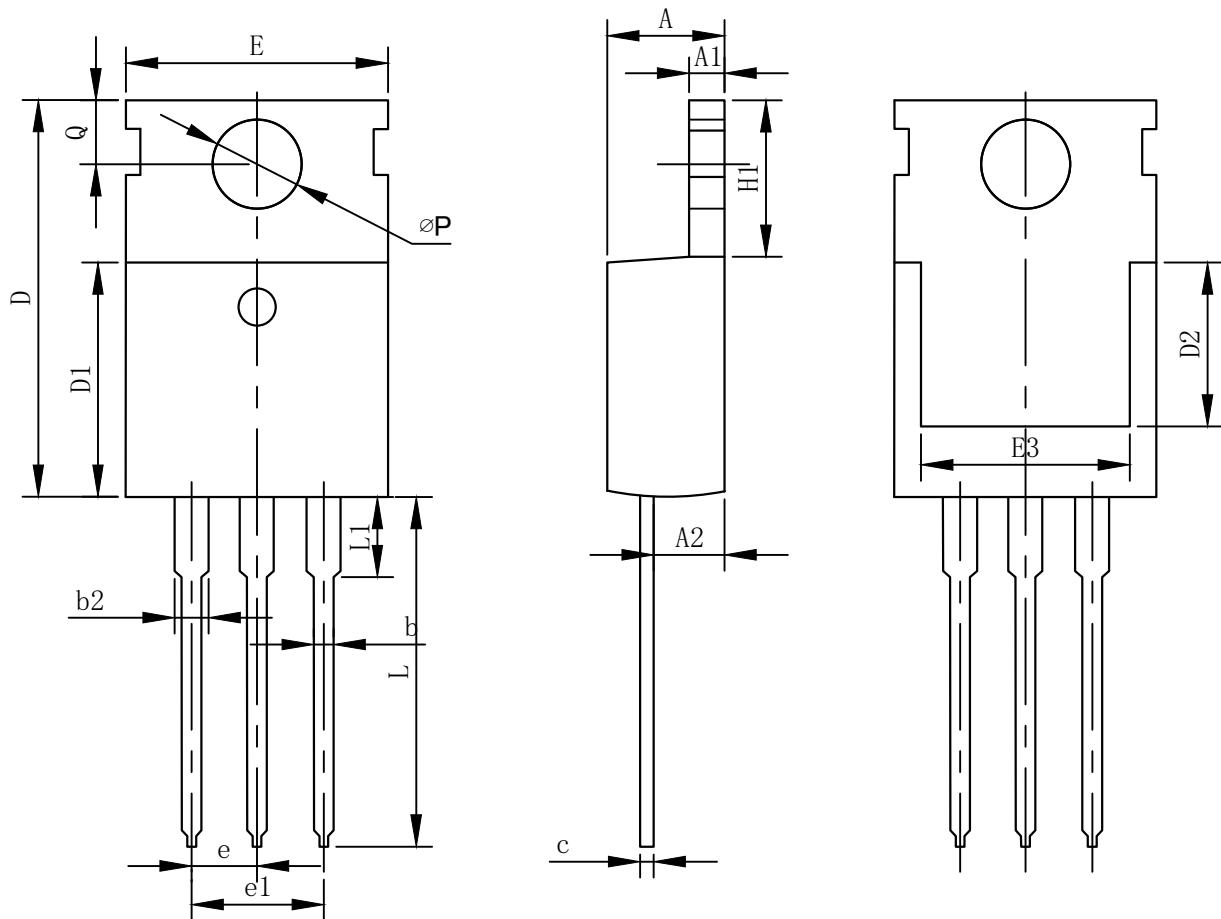


Figure 4, Diode reverse recovery test circuit & waveforms

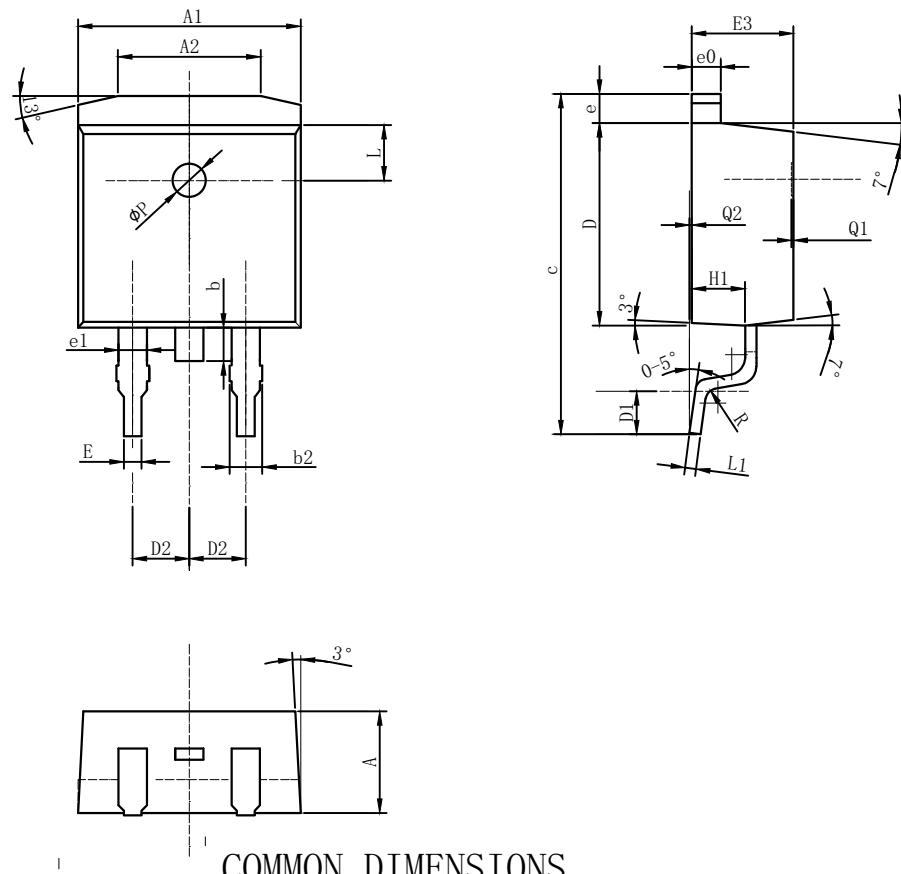
TO-220 Package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.70	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54BSC		
e1	5.08BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ØP	3.40	3.60	3.80
Q	2.60	2.80	3.00

TO-263 Package information



SYMBO	mm		
	MIN	NOM	MAX
A	4.52	4.57	4.62
A1	9.95	10.00	10.05
A2	6.30	6.40	6.50
b	1.30	1.50	1.70
b2	1.17	1.27	1.37
c	14.80	15.00	15.20
D	9.05	9.10	9.15
D1	1.90	2.10	2.30
D2	—	2.54	—
E	—	0.80	—
E3	—	4.57	—
e	—	1.30	—
e0	—	1.30	—
e1	1.73	3	—
H1	—	2.40	—
L	—	2.50	—
L1	—	0.50	—
ØP	—	1.50	—
R	—	0.50	—
Q1	0.10	—	0.15
Q2	0	—	0.02