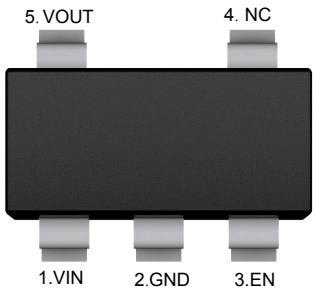
Description

The PJ9193 is designed for portable RF and wireless applications with demanding performance and space requirements. The PJ9193 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The PJ9193 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The PJ9193 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

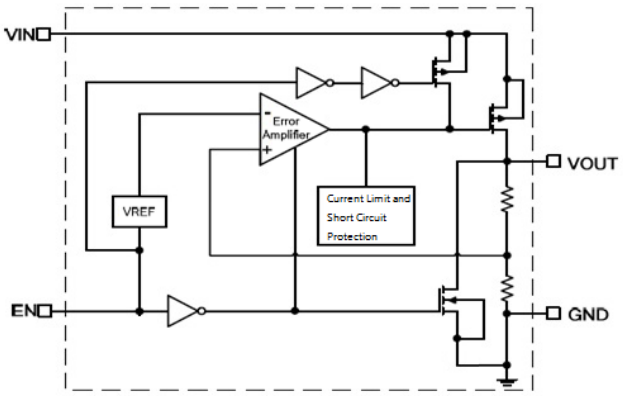
SOT-23-5



Features

- Ultra Low Noise for RF Application
- Ultra Fast Response in Line/Load Transient
- Maximum Output Current: 500mA
- Low Dropout : 200mV @ 200mA
- Wide Operating Voltage Ranges : 2V to 7V
- Low Temperature Coefficient
- Current Limiting Protection
- Thermal Shutdown Protection

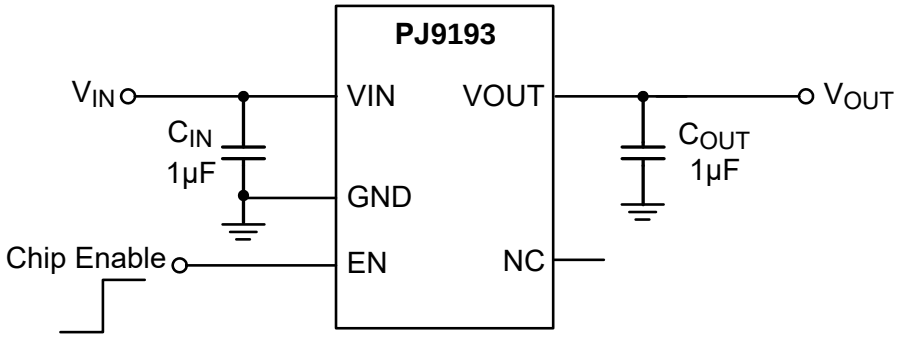
Function Block Diagram



Applications

- Battery-Powered Equipment
- CDMA/GSM Cellular Handsets
- Portable Information Appliances

Typical Application Circuit



Ordering Information

PJ9193- □□□□

Package Type
SE : SOT-23-5

Output Voltage
12 : 1.2V 15 : 1.5V 18 : 1.8V
25 : 2.5V 28 : 2.8V 30 : 3.0V
33 : 3.3V AD : Adjustable

Output current tap
M : 500mA

Functional Pin Description

Pin Name	Pin Function
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
GND	Ground.
VOUT	Output Voltage.
VIN	Power Input Voltage.

Absolute Maximum Ratings Note1

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter	Value	Unit
Supply Voltage	-0.3 ~ +6	V
Output Voltage	-0.3 ~ (VIN+0.3)	V
Output Current	600	mA
Power Dissipation	400	mW
Thermal Resistance,Junction-to-Ambient	250	℃/W
Thermal Resistance,Junction-to-Case	60	℃/W
Junction temperature	-40 ~ +125	℃
Storage temperature range	-55 ~ 150	℃

Note:

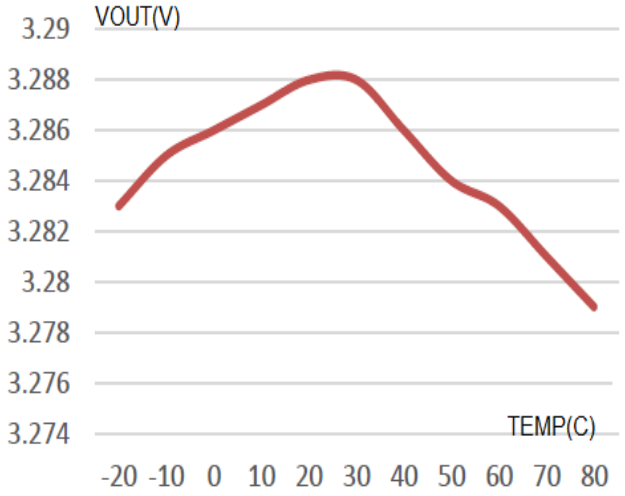
1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

Electrical Characteristics

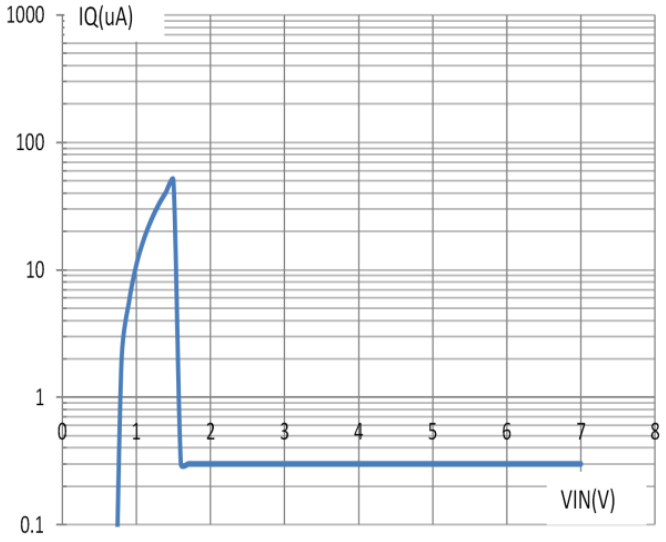
(V_{IN}=V_{OUT}+1, EN=V_{IN}, C_{IN}=C_{OUT}=1μF, T_A=25℃ , unless otherwise noted.)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage		V_{IN}		2		6	V
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT}=1mA	-1.5		+1.5	%
Quiescent Current		I_Q	V_{IN}>V_{OUT},EN=V_{IN} I_{OUT}=0mA		90	130	μA
Dropout Voltage		V_{DROP}	I_{OUT}=200mA		130	180	mV
			I_{OUT}=300mA		210	300	
Line Regulation		ΔV_{LINE}	V_{IN}=3.6V to 5.5V I_{OUT}=1mA			0.17	%/V
Load Regulation		ΔV_{LOAD}	1mA<I_{OUT}<300mA			2	%
Output Voltage Temperature Coefficient		TC_{VOUT}	I_{OUT}=30mA, T_A=0~70℃		±100		ppm/℃
Short circuit/start carrying current		I_{SHORT}	RL=1Ω		90		mA
EN Leakage Current		I_{EN}				0.1	μA
Standby Current		I_{STBY}	V_{EN}=GND,Shutdown		0.01	1	μA
Current Limit		I_{LIM}	VIN=5V		550		mA
EN Input Threshold	Logic Low	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic High	V_{IH}	V_{IN}=3V to 5.5V, Start up	1.2			V
Output Noise Voltage		e_{NO}	10Hz to100KHz, C_{OUT}=1uF		100		μV_{RMS}
Power Supply Rejection Ratio	f=217Hz	PSRR	Iout=100mA		-72		dB
	f=1KHz				-70		
	f=10KHz				-65		
Thermal Shutdown Temperature		T_{SD}	Shutdown, Temp increasing		160		℃
Thermal Shutdown Hysteresis		T_{SDHY}			20		℃

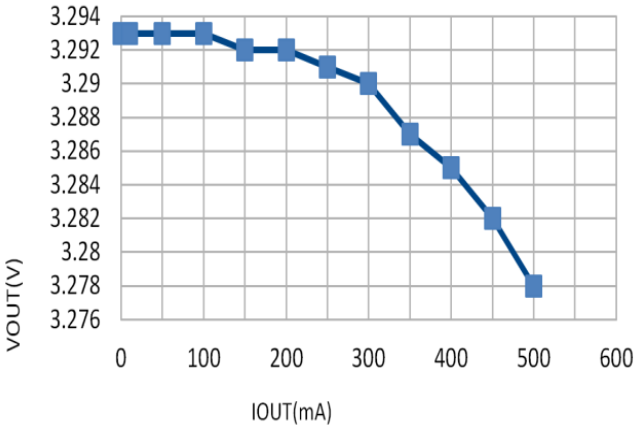
Typical Characteristic Curves



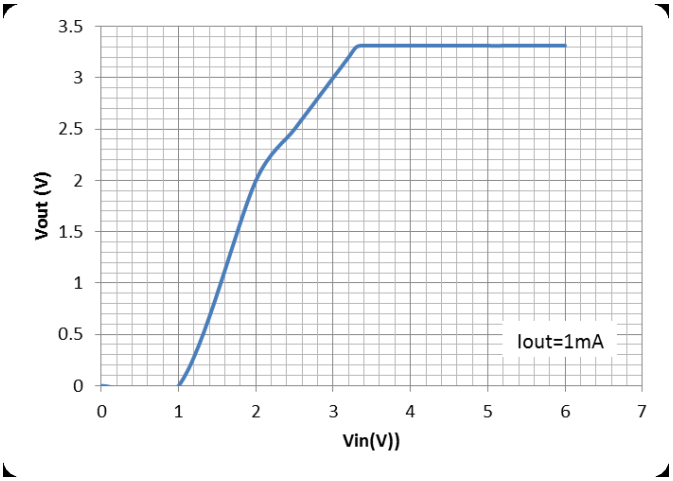
VOUT vs TEMP



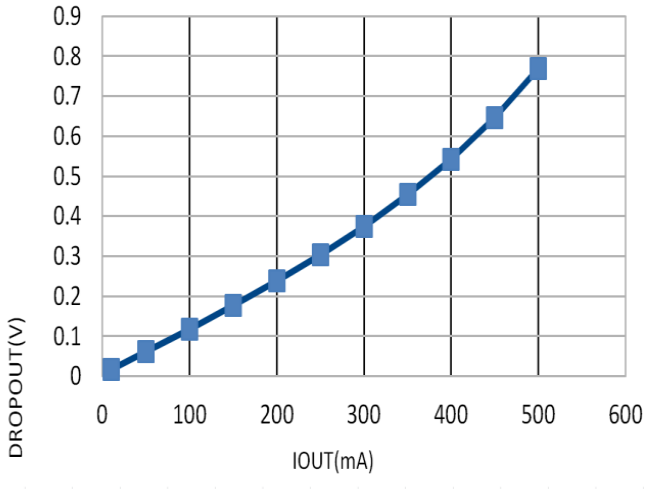
IQ vs VIN



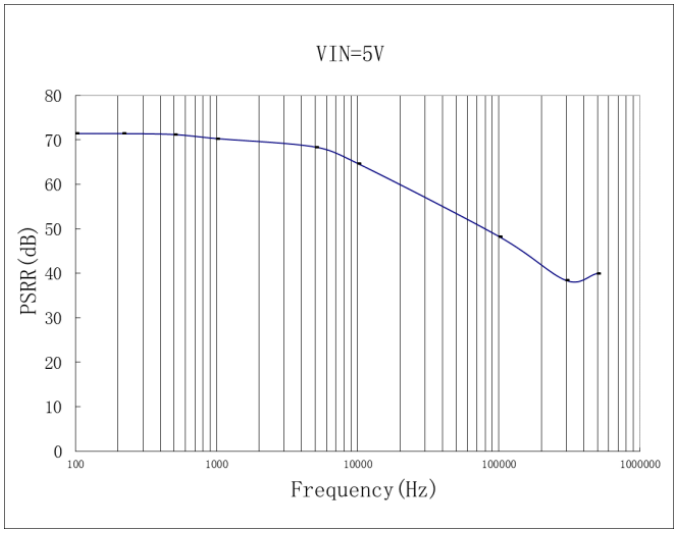
Load Regulation



Line Regulation



Dropout Voltage vs Load Current

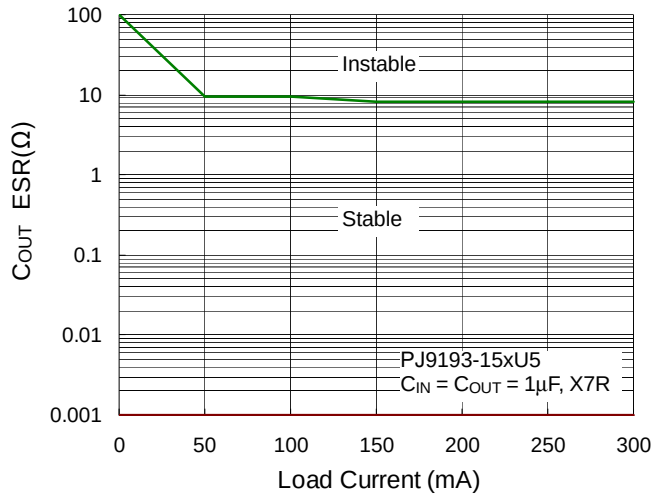


PSRR

Applications Information

Like any low dropout regulator, the external capacitors used with the PJ9193 must be carefully selected for regulator stability and performance. Using a capacitor whose value is >1μF on the PJ9193 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The PJ9193 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is >1mΩ on the PJ9193 output ensures stability. The PJ9193 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the the V_{OUT} pin of the PJ9193 and returned to a clean analog ground.

Figure 1Region of Stable C_{OUT} ESR vs. Load Current



Enable Function

The PJ9193 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the PJ9193 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in PJ9193. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

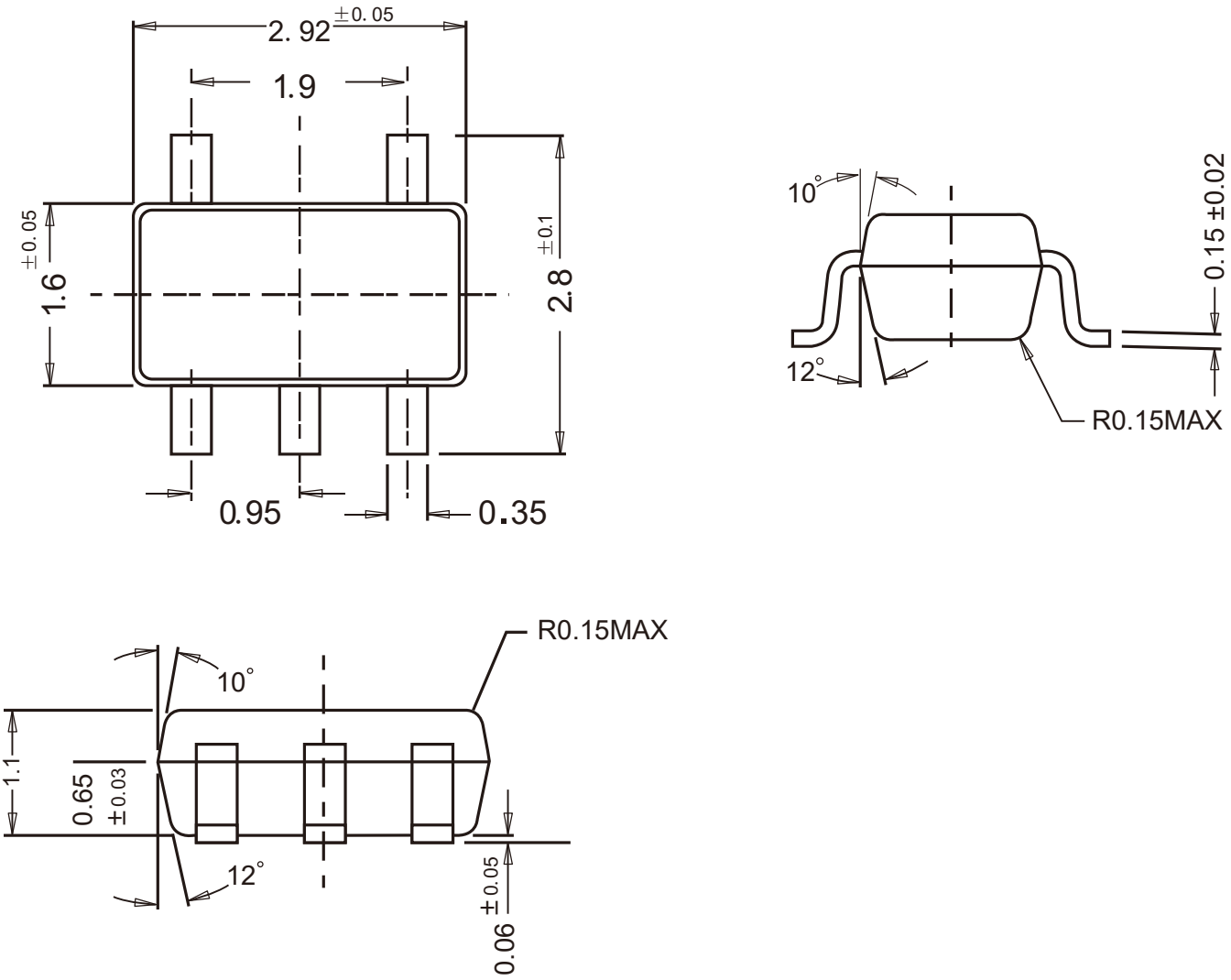
$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.

For recommended operating conditions specification of PJ9193, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance ($R_{\theta JA}$ is layout dependent) for SOT-23-5 package is 250°C/W, The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$$P_{D(MAX)} = (125°C - 25°C) / 250 = 400mW$$

Package Outline
SOT-23-5
Dimensions in mm



Ordering Information

Device	Package	Shipping
PJ9193	SOT-23-5	3,000/ Tape & Reel (7 inches)