N-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS}	200	V
$R_{DS(on)}$ V_{GS} = 10 V	48	mΩ
I_D	40	A
Configuration	Single	

FEATURES

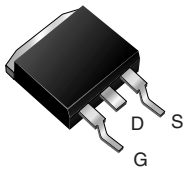
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- PWM Optimized for Fast Switching
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT

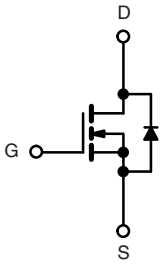
APPLICATIONS

- Isolated DC/DC Converters
  - Primary-Side Switch

D²PAK (TO-263)



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	40	A
	T_C = 125 °C		25	
Pulsed Drain Current		I_{DM}	80	
Avalanche Current		I_{AR}	20	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	16.2	mJ
Maximum Power Dissipation[a]	T_C = 25 °C	P_D	200[b]	W
	T_A = 25 °C[c]		4.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Limit**	**Unit**
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)		R_{thJC}	1	

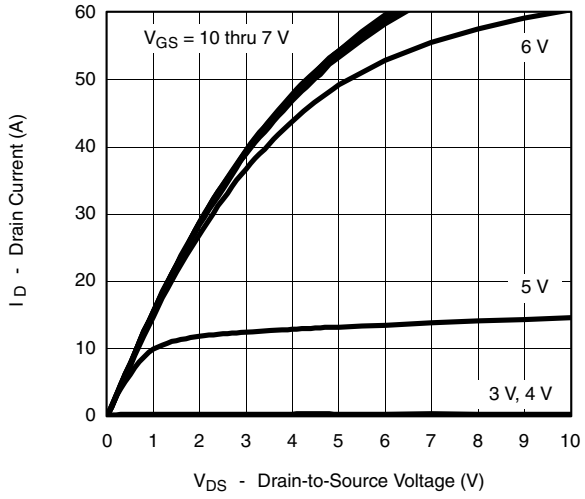
Notes:
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min .**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	200			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			1	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 175 °C			250	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 15 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		48		mΩ
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C		150		
		V_{GS} = 10 V, I_D = 20 A, T_J = 175 °C		180		
Drain-Source on State Resistance		V_{GS}= 6.5 V, I_D = 15 A		60		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	15			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3300		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge[c]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 20 A		35		nC
Gate-Source Charge[c]	Q_{gs}			11		
Gate-Drain Charge[c]	Q_{gd}			14		
Gate Resistance	R_G			2		Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 5 Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	25	ns
Rise Time[c]	t_r			35	55	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	60	
Fall Time[c]	t_f			30	45	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)[b]						
Continuous Current	I_S				40	A
Pulsed Current	I_{SM}				60	
Forward Voltage[a]	V_{SD}	I_F = 20 A, V_{GS} = 0 V		1	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, dI/dt = 100 A/µs		115	170	ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			7.5	12	A
Reverse Recovery Charge	Q_{rr}			0.43	1.02	µC

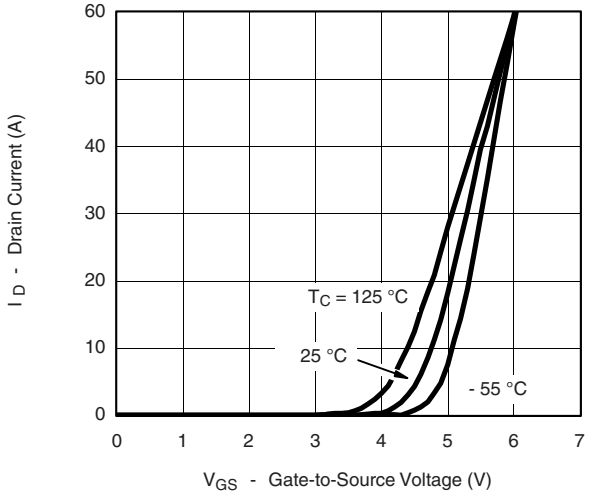
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

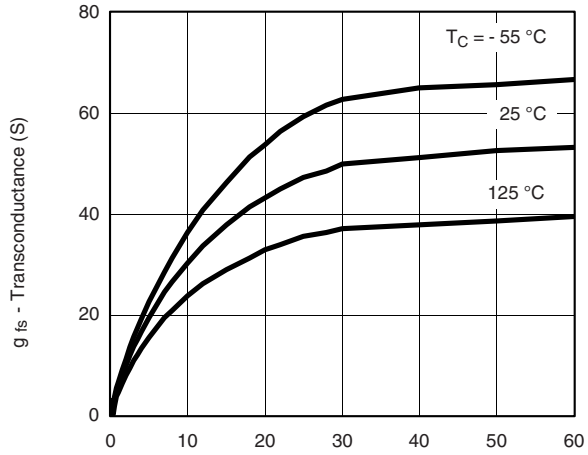
TYPICAL CHARACTERISTICS (25 °C unless noted)



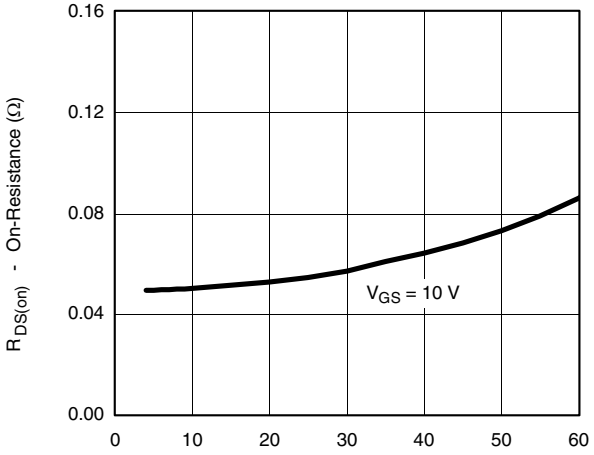
Output Characteristics



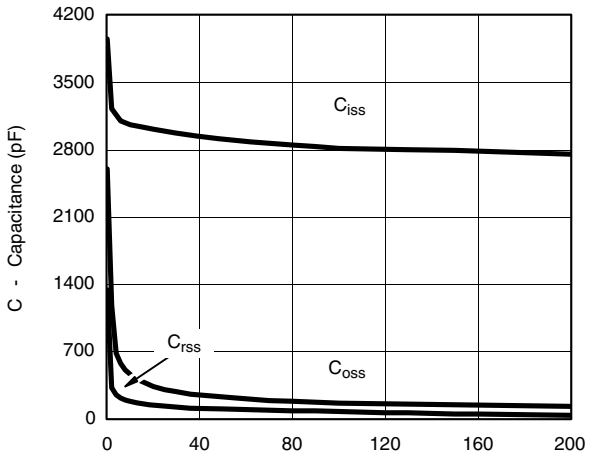
Transfer Characteristics



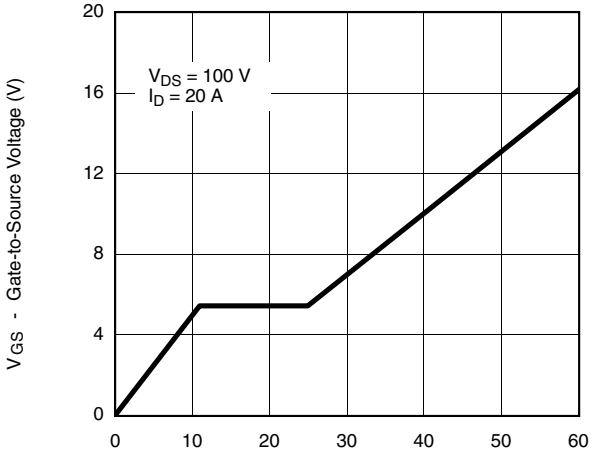
Transconductance



On-Resistance vs. Drain Current

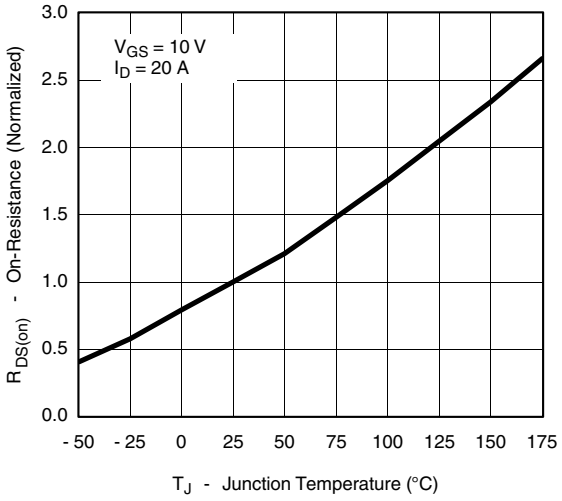


Capacitance

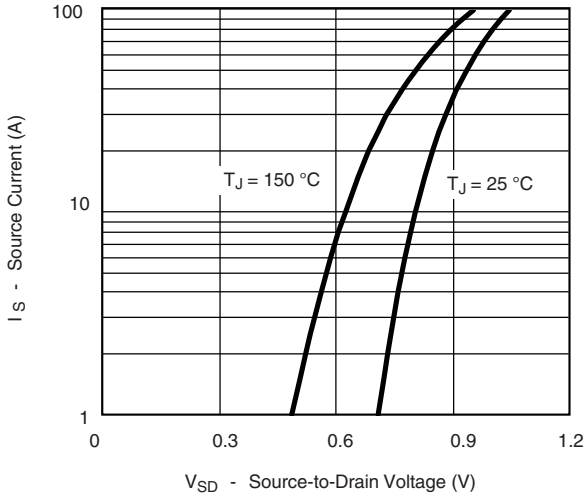


Gate Charge

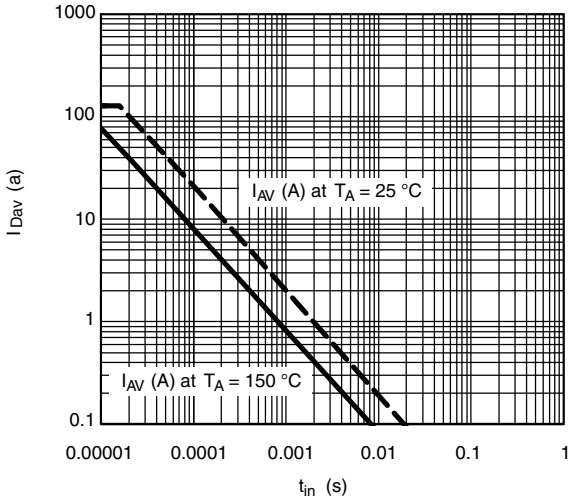
TYPICAL CHARACTERISTICS (25 °C unless noted)



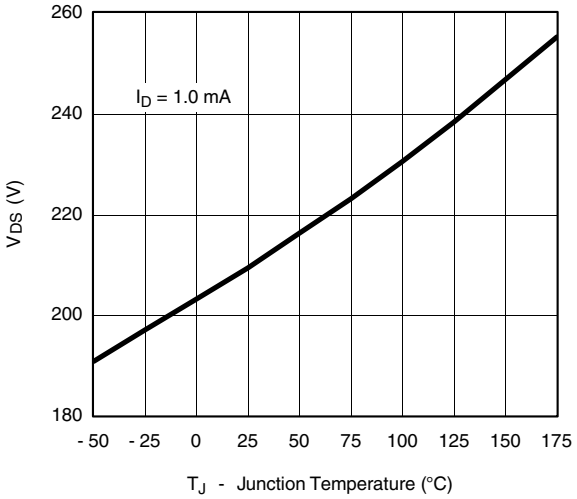
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

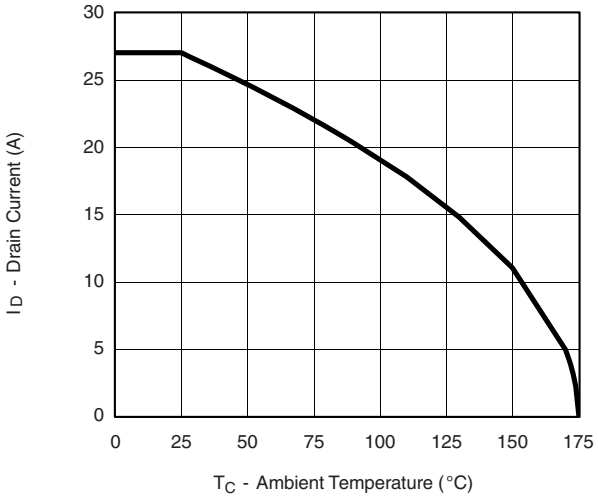


Avalanche Current vs. Time

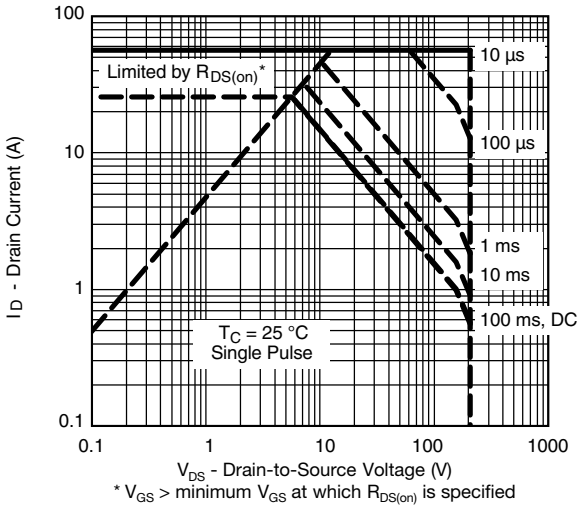


Drain Source Breakdown vs. Junction Temperature

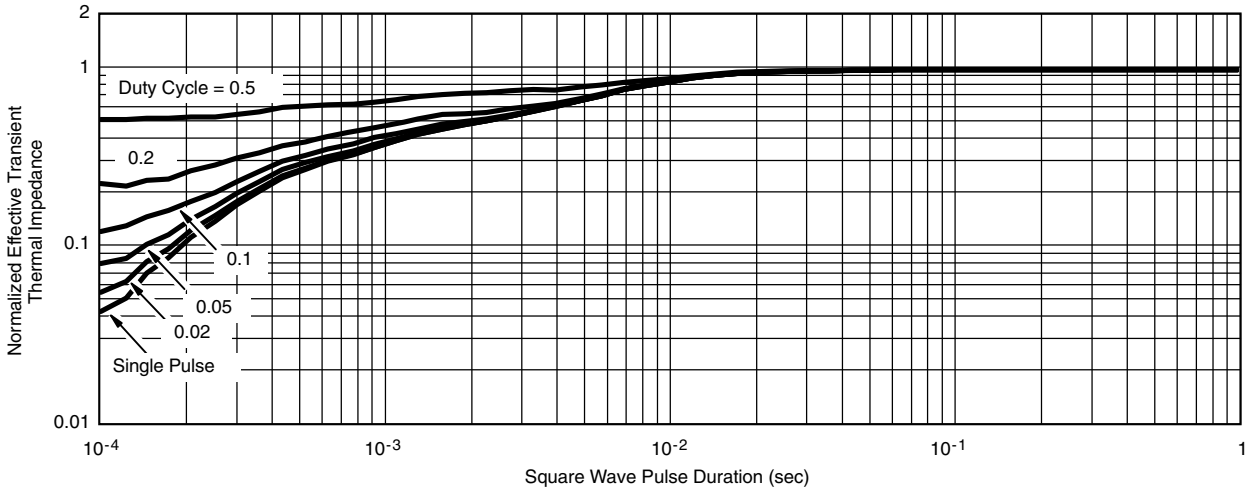
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

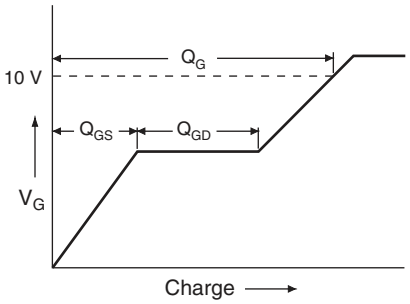


Fig. 13a - Basic Gate Charge Waveform

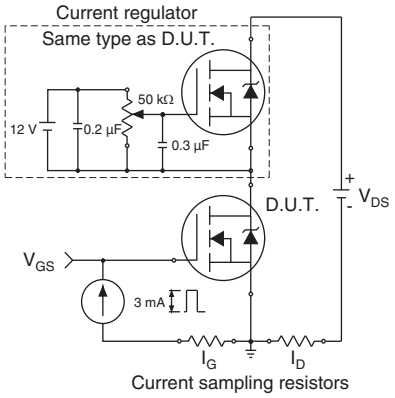
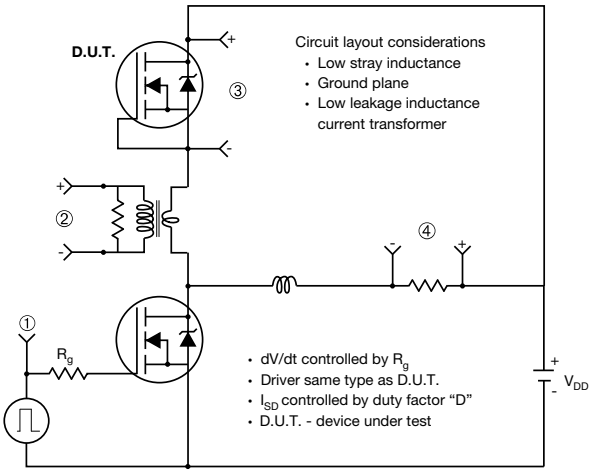
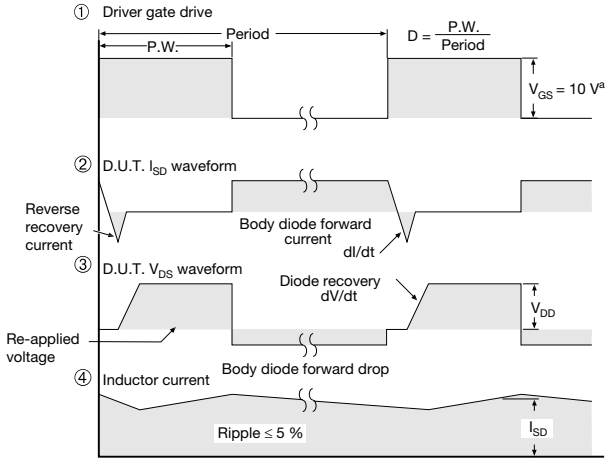


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



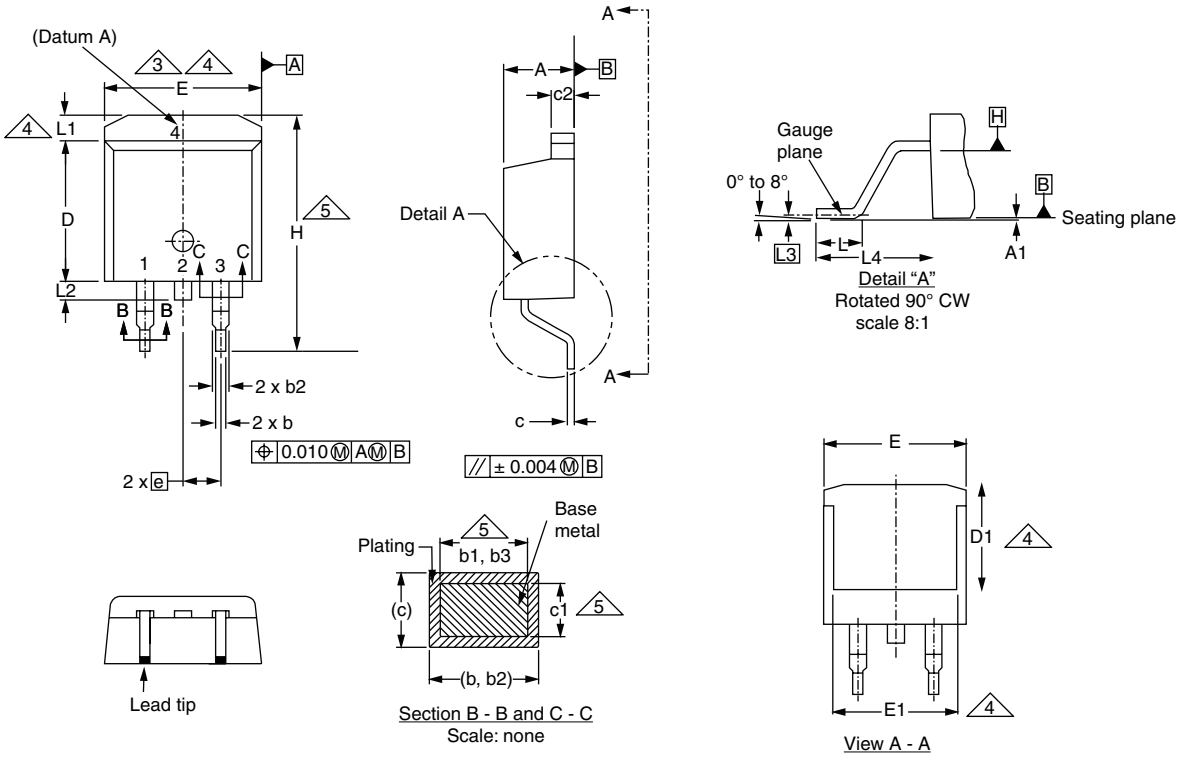


Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

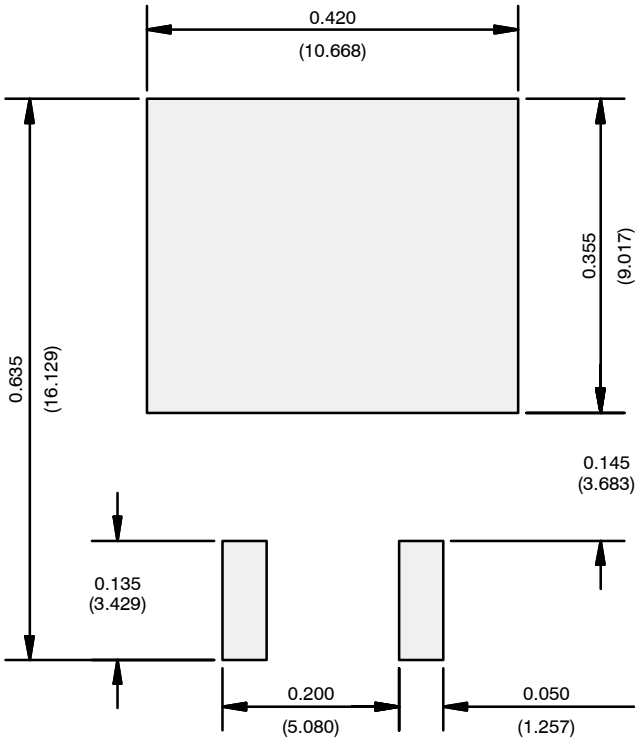
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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