

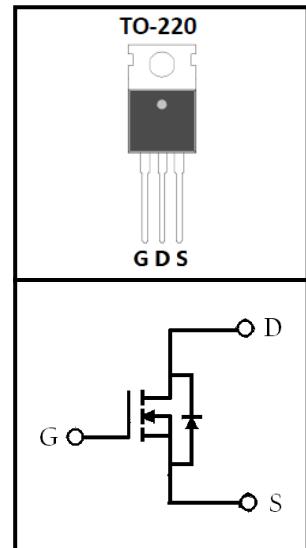
30V N-Channel Trench MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Hard switched and high frequency circuits



Device Marking and Package Information

Device	Package	Marking
CTP03N2P7	TO-220	CTP03N2P7

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	30	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	230	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		150	A
Pulsed Drain Current	I_{DM}	500	A
Gate Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy	E_{AS}	246	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	187	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+175	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.8	°C/W
Thermal Resistance, Junction-to-Ambient (note1)	$R_{\theta JA}$	62	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 55^\circ\text{C}$	--	--	5	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.0	--	2.5	V
Drain-Source On-Resistance (note2)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$	--	2.0	2.7	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 15\text{A}$	--	2.6	3.8	$\text{m}\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1.0\text{MHz}$	--	5850	--	pF
Output Capacitance	C_{oss}		--	720	--	
Reverse Transfer Capacitance	C_{rss}		--	525	--	
Total Gate Charge (4.5V)	Q_g	$V_{\text{DS}} = 15\text{V}, I_D = 15\text{A}, V_{\text{GS}} = 4.5\text{V}$	--	56.9	--	nC
Gate-Source Charge	Q_{gs}		--	13.8	--	
Gate-Drain Charge	Q_{gd}		--	23.5	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = 15\text{V}, I_D = 1\text{A}, V_{\text{GS}} = 10\text{V}, R_G = 3\Omega$	--	20.1	--	ns
Turn-on Rise Time	t_r		--	6.3	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	124.6	--	
Turn-off Fall Time	t_f		--	15.8	--	
Body Diode Characteristics						
Source-Drain Current(Body Diode)	I_{SD}		--	--	230	A
Pulsed Source-Drain Current(Body Diode)	I_{SDM}		--	--	500	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 1\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}} = 25\text{V}, V_{\text{GS}} = 10\text{V}, L = 0.1\text{mH}$
4. The power dissipation is limited by 175°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

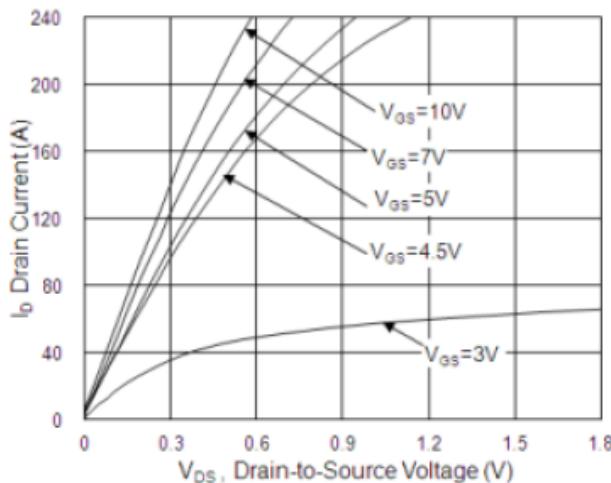


Fig.1 Typical Output Characteristics

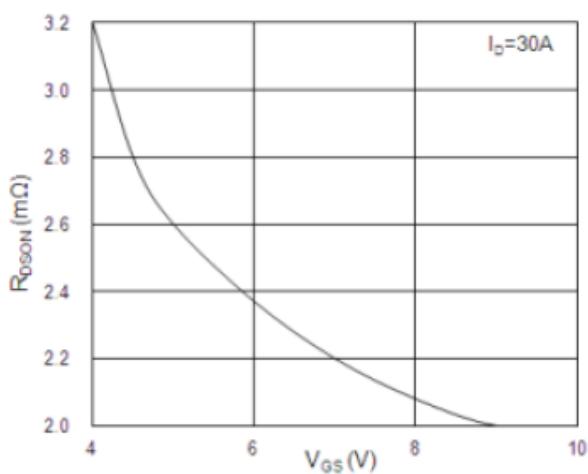


Fig.2 On-Resistance vs. G-S Voltage

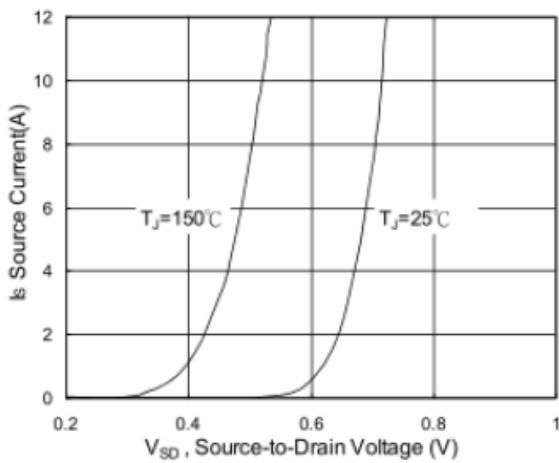


Fig.3 Forward Characteristics of Reverse Diode

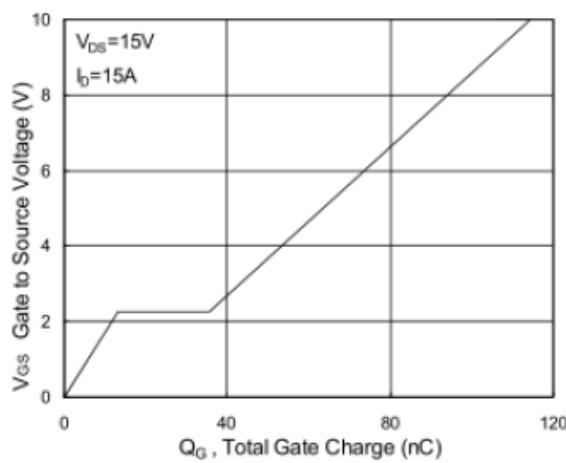


Fig.4 Gate-Charge Characteristics

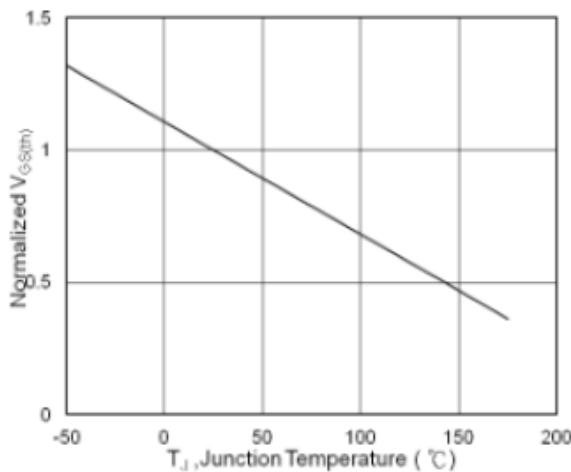


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

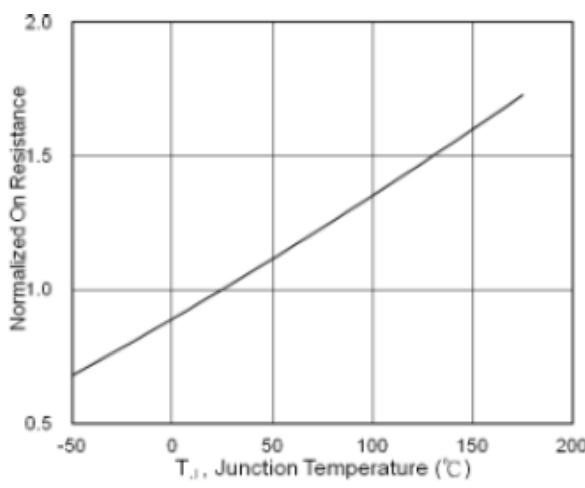


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

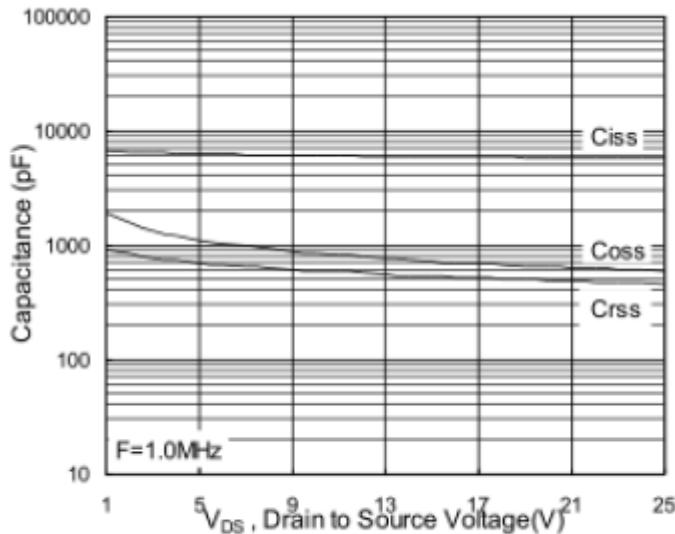


Fig.7 Capacitance

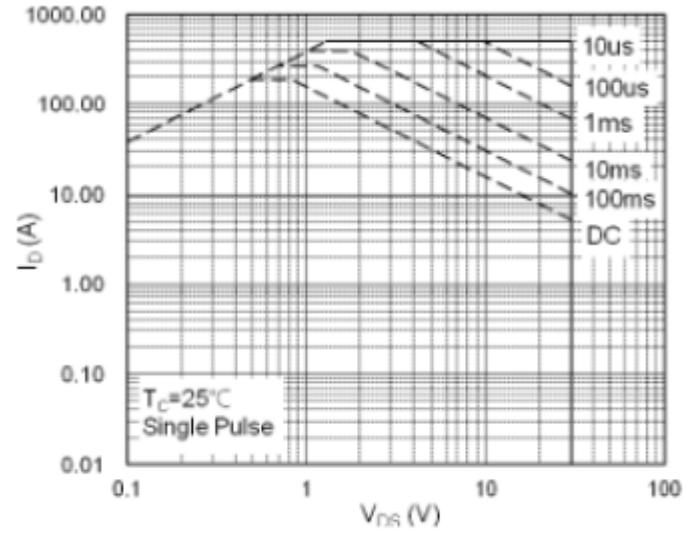


Fig.8 Safe Operating Area

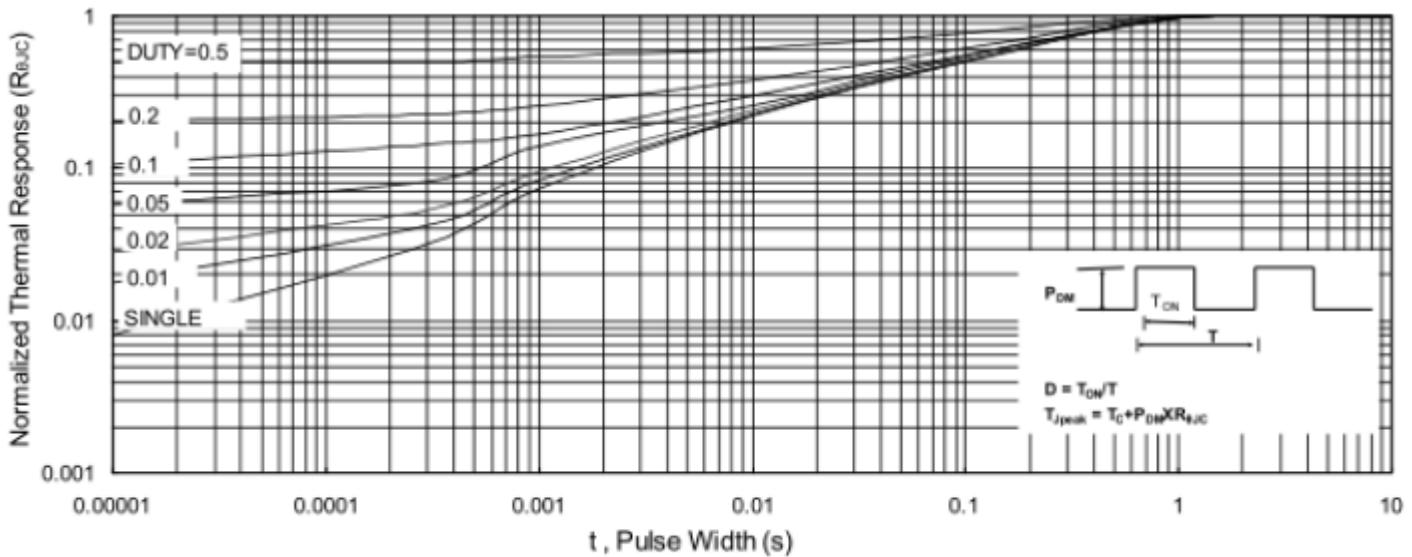
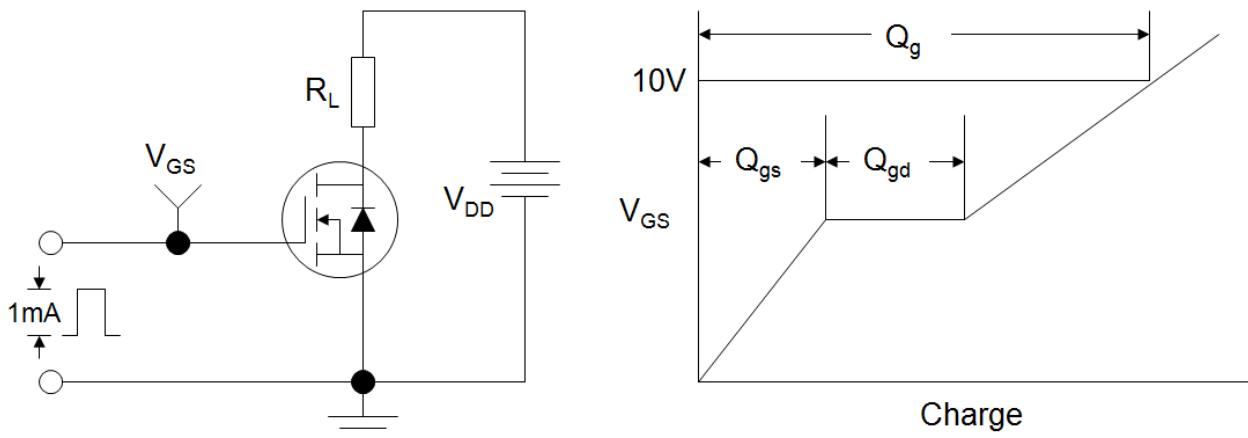
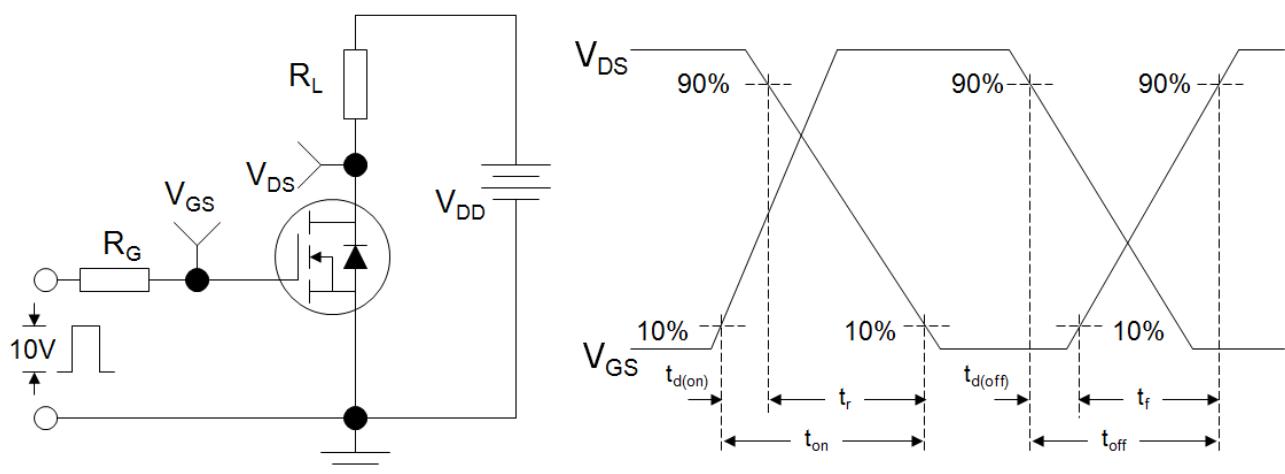
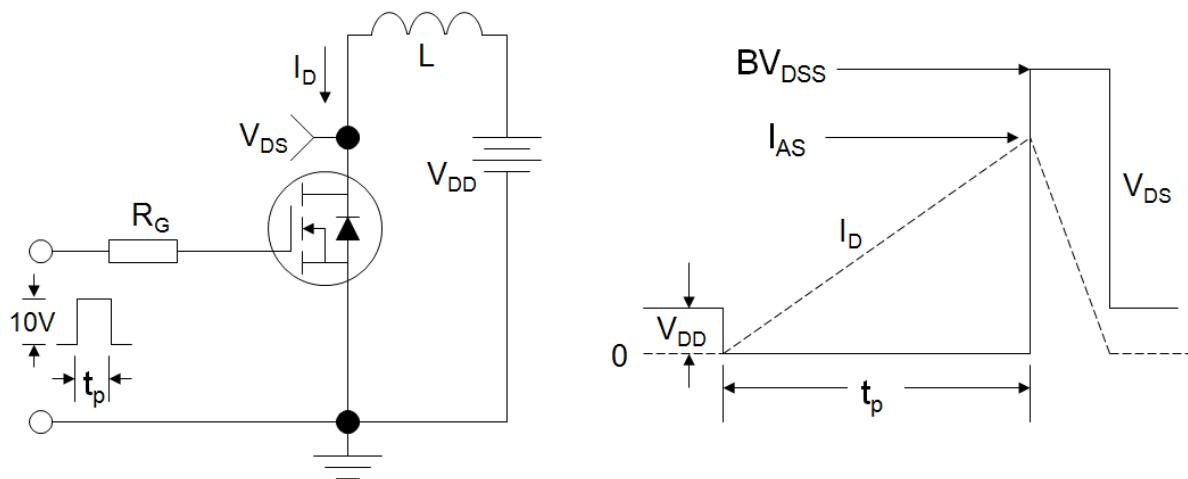
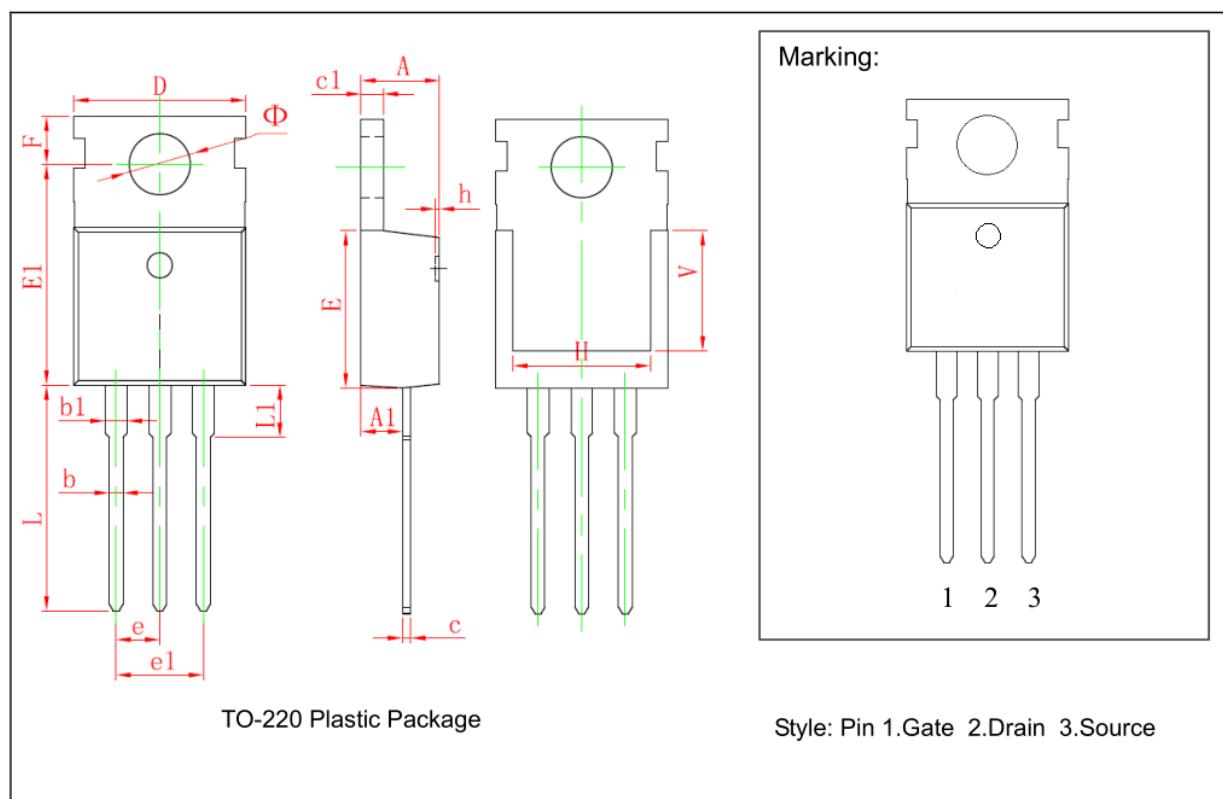


Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


TO-220 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		e	2.540*	0.100*	
A	4.400	4.600	0.173	0.181	e1	4.980	5.180	0.196	0.204
A1	2.250	2.550	0.089	0.100	F	2.650	2.950	0.104	0.116
b	0.710	0.910	0.028	0.036	H	7.900	8.100	0.311	0.319
b1	1.170	1.370	0.046	0.054	h	0.000	0.300	0.000	0.012
c	0.330	0.650	0.013	0.026	L	12.900	13.400	0.508	0.528
c1	1.200	1.400	0.047	0.055	L1	2.850	3.250	0.112	0.128
D	9.910	10.250	0.390	0.404	V	7.500	REF	0.295	REF
E	8.950	9.750	0.352	0.384	Φ	3.600	3.800	0.142	0.150
E1	12.650	12.950	0.498	0.510					

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