

Description

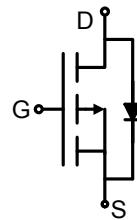
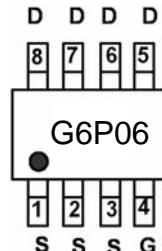
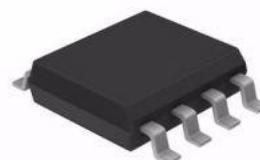
The G6P06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- | | | | |
|-----------|-----------------------------|-----------------------------|-------|
| V_{DSS} | $R_{DS(ON)}$
@-10V (Typ) | $R_{DS(ON)}$
@-4.5V(Typ) | I_D |
| -60V | 80m Ω | 100m Ω | -4A |
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density celldesign for ultra low on-resistance
- RoHS Compliant

Application

- Power switch
- DC/DC converters

**Schematic diagram****Marking and pin Assignment****SOP-8****Ordering Information**

Part Number	Marking	Case	Packaging
G6P06	G6P06	SOP-8	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-60	V
Continuous Drain Current	I_D	-4	A
Pulsed Drain Current (note1)	I_{DM}	-16	A
Gate-Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note2)	E_{AS}	36	mJ
Avalanche Current	I_{As}	12	A
Power Dissipation ($T_C = 25^\circ\text{C}$) (note3)	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	40	°C/W

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -60\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	--	--	-1	μA
		$V_{\text{DS}} = -60\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 150^\circ\text{C}$	--	--	-100	
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.0	-1.8	-3.0	V
Drain-Source On-Resistance (Note3)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -4\text{A}$	--	80	96	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -3\text{A}$	--	100	145	$\text{m}\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -30\text{V}, f = 1.0\text{MHz}$	--	976	--	pF
Output Capacitance	C_{oss}		--	70	--	
Reverse Transfer Capacitance	C_{rss}		--	30	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = -30\text{V}, I_D = -4\text{A}, V_{\text{GS}} = -10\text{V}$	--	24	--	nC
Gate-Source Charge	Q_{gs}		--	2.2	--	
Gate-Drain Charge	Q_{gd}		--	3.6	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -30\text{V}, I_D = -4\text{A}, R_G = 2.5\Omega$	--	10	--	ns
Turn-on Rise Time	t_r		--	5	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	35	--	
Turn-off Fall Time	t_f		--	9	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-4	A
Pulsed Diode Forward Current	I_{SM}		--	--	-16	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = -4\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = -4\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	--	36	--	ns
Reverse Recovery Charge	Q_{rr}		--	38	--	nC

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. VDD = -50V, RG = 25Ω, Starting TJ = 25°C, L=0.5mH
3. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

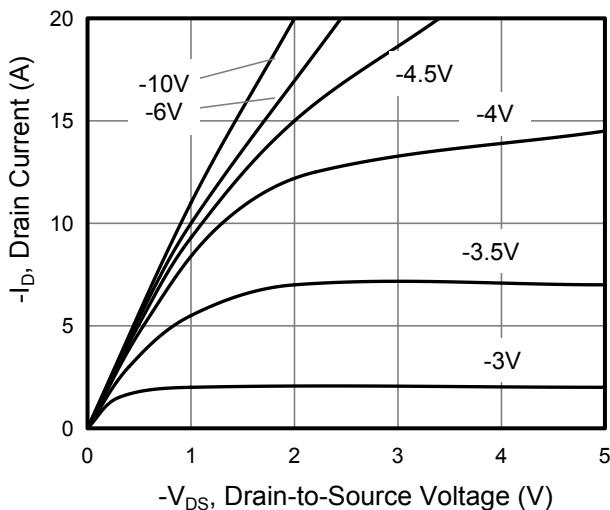


Figure 2. Transfer Characteristics

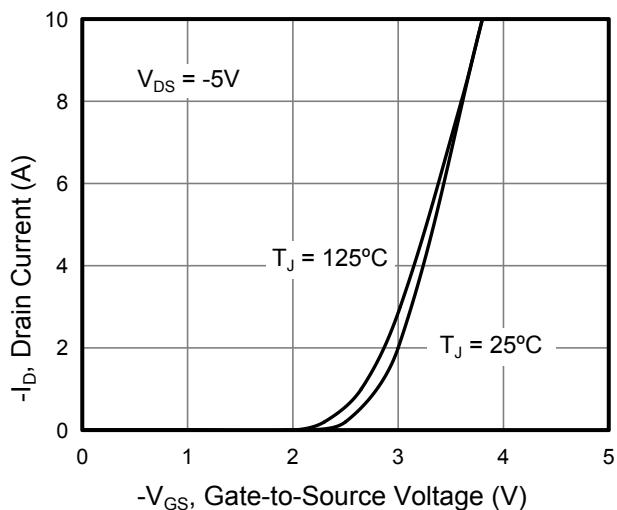


Figure 3. On-Resistance vs. Drain Current

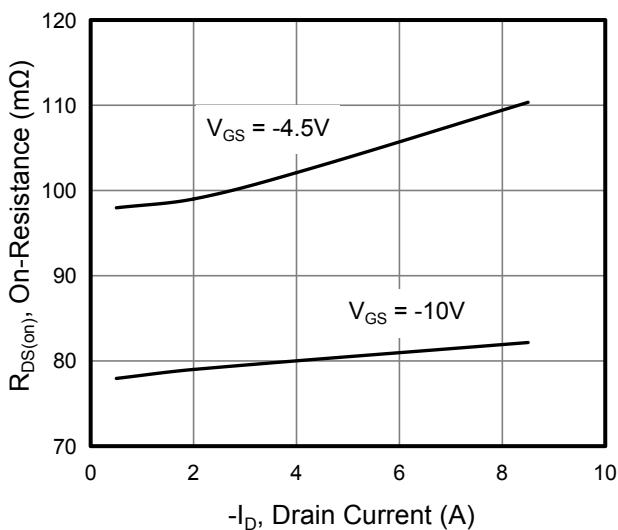


Figure 4. On-Resistance vs. Junction Temperature

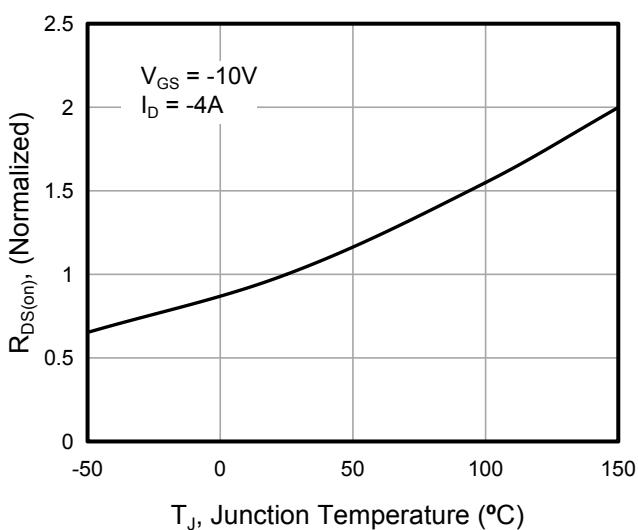


Figure 5. Threshold Voltage vs. Junction Temperature

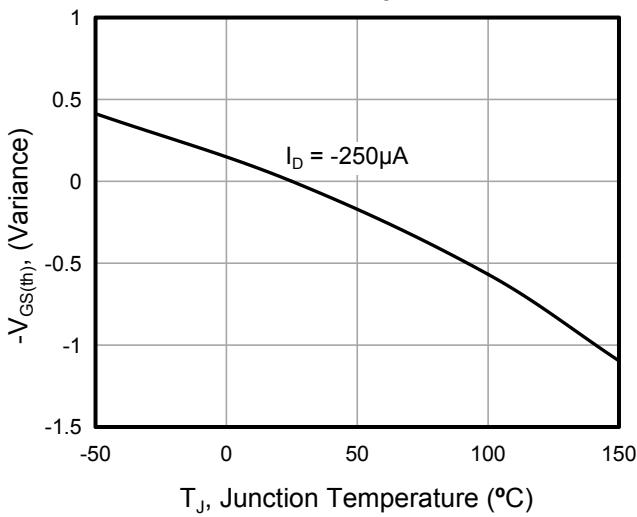
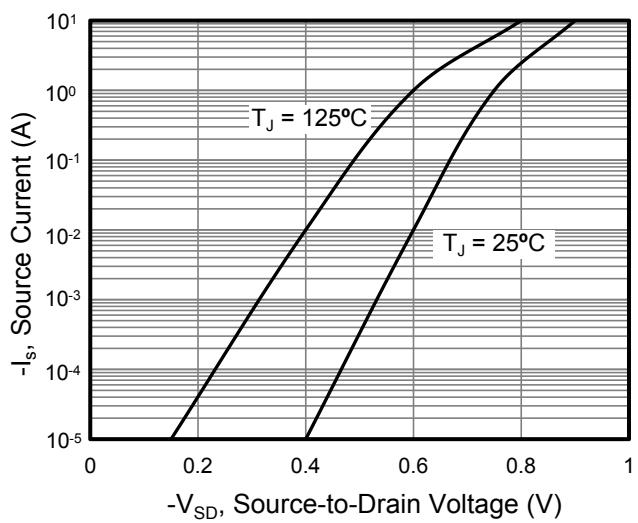


Figure 6. Body Diode Forward Voltage



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Capacitance

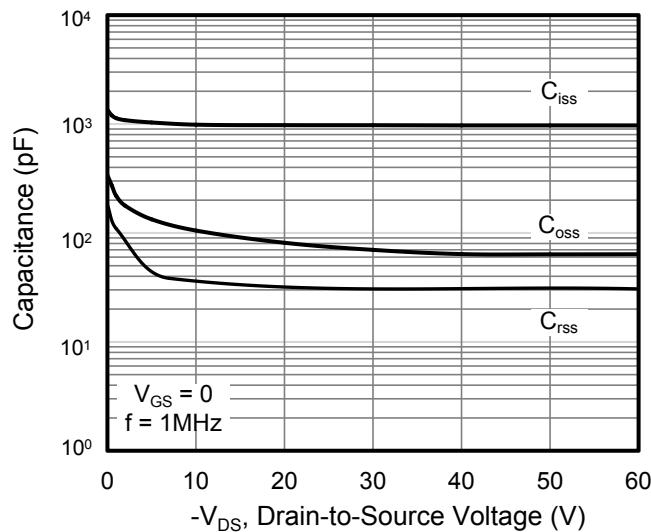


Figure 8. Gate Charge

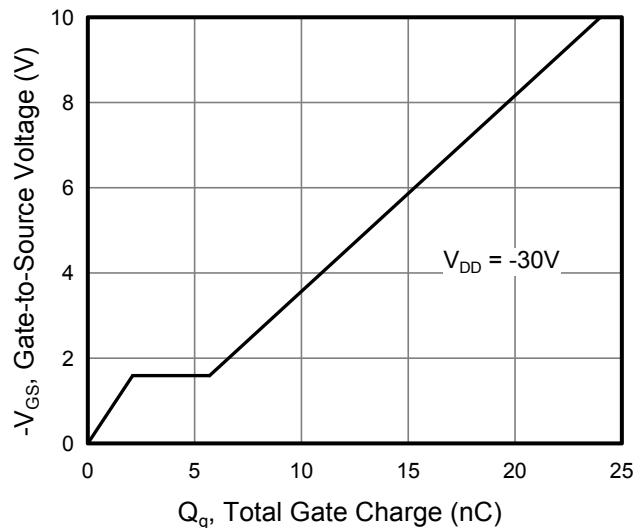


Figure 9. Transient Thermal Impedance

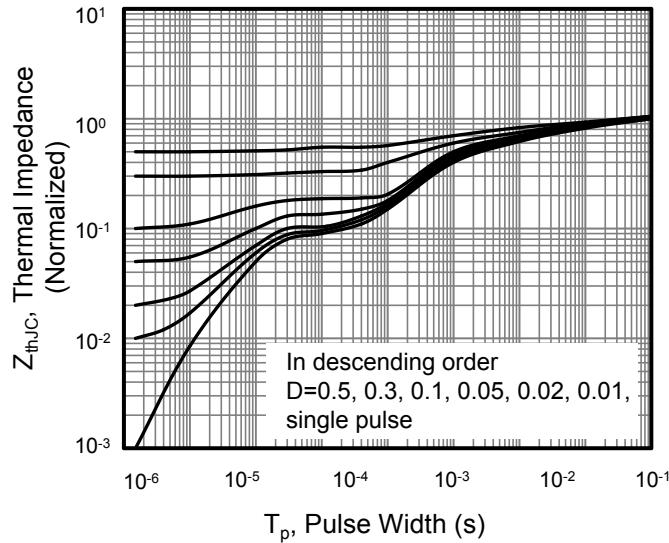
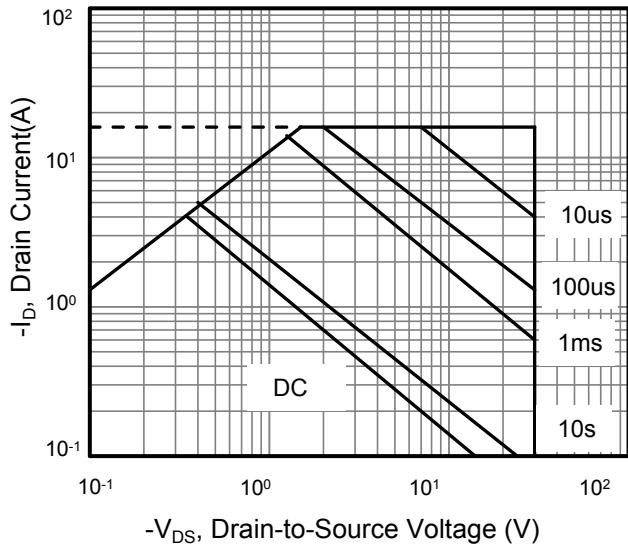
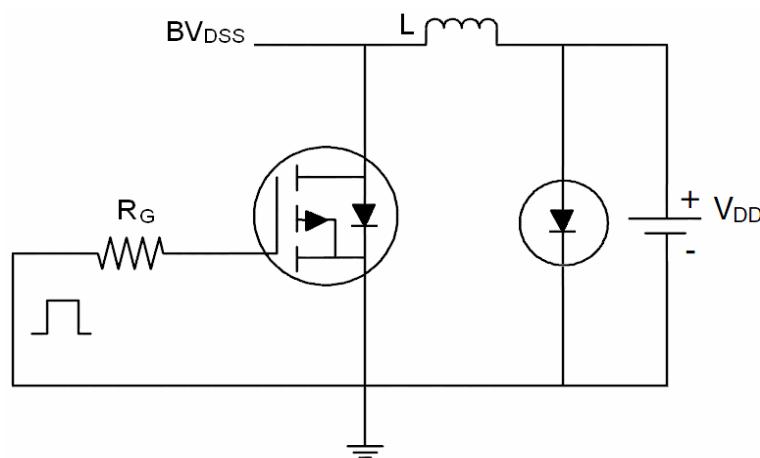


Figure 10. Safe Operating Area

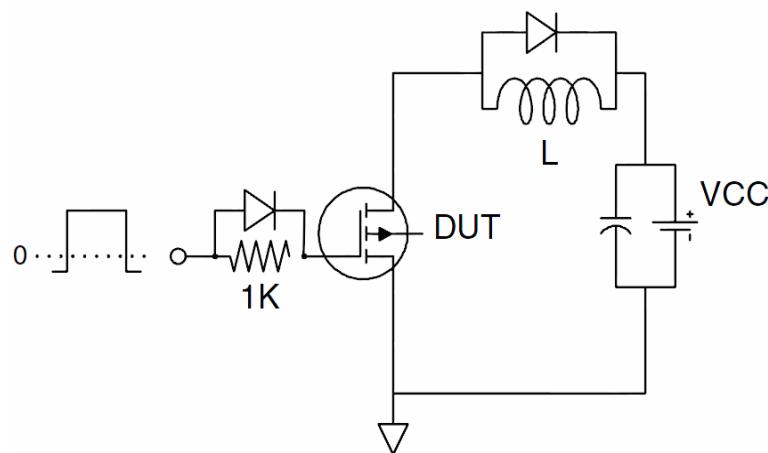


Test Circuit

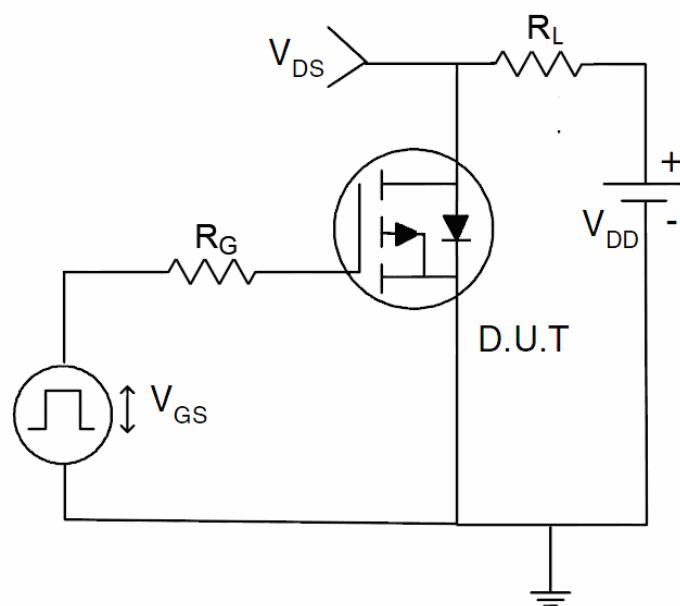
1) E_{AS} Test Circuit



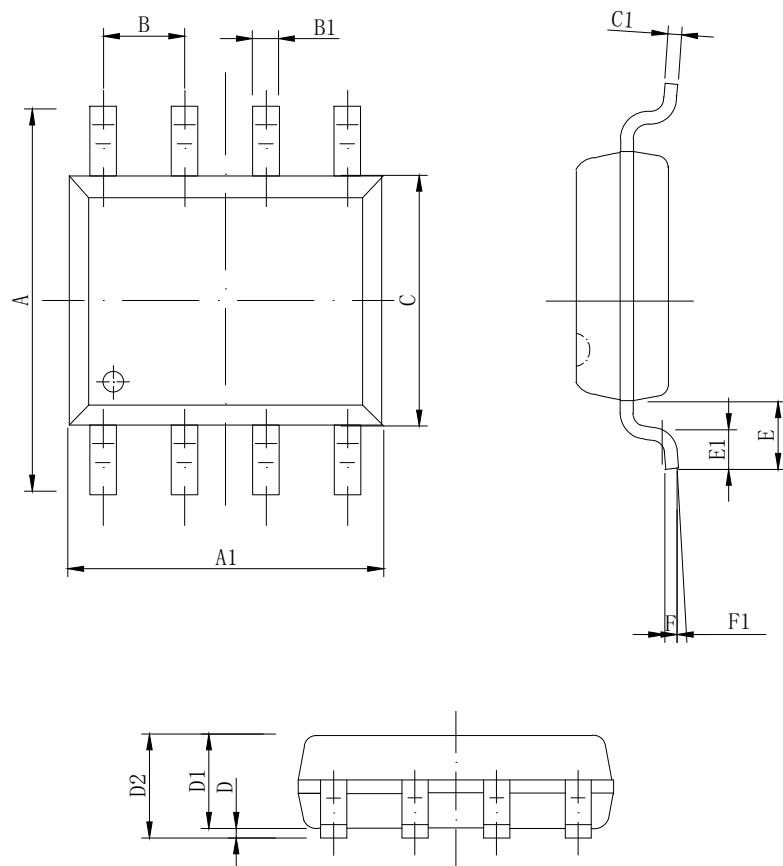
2) Gate Charge Test Circuit



3) Switch Time Test Circuit



SOP-8 Package information



DIM	MIN	NOM	MAX
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B	1.270BSC		
B1	0.35 ^ 8x	0.40 ^ 8x	0.45 ^ 8x
C	3.780	3.880	3.980
C1	-	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
E	1.060 REF		
E1	0.400	0.700	0.100
F	0.250BSC		
F1	2°	4°	6°

All Dimensions in mm