MKM04EL04TD2-TN

NAND Flash and Mobile Memory

162-Ball MCP Specification

4Gb(512Mb x8) NAND Flash

with 4Gb(128Mb x32) LPDDR2

4Gb(512Mb x8) NAND Flash

Featues

- Organization

	x8
Memory cell array	4352 x 128K x 8
Register	4352 x 8
Page size	4352 bytes
Block size	(256K + 16K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 2008 blocks
  Max 2048 blocks

- Power supply
  VCC = 1.8V (1.7 V ~ 1.95V)

- Access time

Cell array to register	25 µs max
Serial Read Cycle	25 ns min (CL=30pF)

- Program/Erase time

Auto Page Program	300 µs/page typ.
Auto Block Erase	3.5 ms/block typ.

- Operating current

Read (50 ns cycle)	30 mA max.
Program (avg.)	30 mA max
Erase (avg.)	30 mA max
Standby	50 µA max

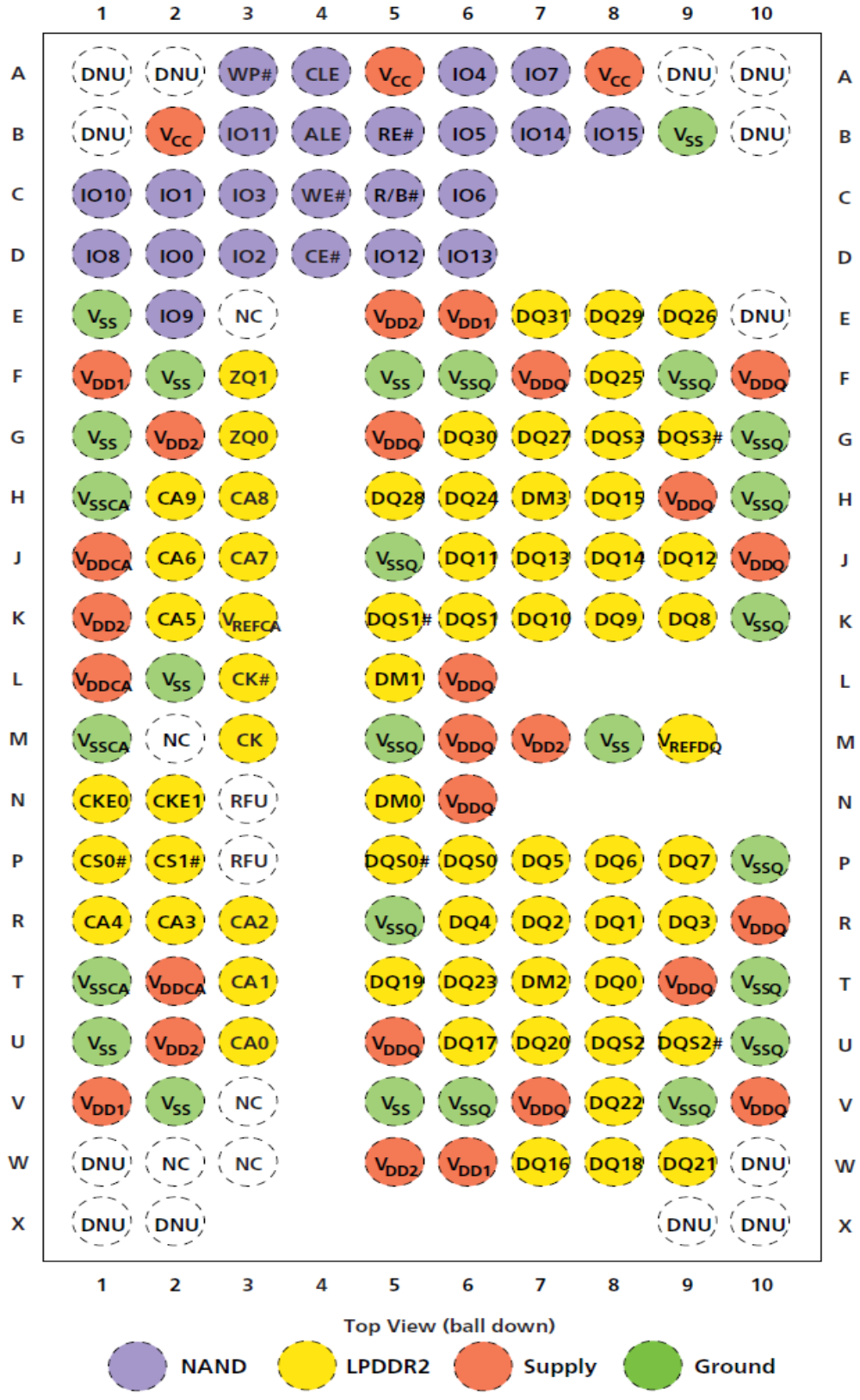
- 8-bits ECC for 512Btyes is required

4Gb(128Mb x32) LPDDR2

Feature

- Double-data rate architecture; two data transfer per clock cycle
- Bidirectional, data strobe (DQS, /DQS) is transmitted/received with data, to be used in capturing data at the receiver
- Eight internal banks for concurrent operation
- Data mask (DM) for write data
- Programmable Burst Lengths: 4 ,8 or 16
- Burst type: Sequential or interleave
- Programmable RL (Read latency) & WL (Write latency)
- Clock Stop capability during idle period
- Auto Precharge for each burst access
- Configurable Drive Strength (DS)
- Auto Refresh and Self Refresh Modes
- Differential clock inputs (CK and /CK)
- Differential data strobe (DQS and /DQS)
- Commands & addresses entered on both positive & negative CK edge; data and data mask referenced to both edges of DQS
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- HSUL_12 compatible inputs (High Speed Un-terminated Logic 1.2V)
- VDD2/VDDCA/VDDQ= 1.14~1.30V; VDD1=1.70~1.95
- Speed: 667MHz / 800MHz / 1066MHz
- 8-Banks / 14bits rows / 10bits columns
- Every Bank is organized as 16384 rows by 1024 columns by 32bits.

MCP Signal Assignments



MCP Ball Descriptions

NAND Flash

Symbol	Type	Function
I/O0 ~ I/O7 (X8) I/O0 ~ I/O15 (X16)	Input/output	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	Input	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	Input	ADDRESS LATCH ENABLE The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	Input	CHIP ENABLE The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	Input	READ ENABLE The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Input	WRITE ENABLE The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Input	WRITE PROTECT The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Input	READY/BUSY OUTPUT The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	Supply	POWER VCC is the power supply for device.

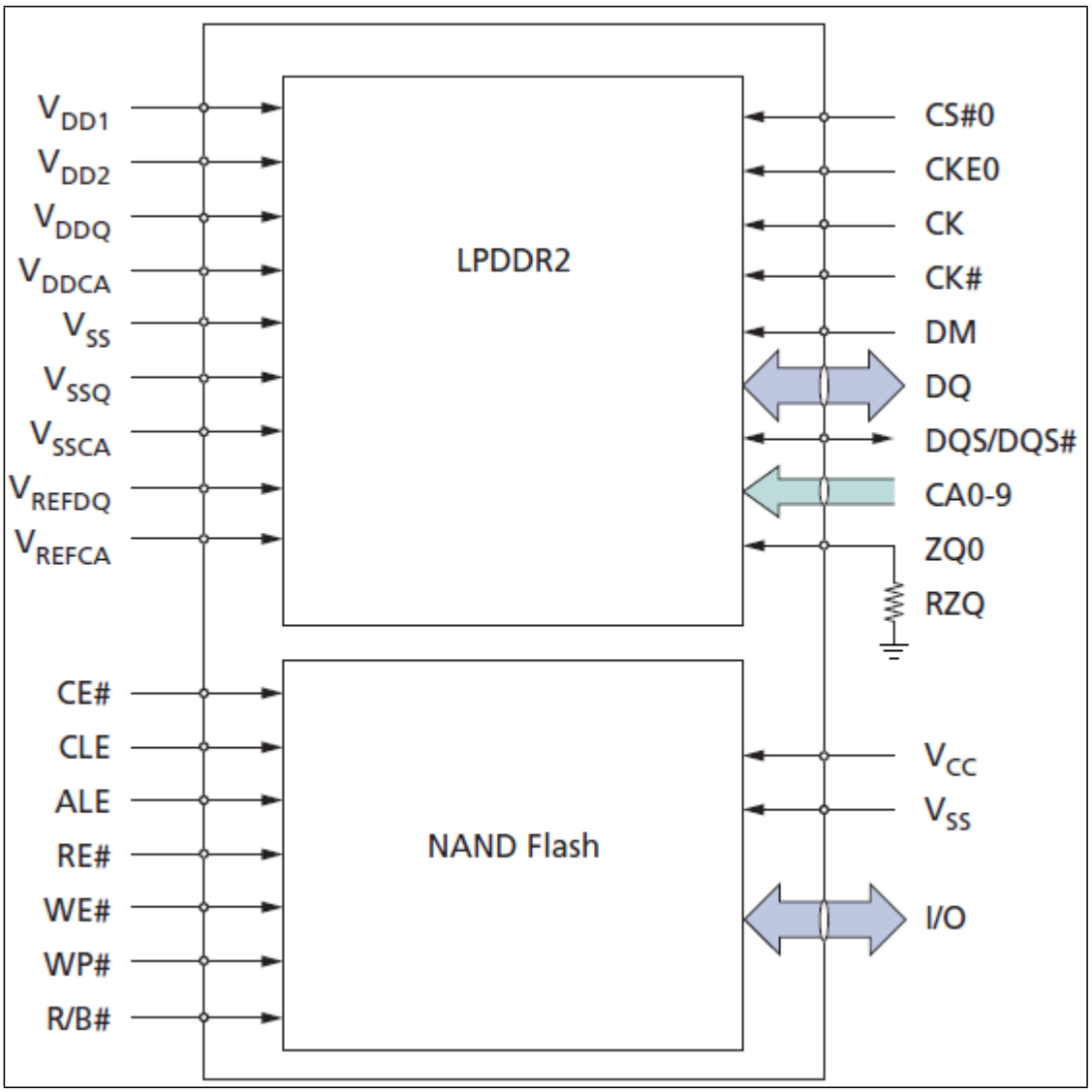
VSS	Supply	GROUND
N.C.	–	NO CONNECTION Lead is not internally connected.

LPDDR2

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All Double Data Rate (DDR) CA input signals are sampled on both positive and negative edge of CK. CS_n and CKE inputs are sampled at the positive edge of CK. AC timings are referenced to clock.
CKE	Input	Clock Enable: CKE high activates, and CKE low deactivates internal clock signals, and device input buffers and output drivers. Power saving modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA0 – CA9	Input	Command/Address Inputs: Uni-directional command/address bus inputs. Provide the command and address inputs according to the command truth table. CA is considered part of the command code.
DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matched the DQ and DQS (or /DQS). DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQ0-DQ31	Input/output	Data Bus: Bi-directional Input / Output data bus.
DQS, DQS# DQS0-3,DQS0#-3#	Input/output	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and Differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data, and centered with write data. DQS0 & DQS0# corresponds to the data on DQ0-DQ7, DQS1 & DQS1# corresponds to the data on DQ8-DQ15, DQS2 & DQS2# corresponds to the data on DQ16-DQ23, DQS3 & DQS3# corresponds to the data on DQ24-DQ31.
ZQ	Input	Reference Pin for Output Drive Strength Calibration. External impedance (240-ohm): this signal is used to calibrate the device output impedance.
VREFDQ, VREFCA	Supply	Reference Voltage: VREFDQ is reference for DQ input buffers. VREFCA is reference for Command

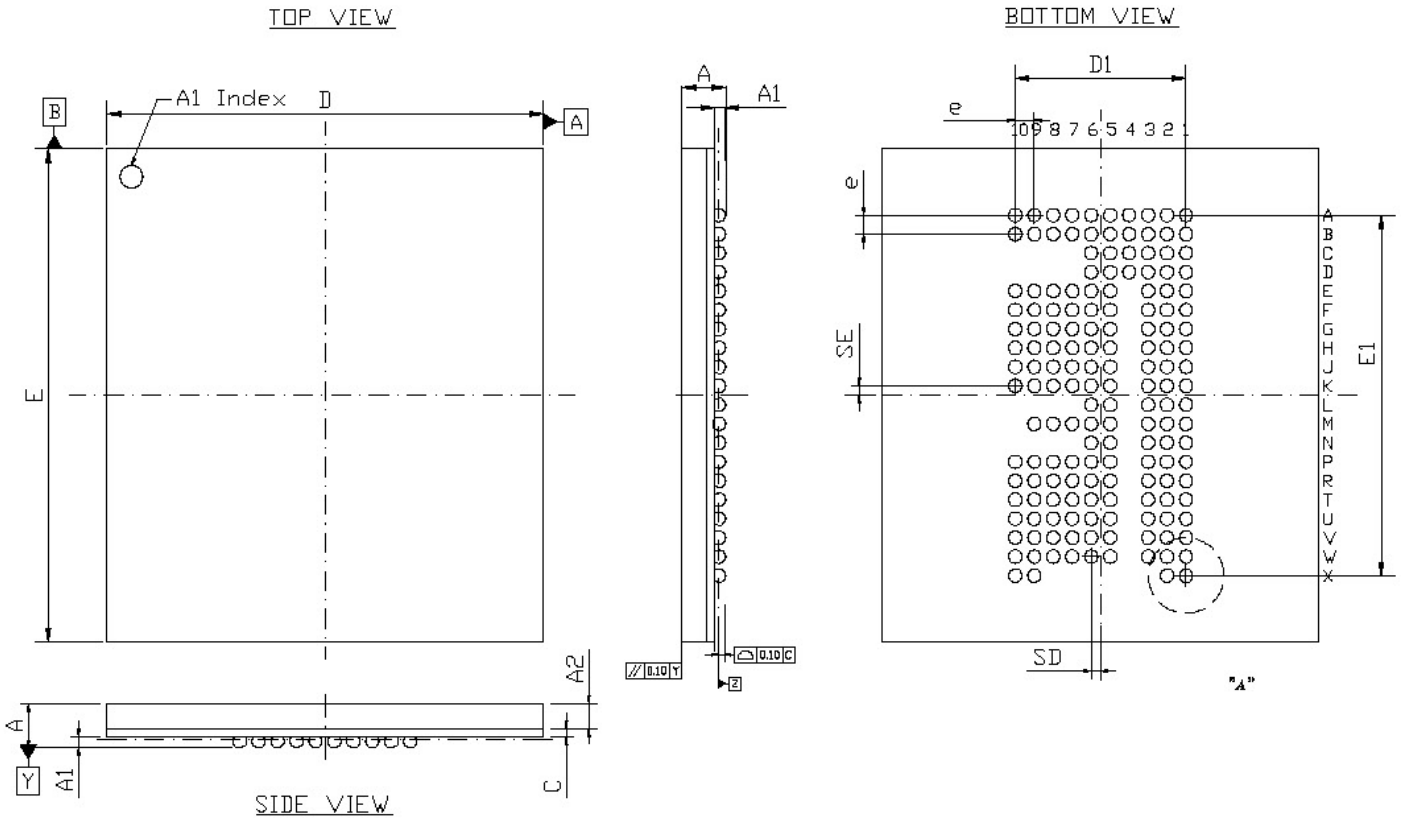
		/ Address input buffers.
NC	–	NO CONNECTION Lead is not internally connected.
VDDQ	Supply	DQ Power Supply: Isolated on the die for improved noise immunity.
VSSQ	Supply	DQ Ground: Isolated on the die for improved noise immunity.
VDDCA	Supply	Command / Address Power Supply.
VSSCA	Supply	Command / Address Ground: Isolated on the die for improved noise immunity.
VDD1	Supply	Core power supply 1.
VDD2	Supply	Core power supply2.
Vss	Supply	Common Ground.

MCP Functional Overview



Block Diagram

MCP Package Dimensions



REF.	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	——	——	1.000	——	——	0.039
A1	0.225	——	0.275	0.009	——	0.011
A2	0.465	——	0490	0.018	——	0.019
C	0.180	0.210	0.240	0.007	0.008	0.009
øb	0.25	0.30	0.35	0.010	0.012	0.014
D	11.40	11.50	11.60	0.449	0.453	0.457
D1	4.50 BSC			0.177 BSC		
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.50 BSC			0.374 BSC		
SE	0.250 BSC			0.010 BSC		
SD	0.250 BSC			0.010 BSC		
e	0.500 BSC			0.026 BSC		

4Gbit NAND Flash(512M x 8bit)

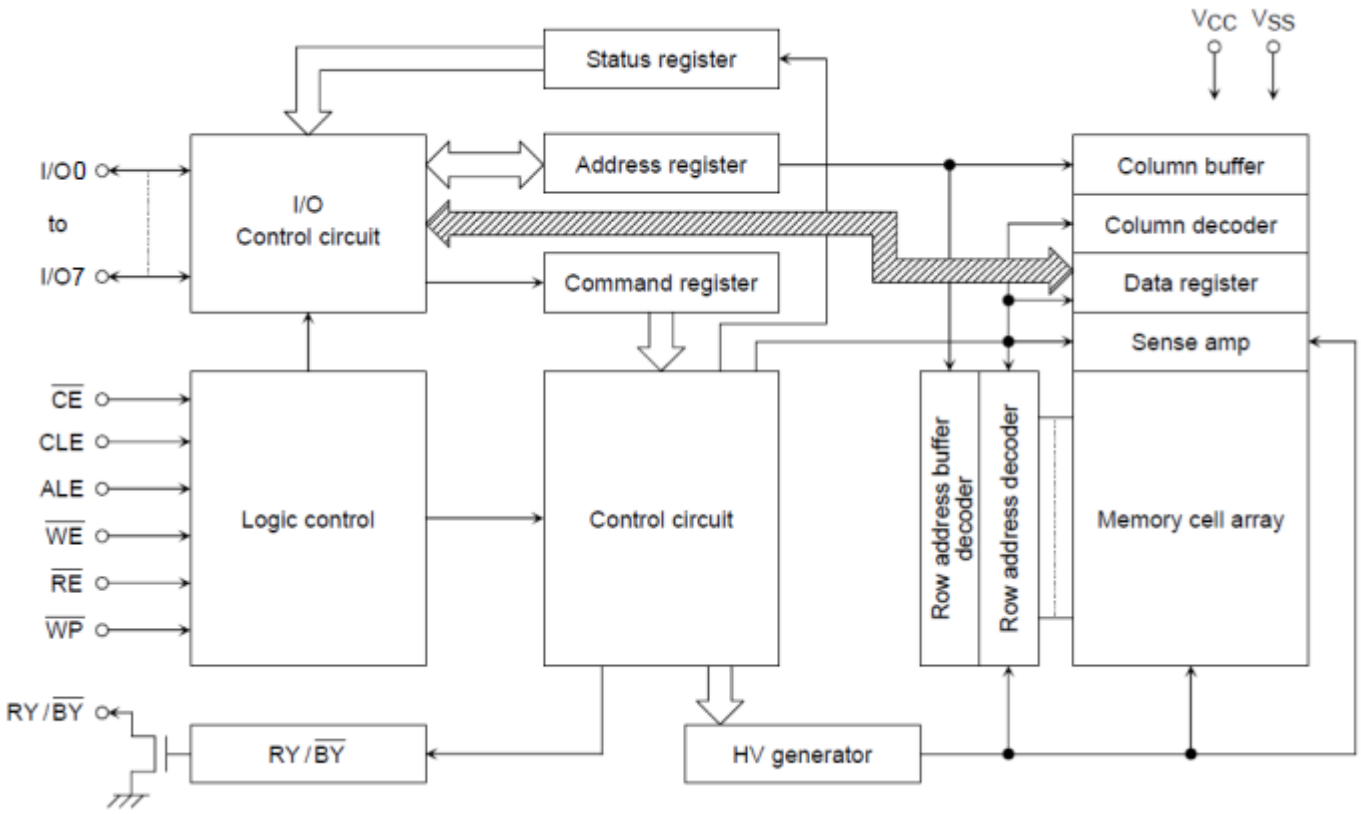
Descriptions

The Device is a single 1.8V 4 Gbit (4,563,402,752 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E2PROM) organized as (4096 + 256) bytes × 64 pages × 2048blocks.

The Device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

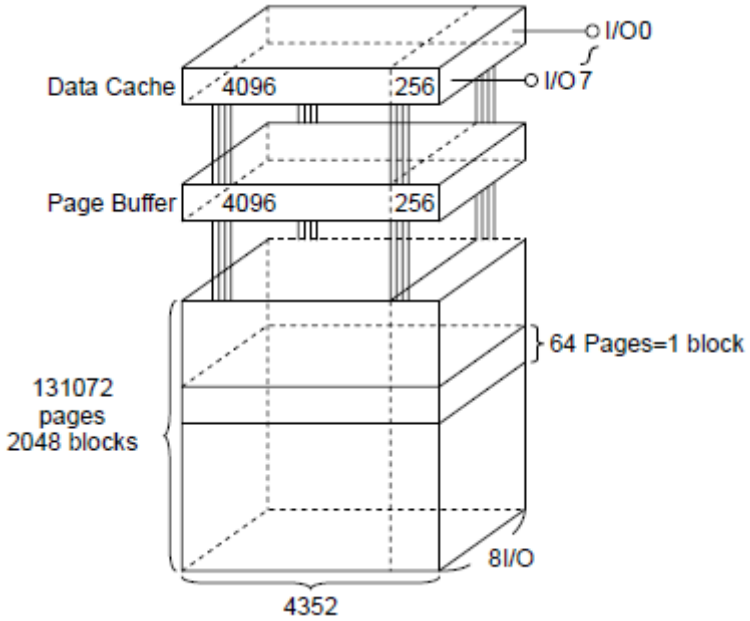
The device has two 4352-bytes static registers which allow program and read data to be transferred between the register and the memory cell array in 4352-byte increments. The Erase operation is implemented in a single block unit (256Kbytes + 16Kbytes: 4352bytes × 64pages).

Block Diagram



Functional Block Diagram

Schematic Cell Layout and Address Assignment



A page consists of 4352bytes in which 4096 bytes are used for main memory storage and 256bytes are for redundancy or for other uses.

1 page = 4352 bytes

1 block = 4352 bytes X 64 pages = (256K + 16K) bytes

Capacity = 4352 bytes X 64 pages X 2048 blocks = 570,425,344 bytes

= 4,563,402,752 bits

	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	L	PA16

CA0 to CA12 : Column address

PA0 to PA16 : Page address

PA0 to PA5 : NAND address in block

PA6 to PA16 : Block address

Operation Mode: Logic and Command Tables

Logic Tables

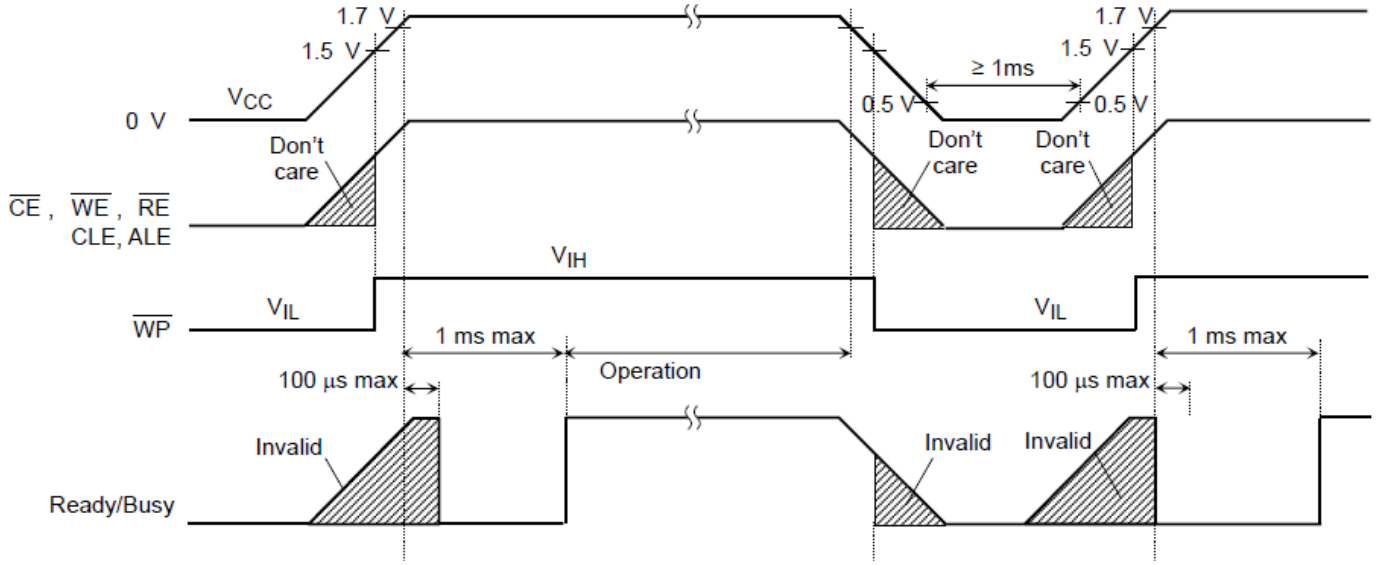
	CLE	ALE	CE#	WE#	RE#	WP#
Command Input	H	L	L		H	X
Data Input	L	L	L		H	H
Address Input	L	H	L		H	X
Serial Data Output	L	L	L	H		X
During Program (Busy)	X	X	X	X	X	H
During Erase (Busy)	X	X	X	X	X	H
During Read (Busy)	X	X	H	X	X	X
	X	X	L	H	H	X
Program / Erase Inhibit	X	X	X	X	X	L
Standby	X	X	H	X	X	0V / VCC

Command Tables

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	—	
Read Start for Last Page in Read Cycle with Data Cache	3F	—	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Program with Data Cache	80	15	
Multi Page Program	80	11	
	81	15	
	81	10	
Read for Page Copy (2) with Data Out	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
Status Read for Multi-Page Program or Multi Block Erase	71	—	○
Reset	FF	—	○

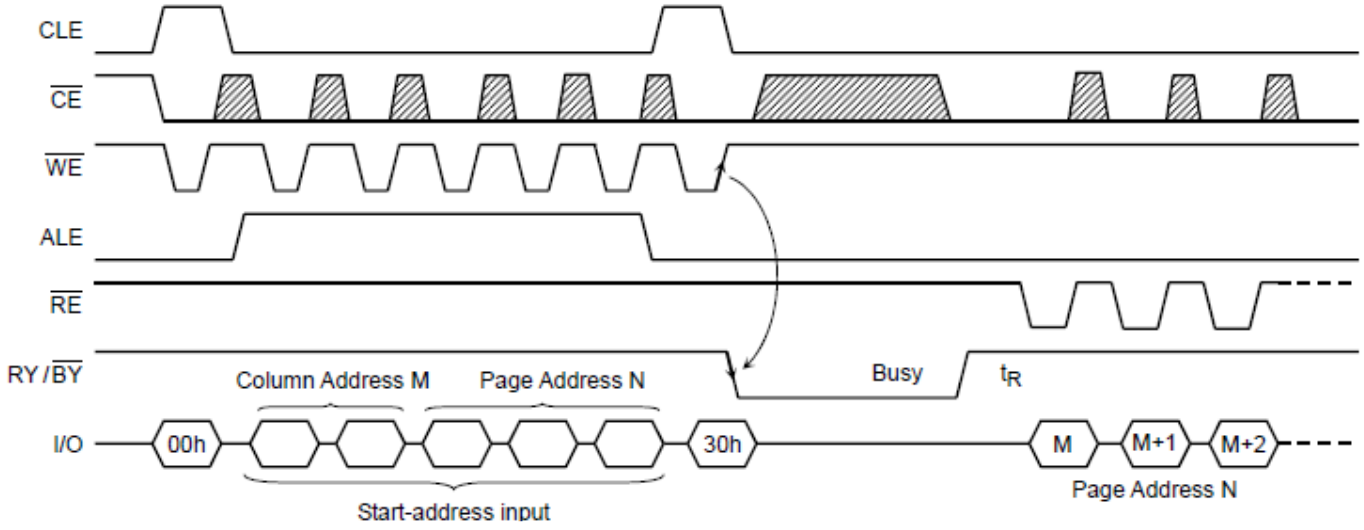
Power On/Off Sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence. The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h. The WP signal is useful for protecting against data corruption at power-on/off.



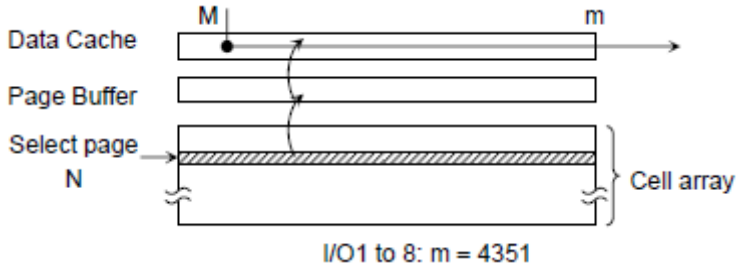
Device Operation

Read



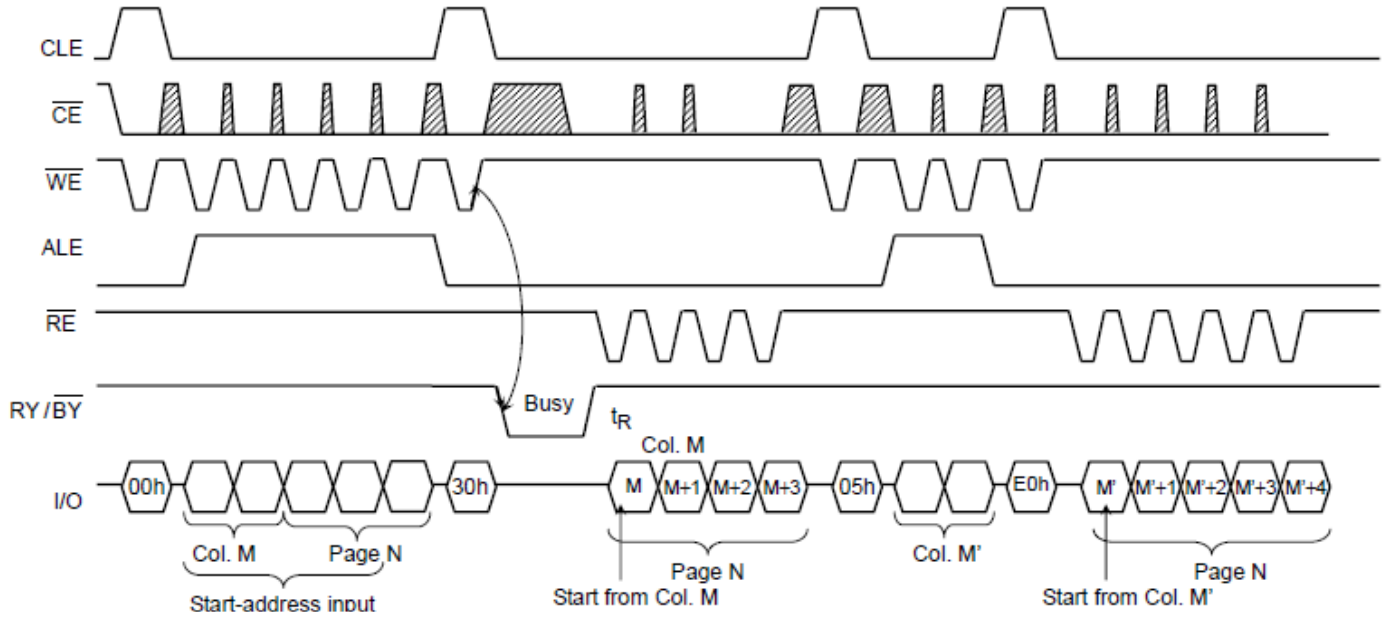
Read mode is set when the 00h and 30h commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence,

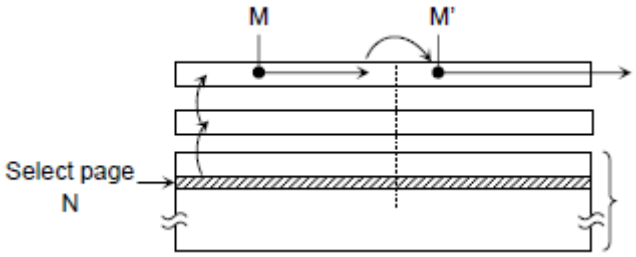
00h command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only five address cycles and 30h command. Refer to the figures below for the sequence and the block diagram.



A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of WE in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period. After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle





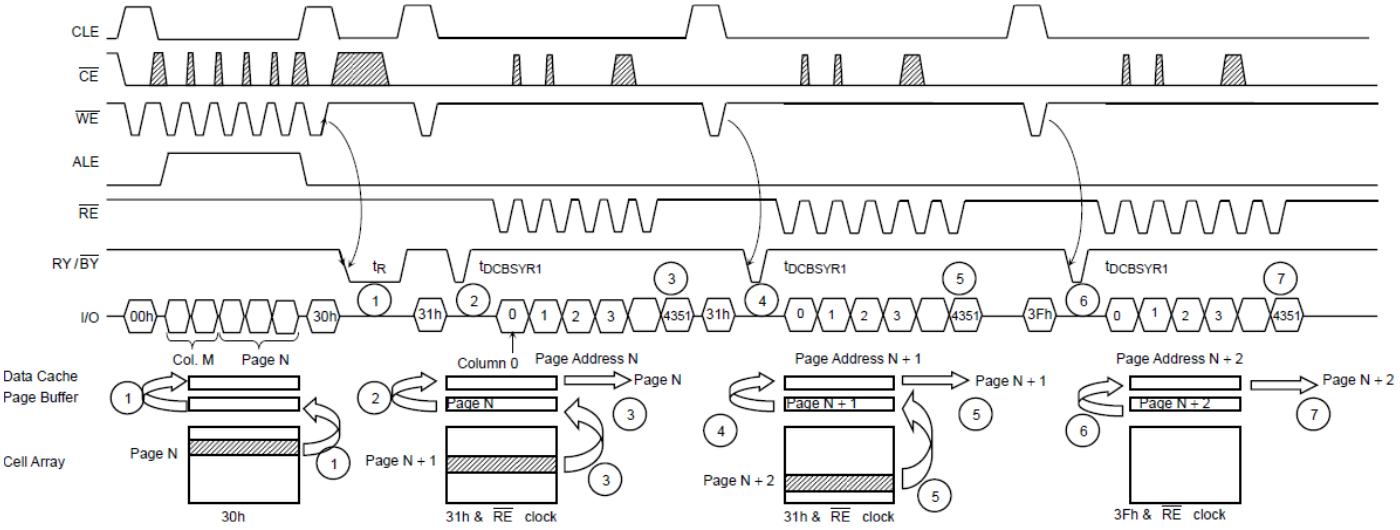
During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new

column address. Random Column Address Change operation can be done multiple times within the same page.

Read Operation with Read Cache

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning. If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

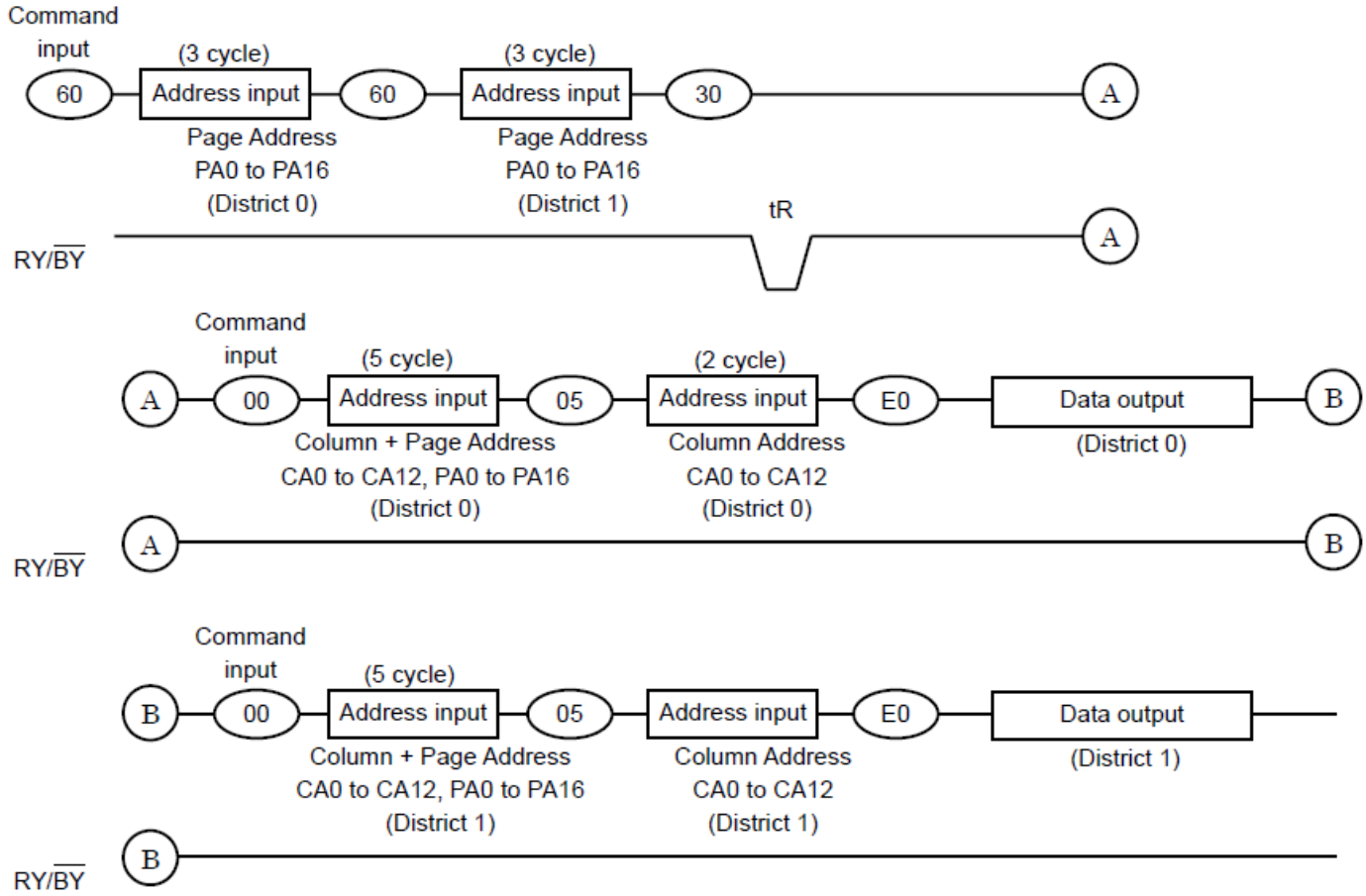
1. Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.
2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.
3. Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.
4. The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
5. Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously
6. The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
7. Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

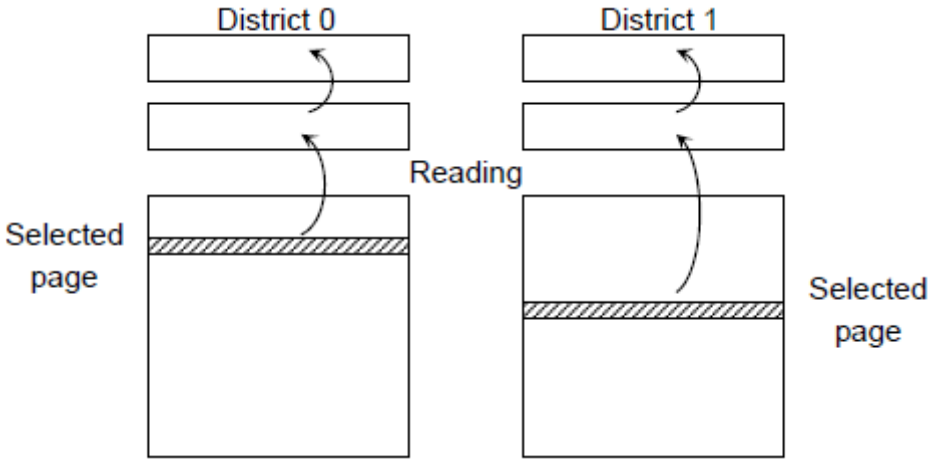


Multi Page Read Operation

(1) Multi Page Read without Data Cache

The sequence of command and address input is shown below. Same page address (PA0 to PA5) within each district has to be selected.

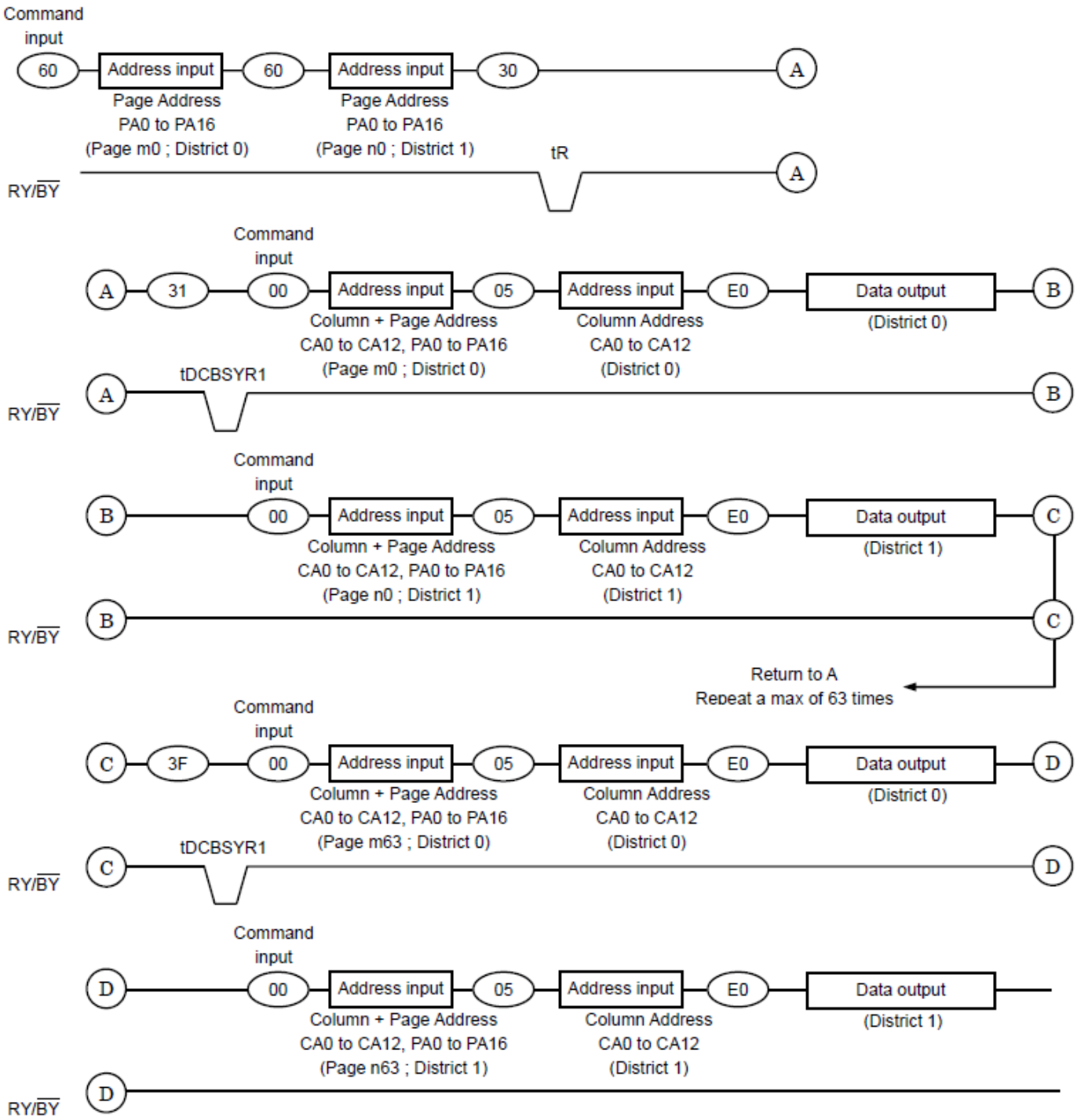




The data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of WE in the 30h command input cycle (after the 2 Districts address information has been latched). The device will be in the Busy state during this transfer period. After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start address designated in the address input cycle.

(2) Multi Page Read with Data Cache

When the block address changes (increments) this sequenced has to be started from the beginning. The sequence of command and address input is shown below. Same page address (PA0 to PA5) within each district has to be selected.



Internal addressing in relation with the Districts: to use Multi Page Read operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

  District 0: Block 0, Block 2, Block 4, Block 6,…, Block 2046

  District 1: Block 1, Block 3, Block 5, Block 7,…, Block 2047

Address input restriction for the Multi Page Read operation: There are following restrictions in using

Multi Page Read, maximum one block should be selected from each District. Same page address (PA0 to PA5) within two districts has to be selected. For example,

(60) [District 0, Page Address 0x00000] (60) [District 1, Page Address 0x00040] (30)

(60) [District 0, Page Address 0x00001] (60) [District 1, Page Address 0x00041] (30)

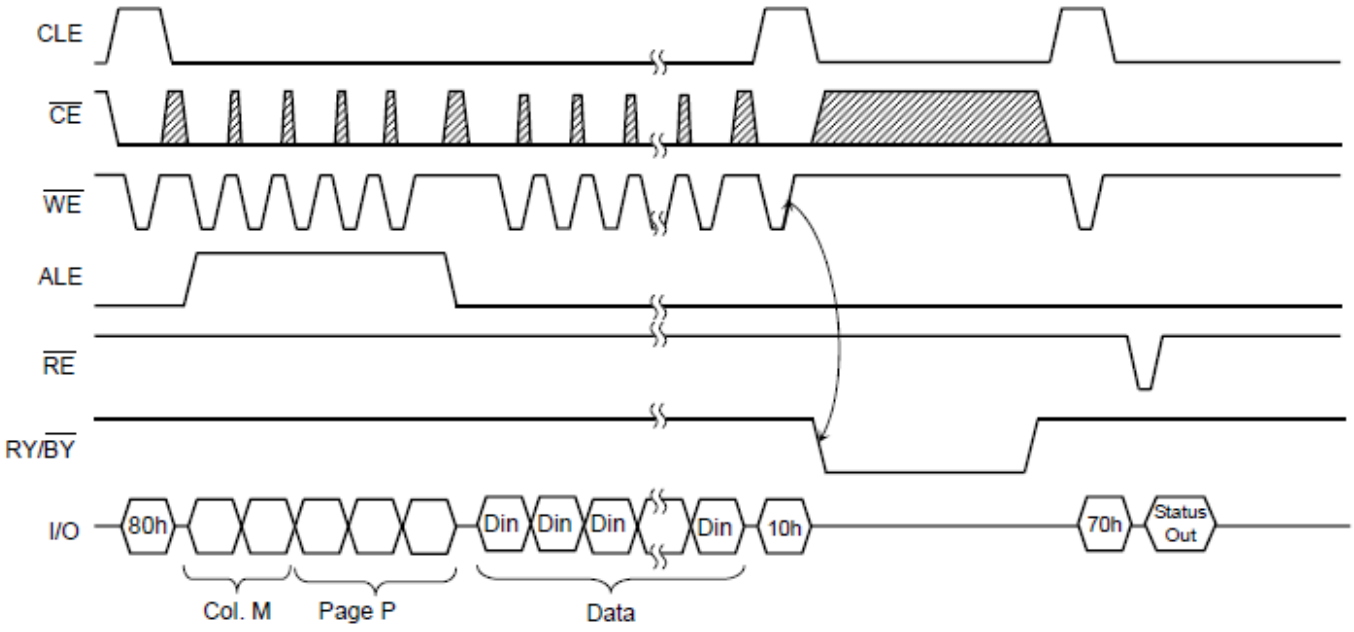
(Acceptance)There is no order limitation of the District for the address input. For example, following operation is accepted,

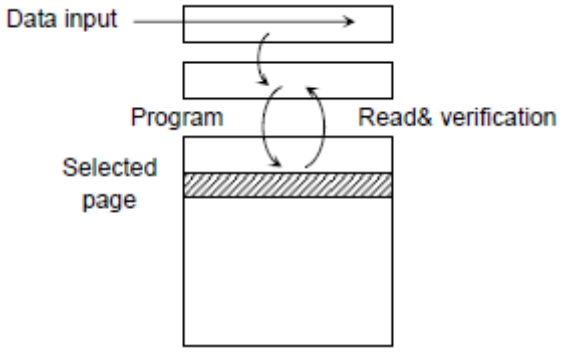
(60) [District 0] (60) [District 1] (30)

(60) [District 1] (60) [District 0] (30)

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a 10h Program command after the address and data have been input. The sequence of command, address and data input is shown below.



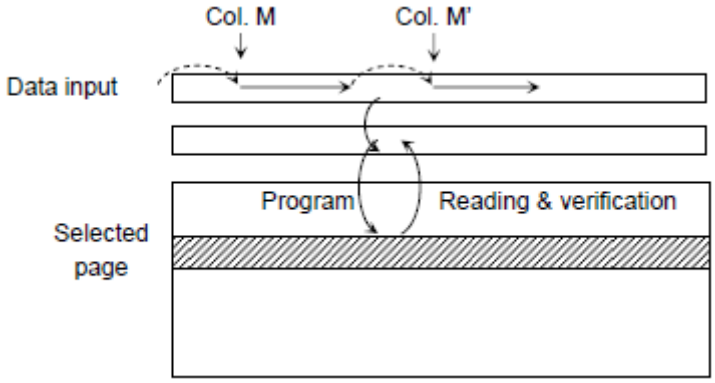


The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of WE following input of the 10h command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not

succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

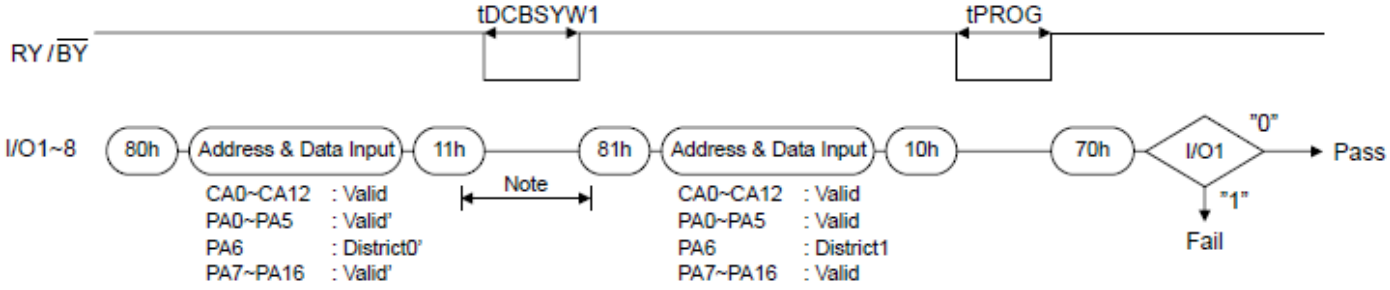
Random Column Address Change in Auto Page Program Operation

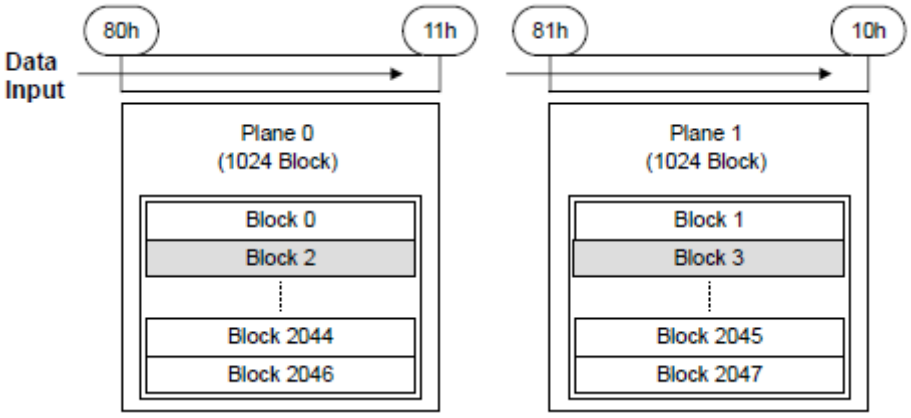
The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation. Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



Multi Page Program

The device has a Multi Page Program, which enables even higher speed program operation compared to Auto Page Program. The sequence of command, address and data input is shown below. Although two planes are programmed simultaneously, pass/fail is not available for each page by 70h command when the program operation completes. Status bit of I/O 1 is set to 1 when any of the pages fails. Limitation in addressing with Multi Page Program is shown below.





Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning. Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache.

1. Data for Page N is input to Data Cache.
2. Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State (tDCBSYW2).
3. Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.
4. By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 (tDCBSYW2).
5. Data for Page N + P is input to the Data Cache while the data of the Page N + P – 1 is being programmed.
6. The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

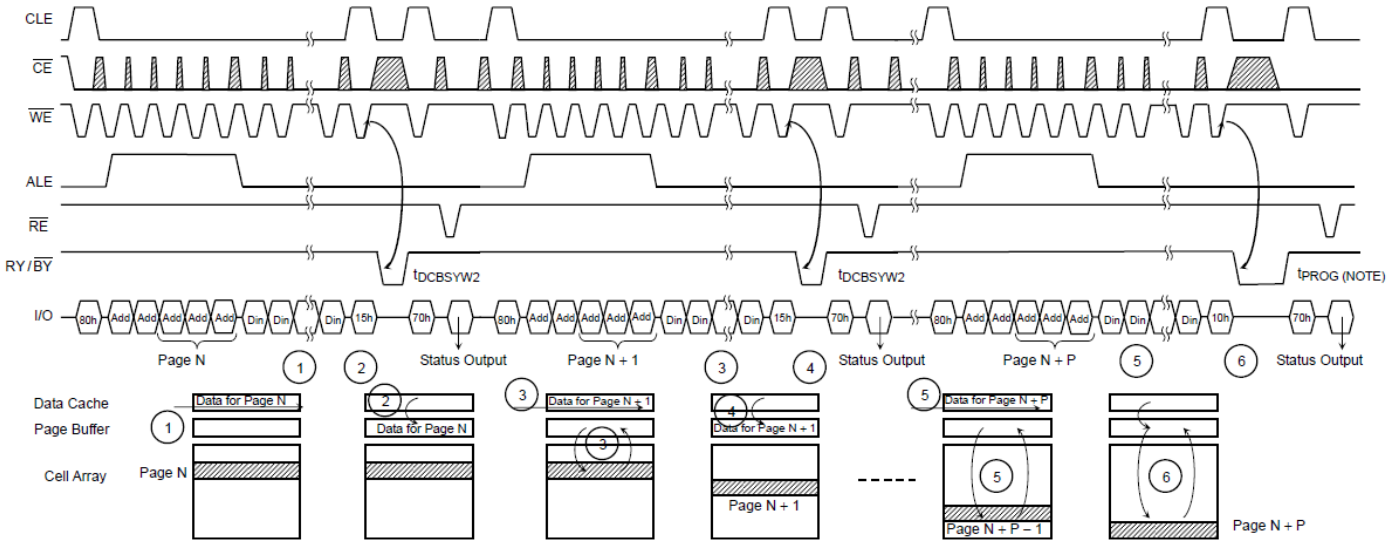
I/O1 : Pass/fail of the current page program operation.

I/O2 : Pass/fail of the previous page program operation.

The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

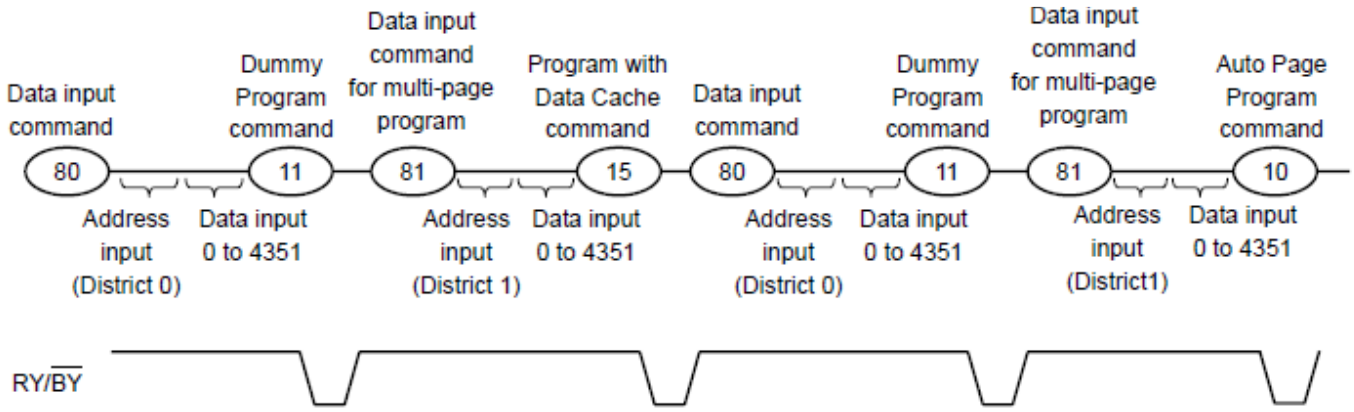
Status on I/O1: Page Buffer Ready/Busy is Ready State. The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or RY / BY pin after the 10h command.

Status on I/O2: Data Cache Read/Busy is Ready State. The Data Cache Ready/Busy is output on I/O7 by Status Read operation or RY / BY pin after the 15h command.

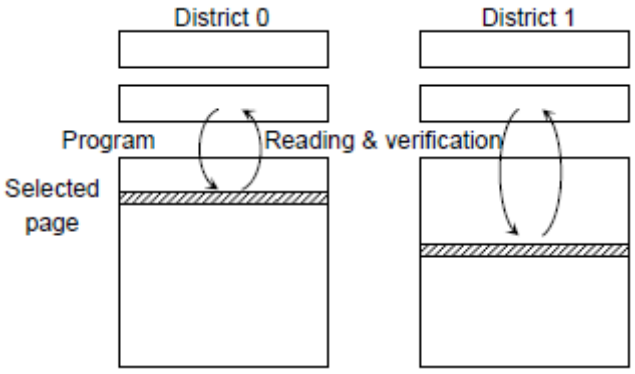


Multi Page Program with Data Cache

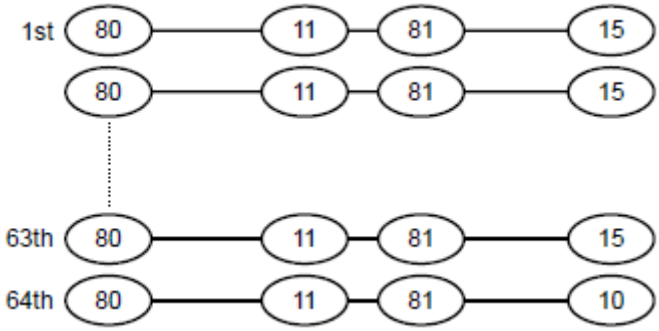
The device has a Multi-Page Program with Data Cache operation, which enables even higher speed program operation compared to Auto Page Program with Data Cache as shown below. When the block address changes (increments) this sequenced has to be started from the beginning.



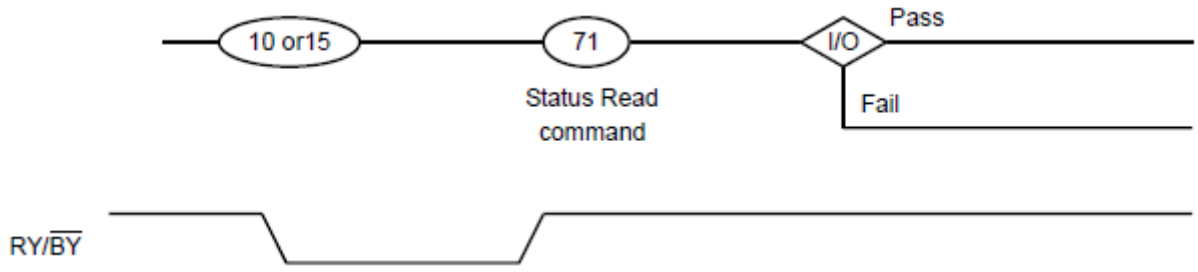
The data is transferred (programmed) from the page buffer to the selected page on the rising edge of WE# following input of the 15h or 10h command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.



Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 64 times with incrementing the page address in the blocks, and then input the last page data of the blocks, 10h command executes final programming. Make sure to terminate with 81h-10h-command sequence.



After the 15h or 10h command, the results of the above operation is shown through the 71h Status Read command.



The 71h command Status description is as below.

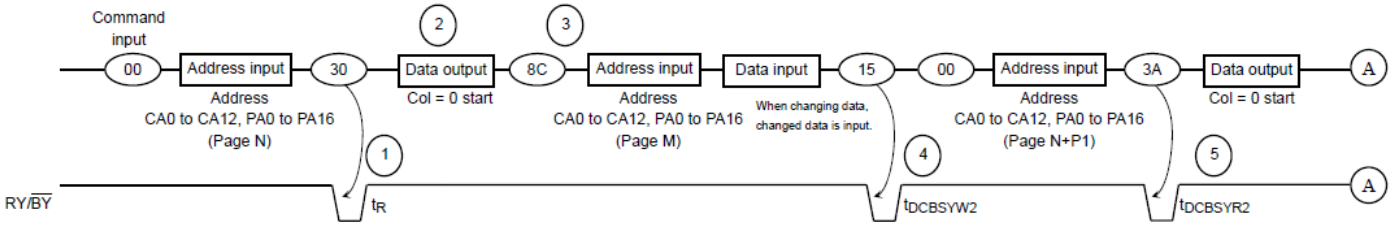
	Status	Output

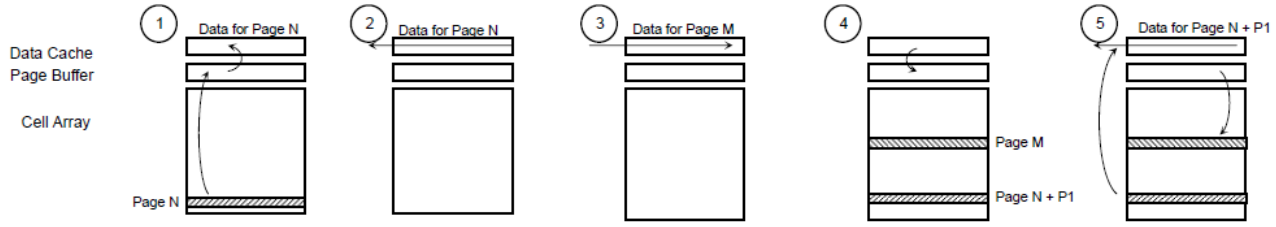
IO0	Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
IO1	District 0 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
IO2	District 1 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
IO3	District 0 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
IO4	District 1 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
IO5	Ready/Busy	Ready:1	Busy: 0
IO6	Data Cache Ready/Busy	Ready:1	Busy: 0
IO7	Write Protect	Protect: 0	Not Protect: 1

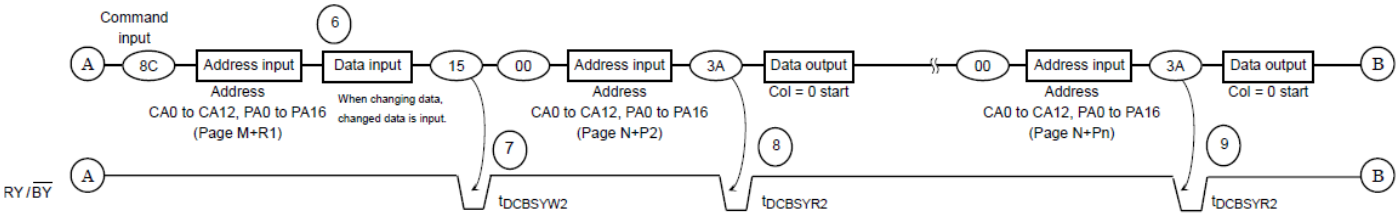
Page Copy (2)

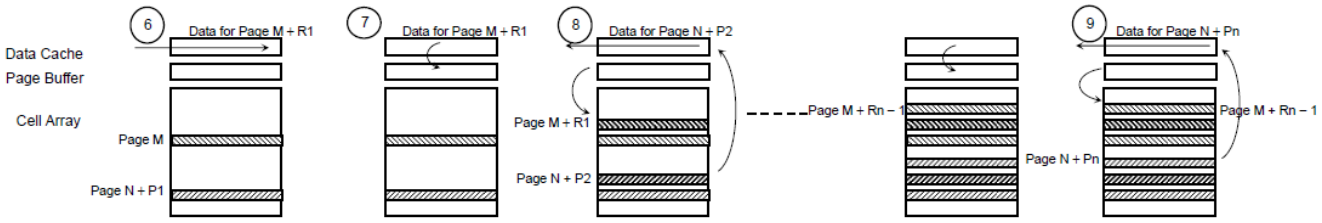
By using Page Copy (2), data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning. Page Copy (2) operation is as following.

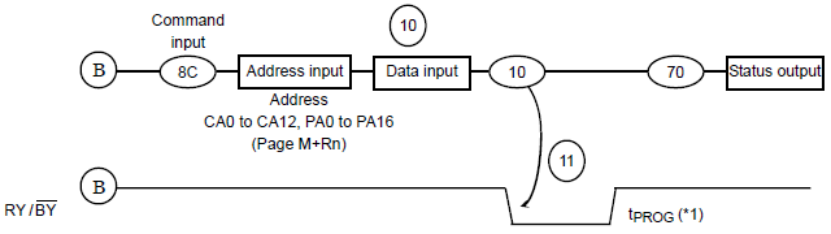
1. Data for Page N is transferred to the Data Cache.
2. Data for Page N is read out.
3. Copy Page address M is input and if the data needs to be changed, changed data is input.
4. Data Cache for Page M is transferred to the Page Buffer.
5. After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.
6. Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.
7. After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8. By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9. The data in the Page Buffer is programmed to Page M + Rn − 1. Data for Page N + Pn is transferred to the Data Cache.
10. Copy Page address (M + Rn) is input and if the data needs to be changed, changed data is input.
11. By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

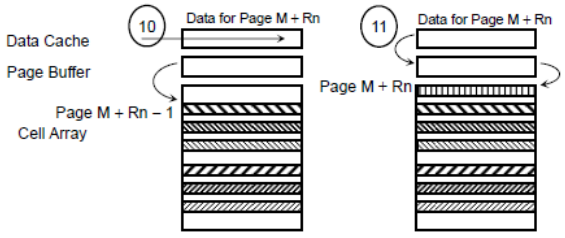

Command input
00
Address input
Address
CA0 to CA12, PA0 to PA16
(Page N)
30
Data output
Col = 0 start
8C
Address input
Address
CA0 to CA12, PA0 to PA16
(Page M)
Data input
When changing data, changed data is input.
15
00
Address input
Address
CA0 to CA12, PA0 to PA16
(Page N+P1)
3A
Data output
Col = 0 start
A
RY/BY
tR
tDCBSYW2
tDCBSYR2


Data Cache
Page Buffer
Cell Array
Page N
Data for Page N
Data for Page M
Page M
Page N + P1
Data for Page N + P1


Command input
A
8C
Address input
Address
CA0 to CA12, PA0 to PA16
(Page M+R1)
Data input
When changing data, changed data is input.
15
00
Address input
Address
CA0 to CA12, PA0 to PA16
(Page N+P2)
3A
Data output
Col = 0 start
00
Address input
Address
CA0 to CA12, PA0 to PA16
(Page N+Pn)
3A
Data output
Col = 0 start
B
RY/BY
tDCBSYW2
tDCBSYR2
tDCBSYR2

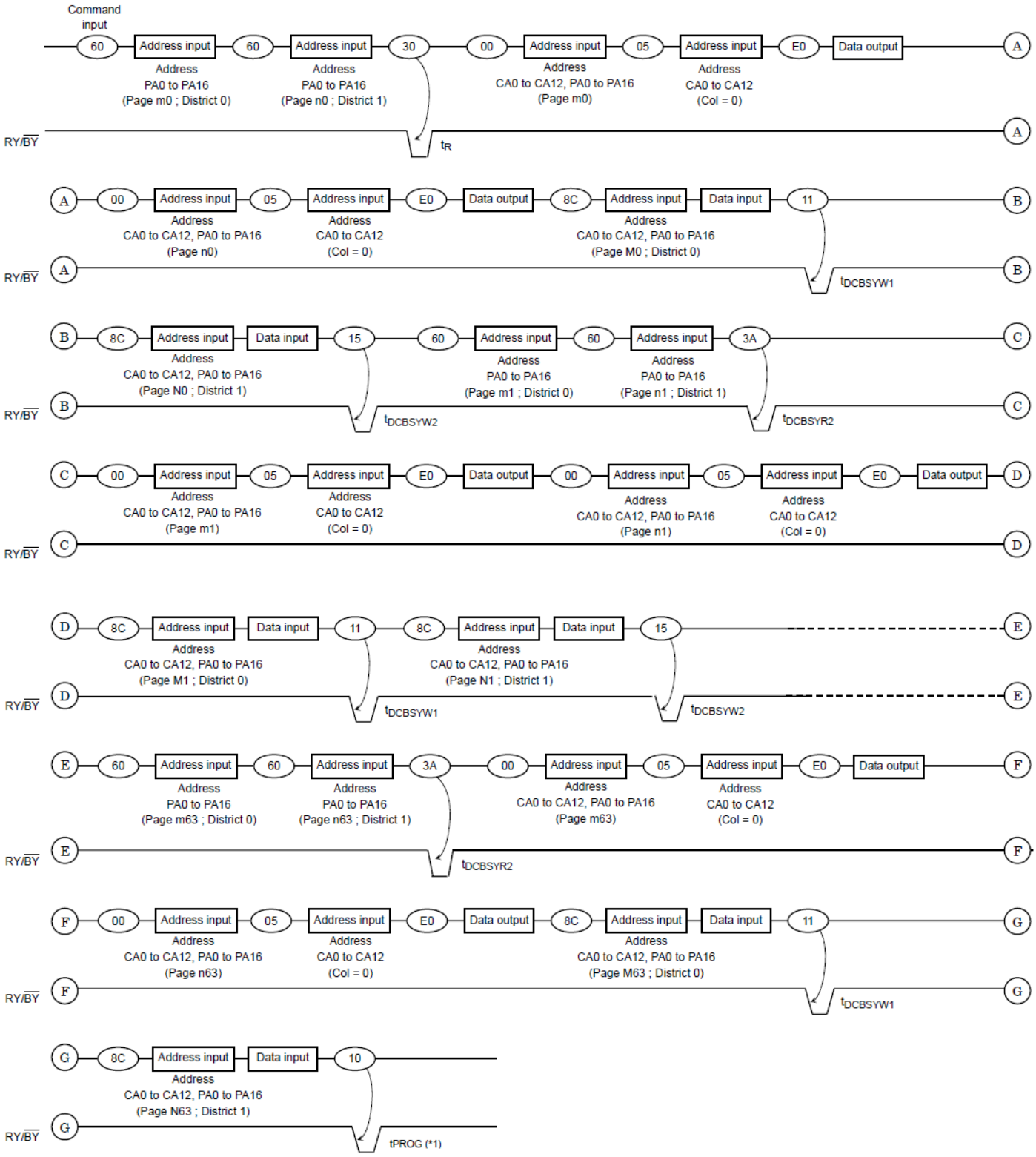

Data Cache
Page Buffer
Cell Array
Page M
Page N + P1
Data for Page M + R1
Page M + R1
Page N + P2
Data for Page N + P2
Page M + Rn – 1
Page N + Pn
Data for Page N + Pn


Command input
B
8C
Address input
Address
CA0 to CA12, PA0 to PA16
(Page M+Rn)
Data input
10
70
Status output
11
RY/BY
tPROG (*1)


Data Cache
Page Buffer
Page M + Rn – 1
Cell Array
Data for Page M + Rn
Page M + Rn

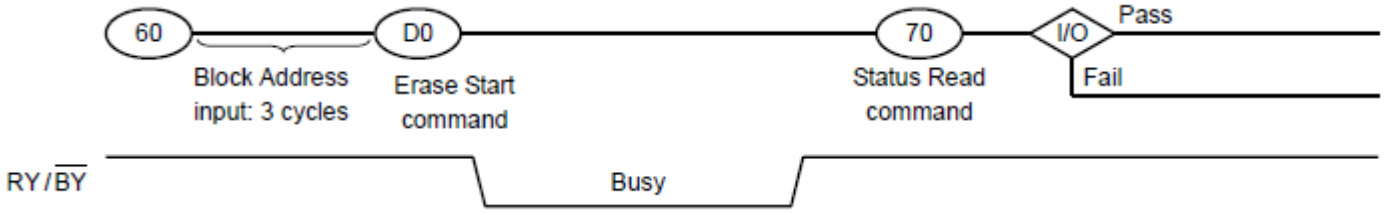
Multi Page Copy (2)

By using Multi Page Copy (2), data in two pages can be copied to other pages after the data has been read out. When each block address changes (increments) this sequence has to be started from the beginning. Same page address (PA0 to PA5) within two districts has to be selected.



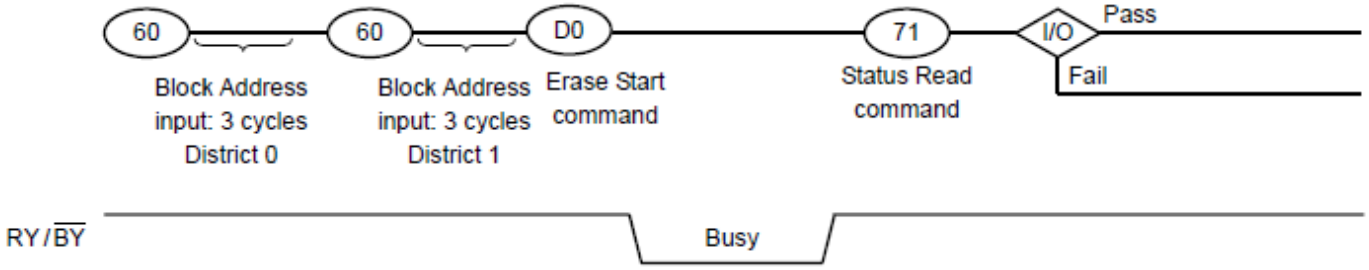
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE after the Erase Start command D0h which follows the Erase Setup command 60h. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



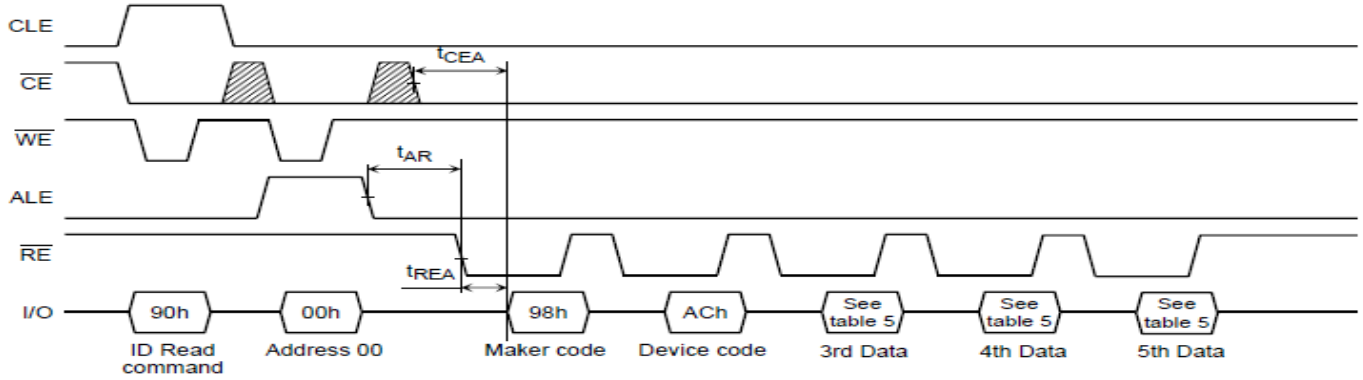
Multi Block Erase

The Multi Block Erase operation starts by selecting two block addresses before D0h command as in below diagram. The device automatically executes the Erase and Verify operations and the result can be monitored by checking the status by 71h status read command.



ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:



Code Table

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	0	1	0	1	1	0	0	ACh
3rd Data	Chip Number, Cell Type	1	0	0	1	0	0	0	0	90h
4th Data	Page Size, Block Size, I/O Width	0	0	1	0	0	1	1	0	26h
5th Data	Plane Number	0	1	1	1	0	1	1	0	76h

3rd Table

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Reserved		1	0	0	1				

4th Table

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Page Size (without redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (without redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
I/O Width	x8		0						
	x16		1						
Reserved		0				0	1		

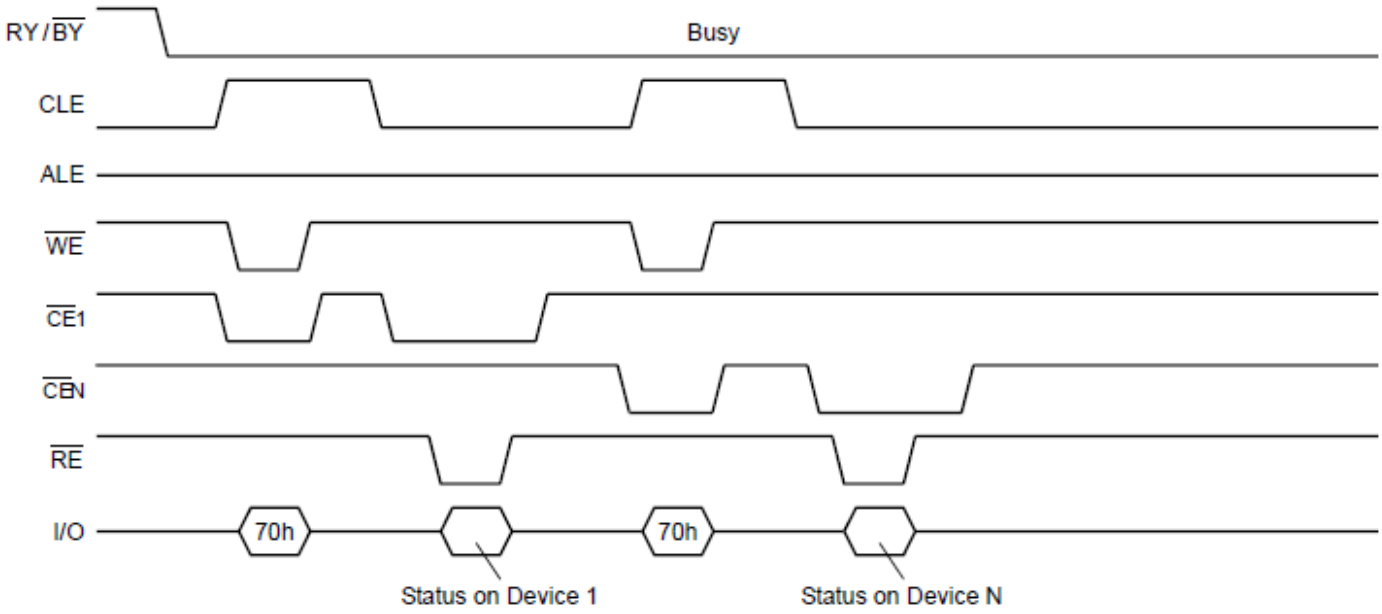
5th Table

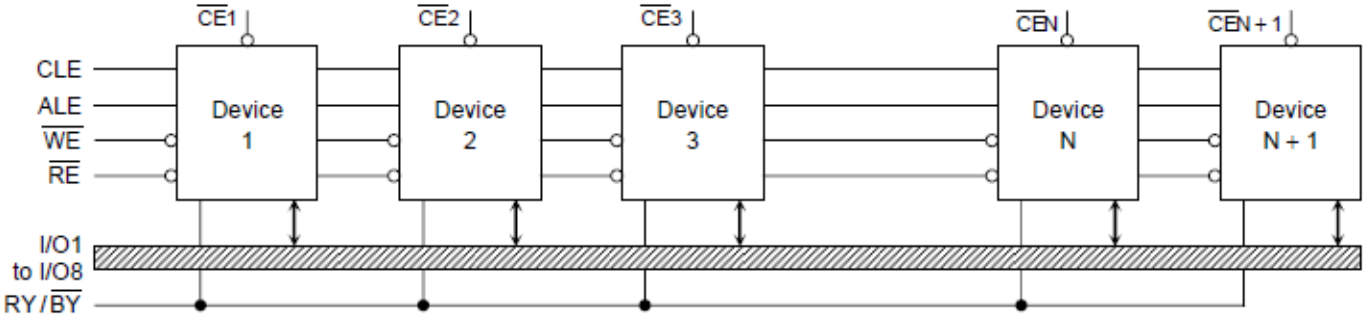
	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Plane Number	1Plane					0	0		
	2Plane					0	1		
	4Plane					1	0		
	8Plane					1	1		
Reserved		0	1	1	1			1	0

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using RE after a 70h command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

	Definition	Page Program Block Erase	Cache Program	Read Cache Read
IO0	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
IO1	Chip Status 2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
IO2	Not Used	0	0	0
IO3	Not Used	0	0	0
IO4	Not Used	0	0	0
IO5	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
IO6	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
IO7	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

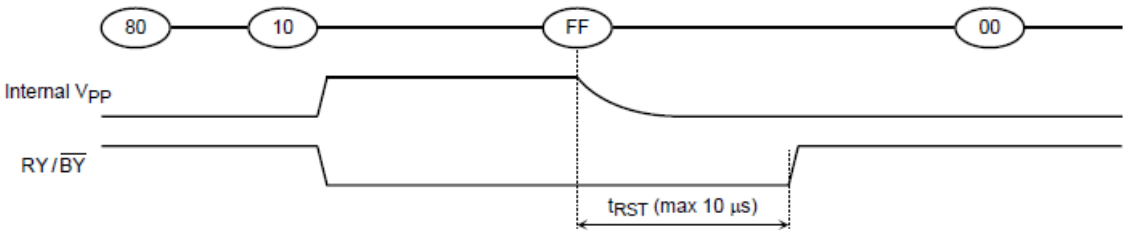




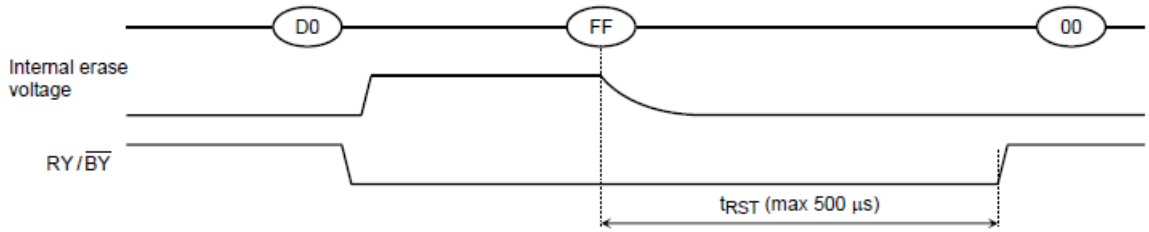
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state. Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input. The response to a FFh Reset command input during the various device operations is as follows:

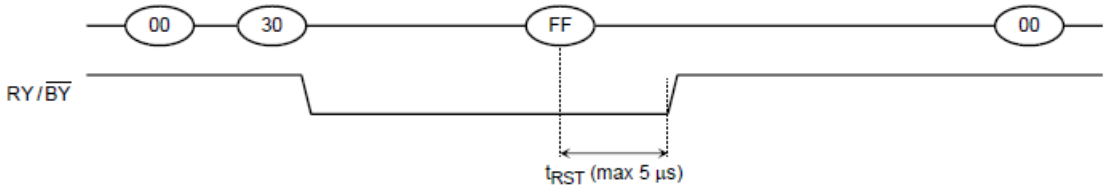
When a Reset (FFh) command is input during programming



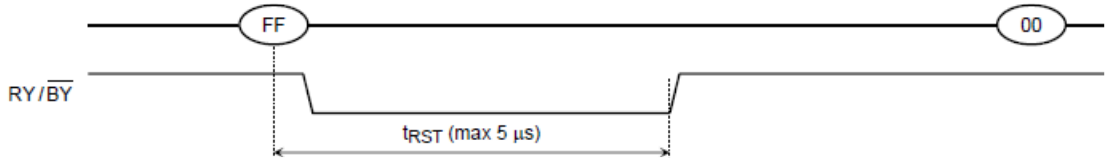
When a Reset (FFh) command is input during erasing



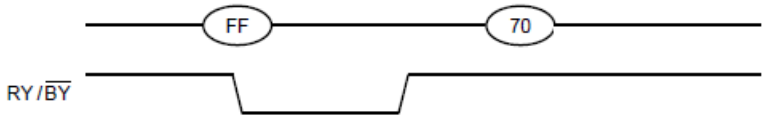
When a Reset (FFh) command is input during Read Operation



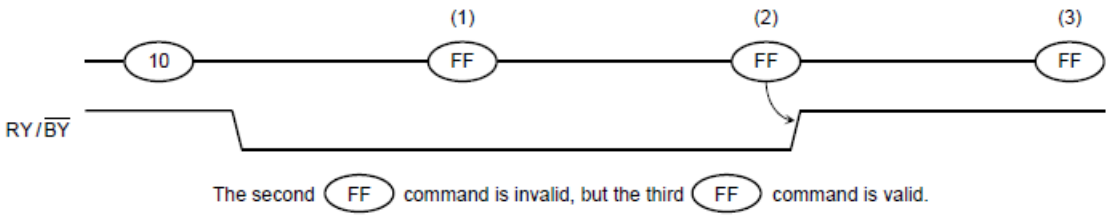
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	Vcc	-0.6 to +2.5	V
	V_{IN}	-0.6 to +2.5	
	$V_{I/O}$	-0.6 to Vcc+0.3(<2.5V)	
Power Dissipation	P_D	0.3	W
Soldering Temperature (10 s)	T_{SOLDER}	260	
Storage Temperature	T_{STG}	RT to +85	℃
Operating Temperature	T_{ORP}	RT to +85	℃

NOTE : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	–	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	–	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	2008	–	2048	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment. The specification for the minimum number of valid blocks is applicable over lifetime

The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	1.7	1.8	1.95	V
High Level Input Voltage	VIH	VCC x 0.8	—	VCC + 0.3	V
Low Level Input Voltage	VIL	-0.3	—	VCC x 0.2	V

DC CHARACTERISTICS (Ta = RT to 85℃, VCC = 1.7 to 1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	CE = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	CE = V_{CC} − 0.2 V, WP = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.1 mA	V_{CC} − 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/BY)	Output current of RY/BY pin	V_{OL} = 0.2 V	—	4	—	mA

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode. When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE,ALE,/CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

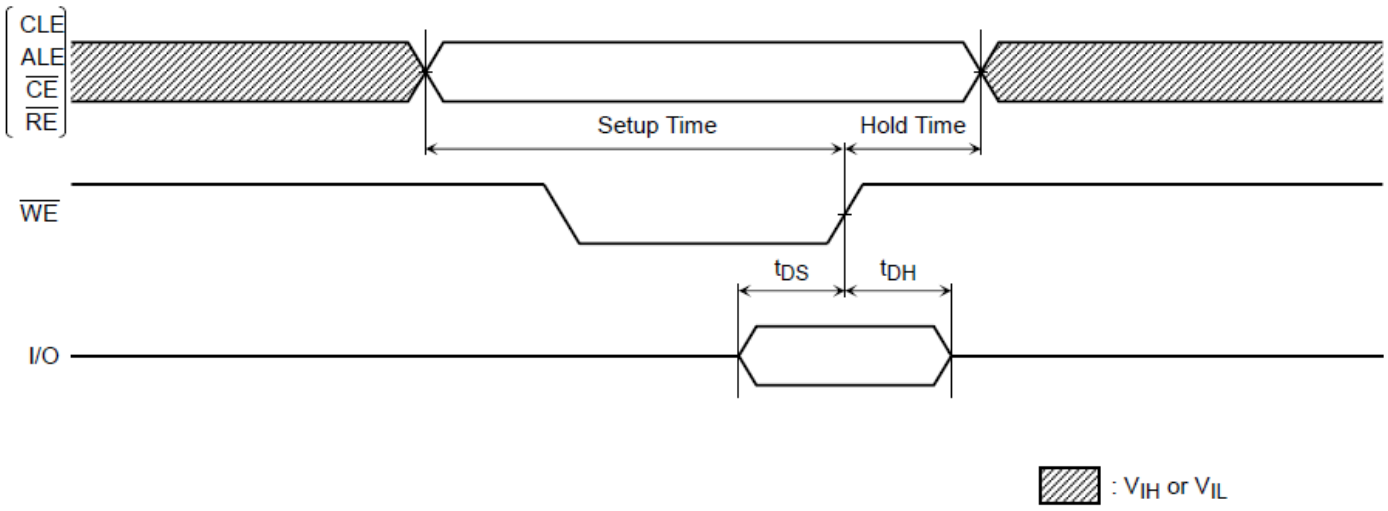
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = RT to 85℃, V_{CC} = 1.7 to 1.95V)

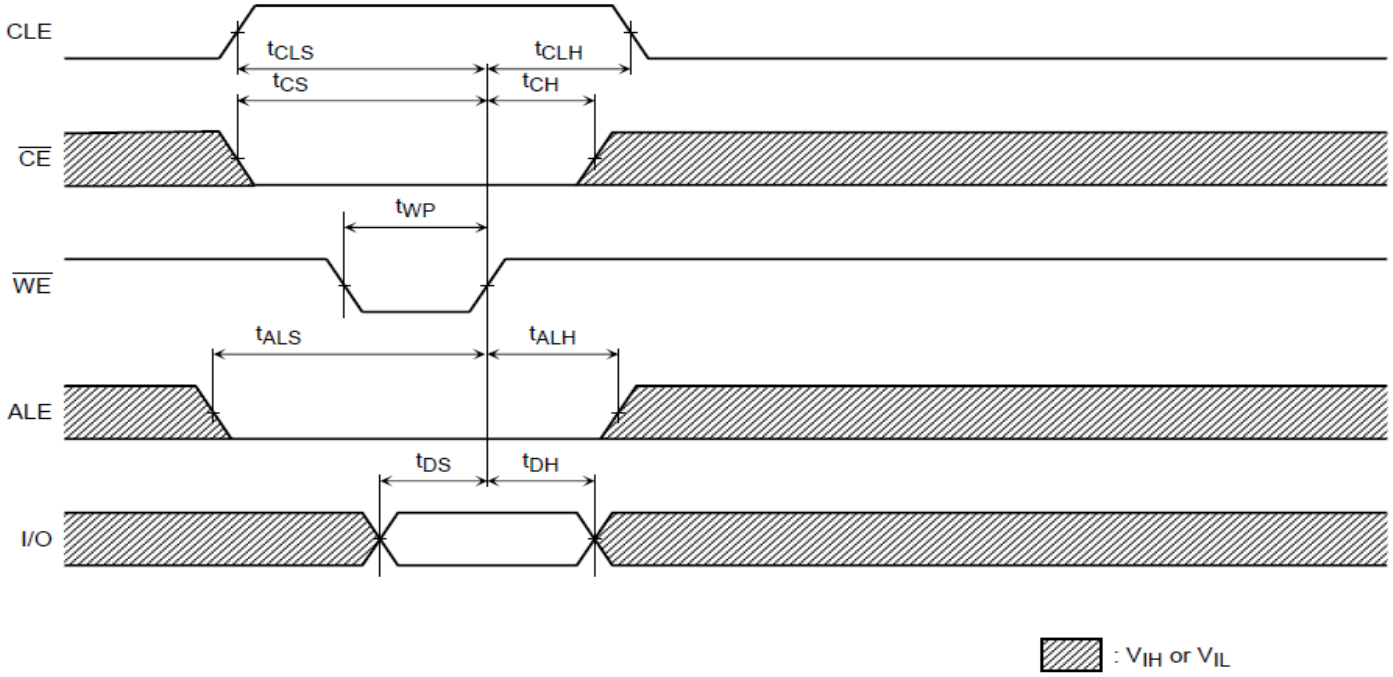
SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	-	ns
t_{CLH}	CLE Hold Time	5	-	ns
t_{CS}	CE Setup Time	20	-	ns
t_{CH}	CE Hold Time	5	-	ns
t_{WP}	Write Pulse Width	12	-	ns
t_{ALS}	ALE Setup Time	12	-	ns
t_{ALH}	ALE Hold Time	5	-	ns
t_{DS}	Data Setup Time	12	-	ns
t_{DH}	Data Hold Time	5	-	ns
t_{WC}	Write Cycle Time	25	-	ns
t_{WH}	WE High Hold Time	10	-	ns
t_{WW}	WP High to WE Low	100	-	ns
t_{RR}	Ready to RE Falling Edge	20	-	ns
t_{RW}	Ready to WE Falling Edge	20	-	ns
t_{RP}	Read Pulse Width	12	-	ns
t_{RC}	Read Cycle Time	25	-	ns
t_{REA}	RE Access Time	-	20	ns
tCEA	CE Access Time	-	25	ns
t_{CLR}	CLE Low to RE Low	10	-	ns
t_{AR}	ALE Low to RE Low	10	-	ns
t_{RHOH}	RE High to Output Hold Time	25	-	ns
t_{RLOH}	RE Low to Output Hold Time	5	-	ns
t_{RHZ}	RE High to Output High Impedance	-	60	ns
t_{CHZ}	CE High to Output High Impedance	-	20	ns
t_{CSD}	CE High to ALE or CLE Don't Care	0	-	ns
t_{REH}	RE High Hold Time	10	-	ns
t_{IR}	Output-High-impedance-to-RE Falling Edge	0	-	ns
t_{RHW}	RE High to WE Low	30	-	ns
t_{WHC}	WE High to CE Low	30	-	ns
t_{WHR}	WE High to RE Low	60	-	ns
t_{R}	Memory Cell Array to Starting Address	-	25	µs
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	-	25	µs
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	-	30	µs
t_{WB}	WE High to Busy	-	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	-	5/5/10/500	µs

Timing Diagram

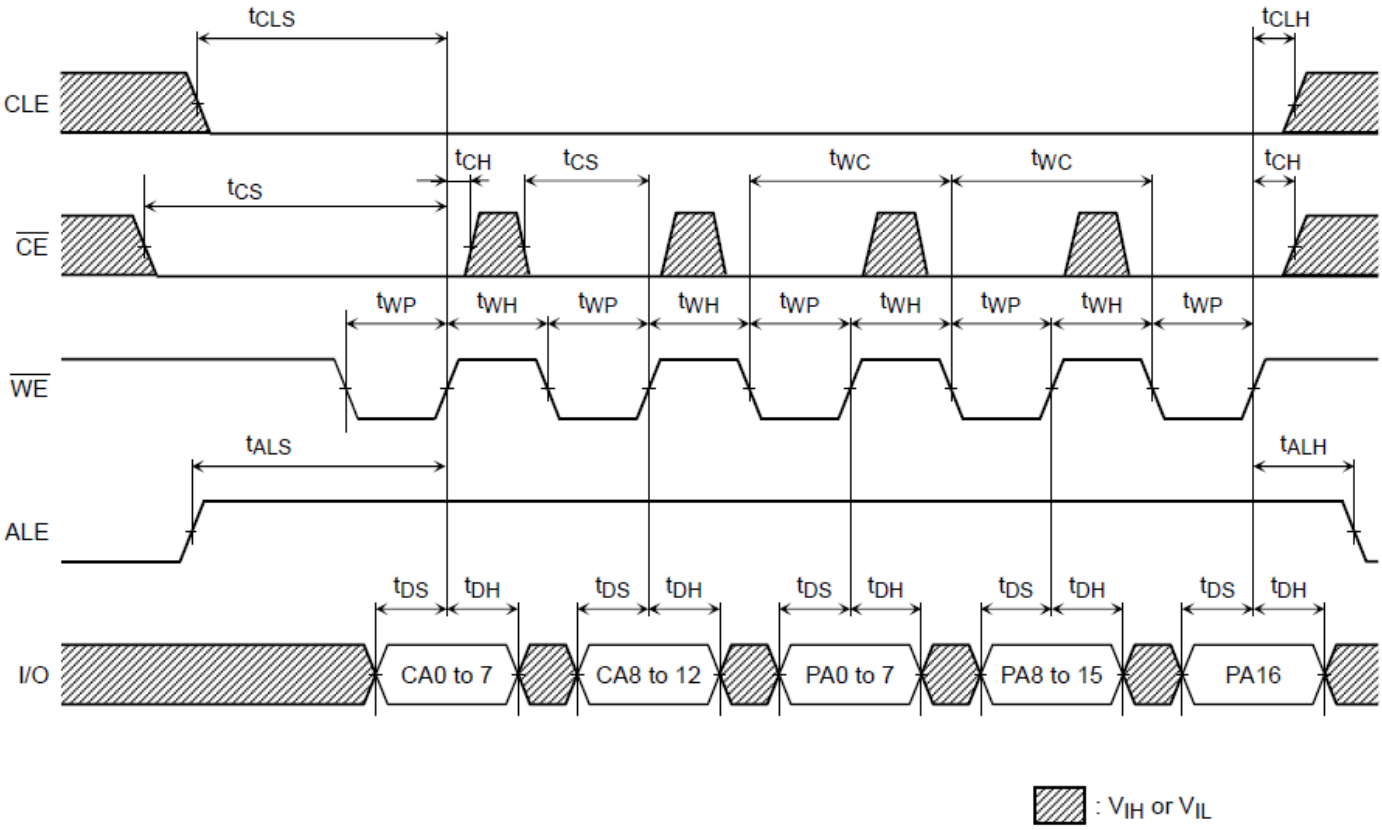
Latch Timing Diagram for Command/Address/Data



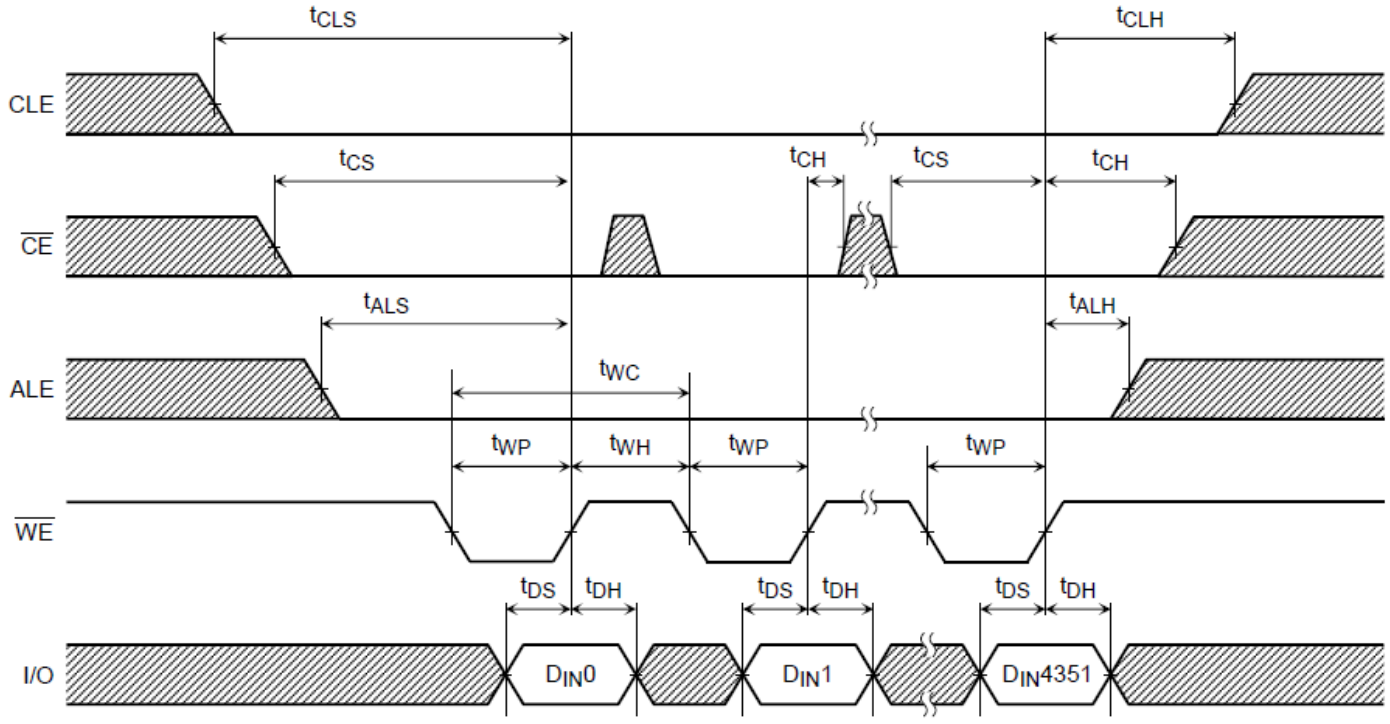
Command Input Cycle Timing Diagram



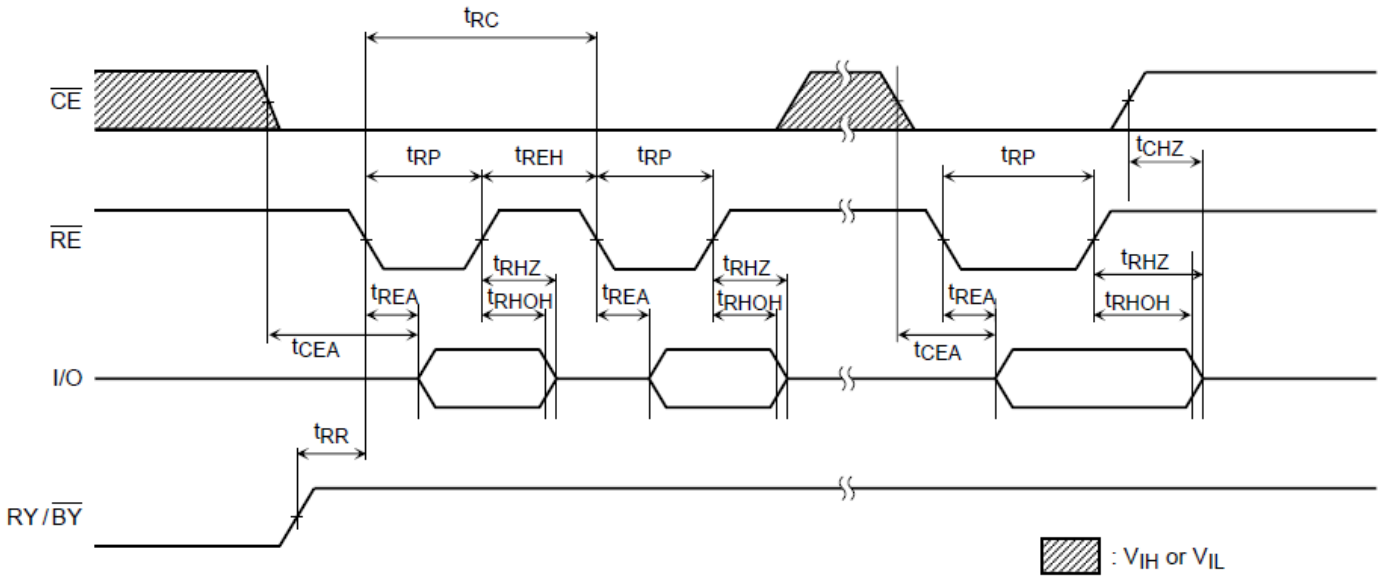
Address Input Cycle Timing Diagram



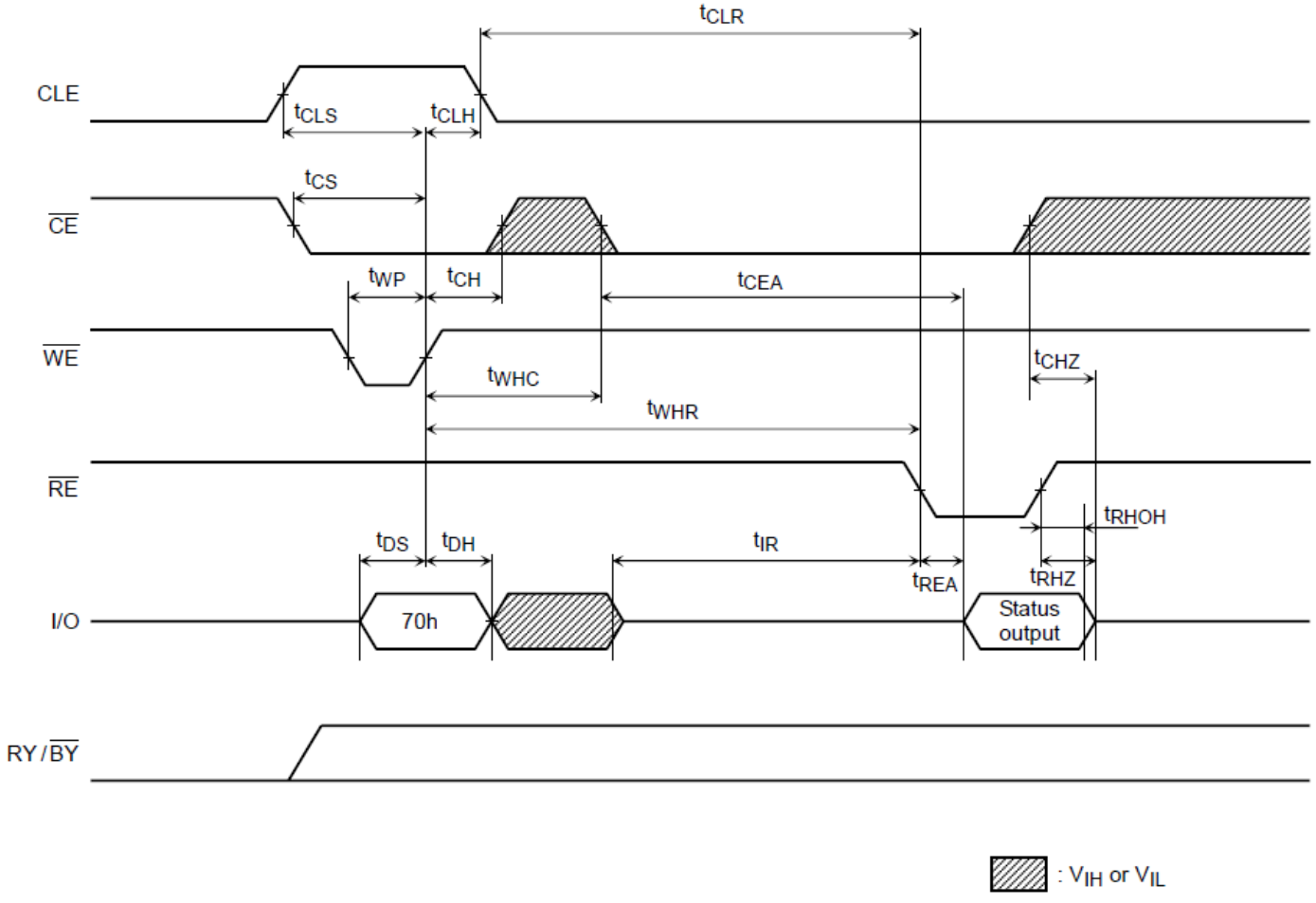
Data Input Cycle Timing Diagram



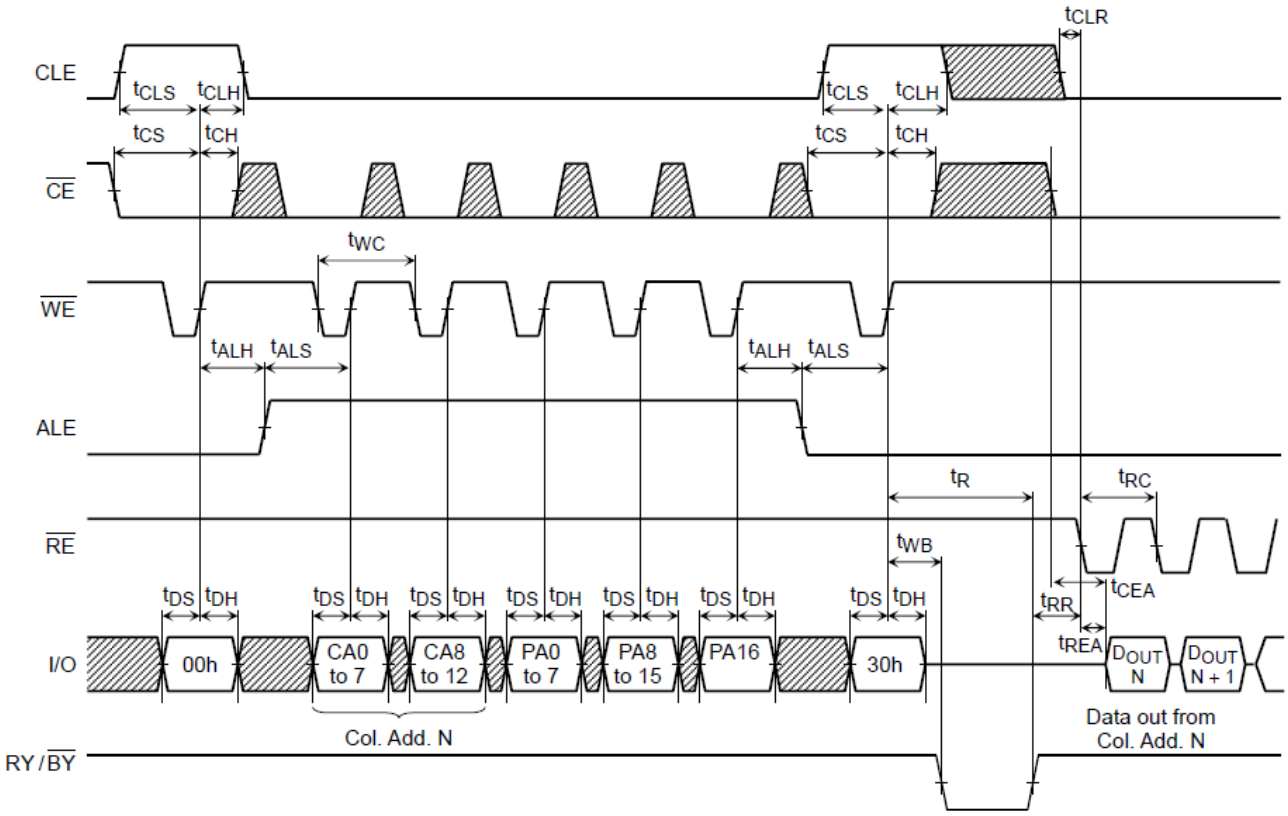
Serial Read Cycle Timing Diagram



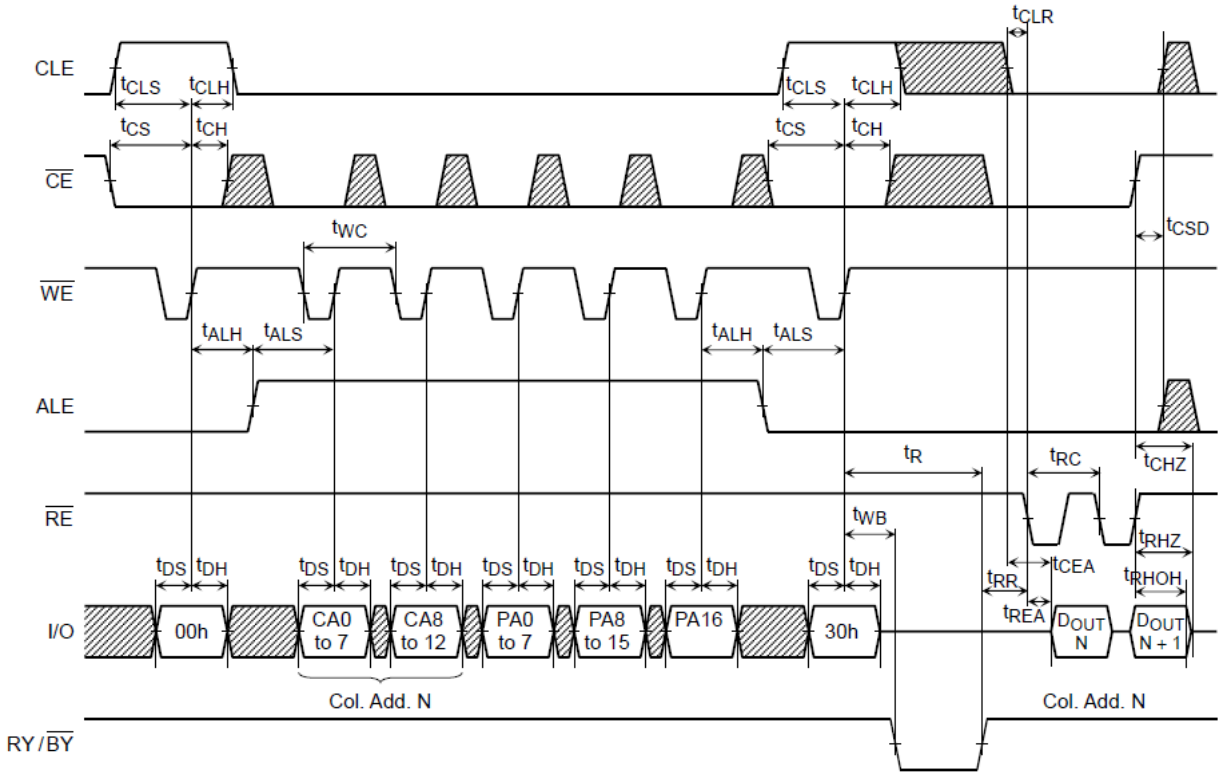
Status Read Cycle Timing Diagram



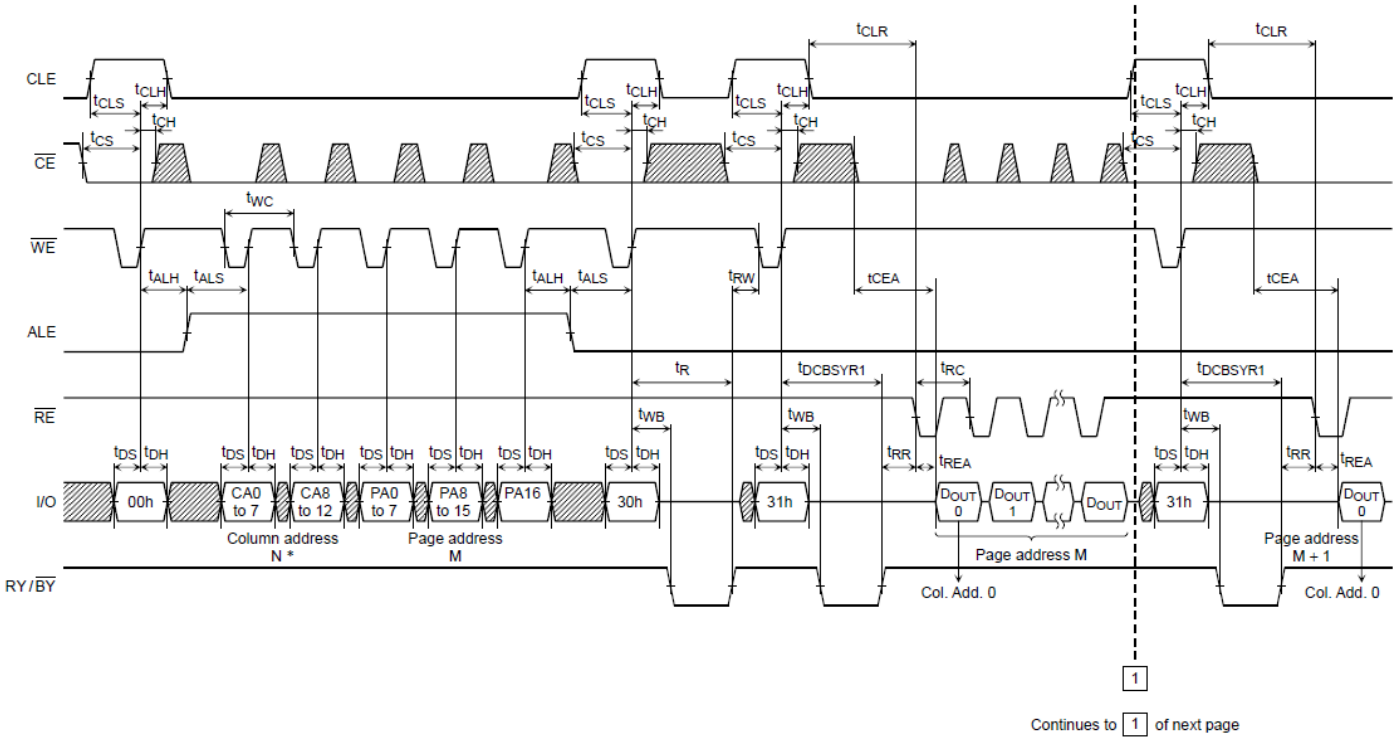
Read Cycle Timing Diagram



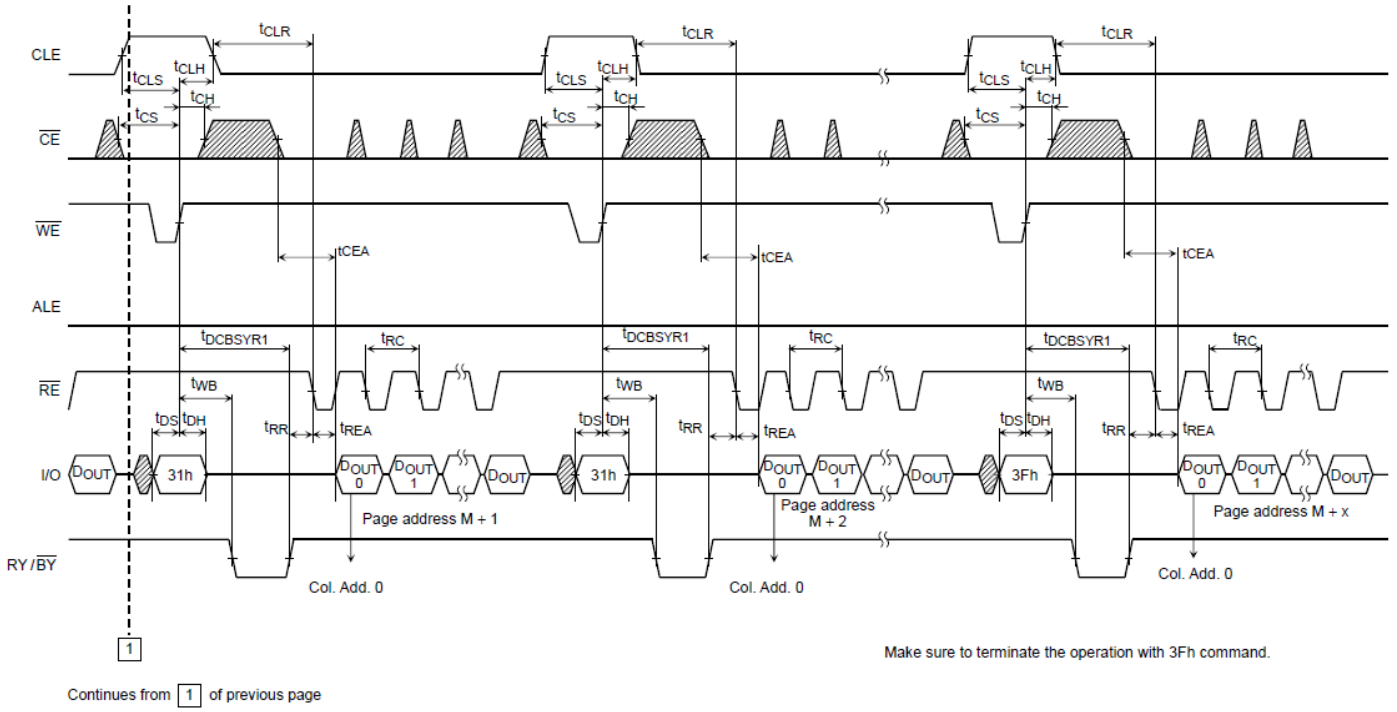
Read Cycle Timing Diagram: When Interrupted by CE



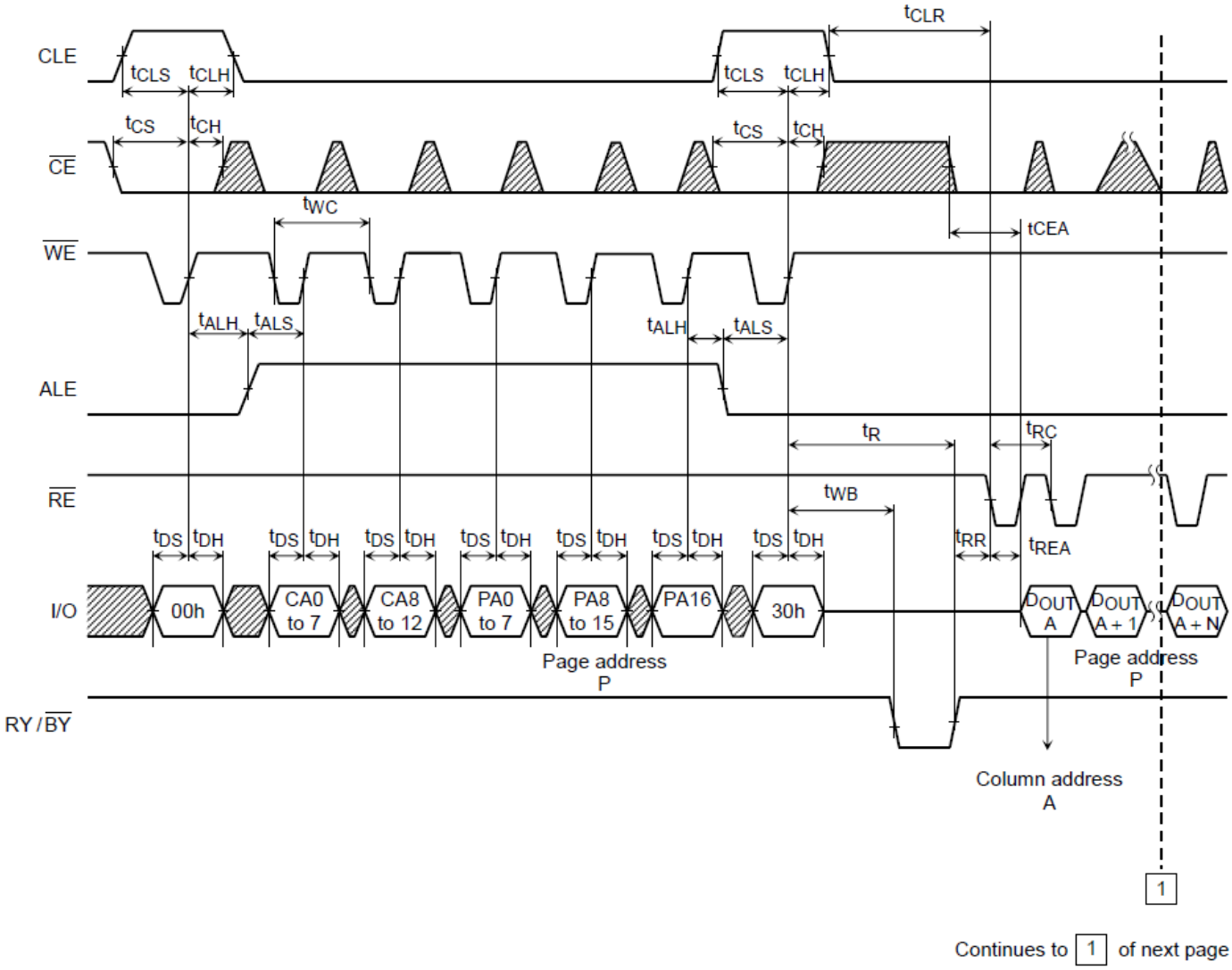
Read Cycle with Data Cache Timing Diagram (1/2)



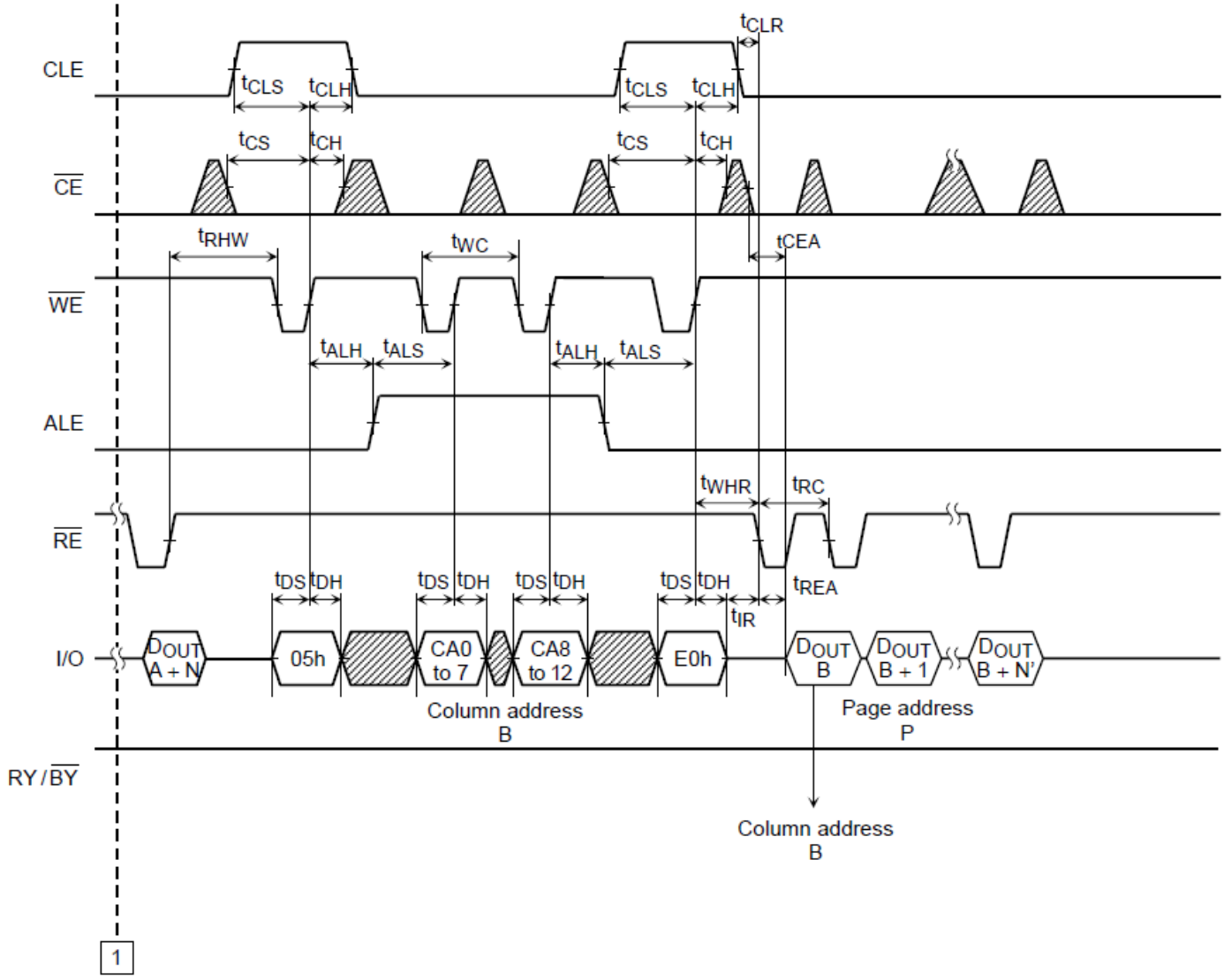
Read Cycle with Data Cache Timing Diagram (2/2)



Column Address Change in Read Cycle Timing Diagram (1/2)



Column Address Change in Read Cycle Timing Diagram (2/2)



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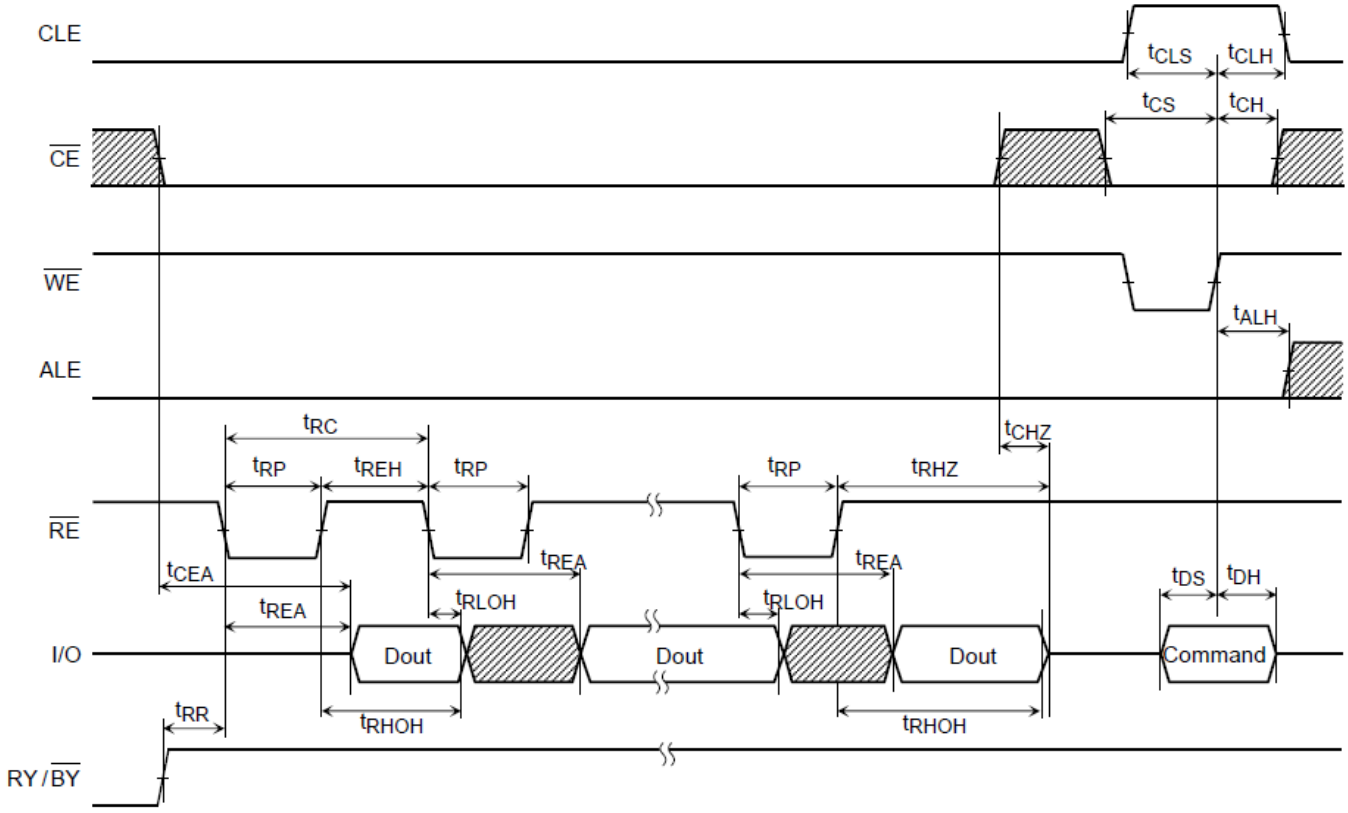
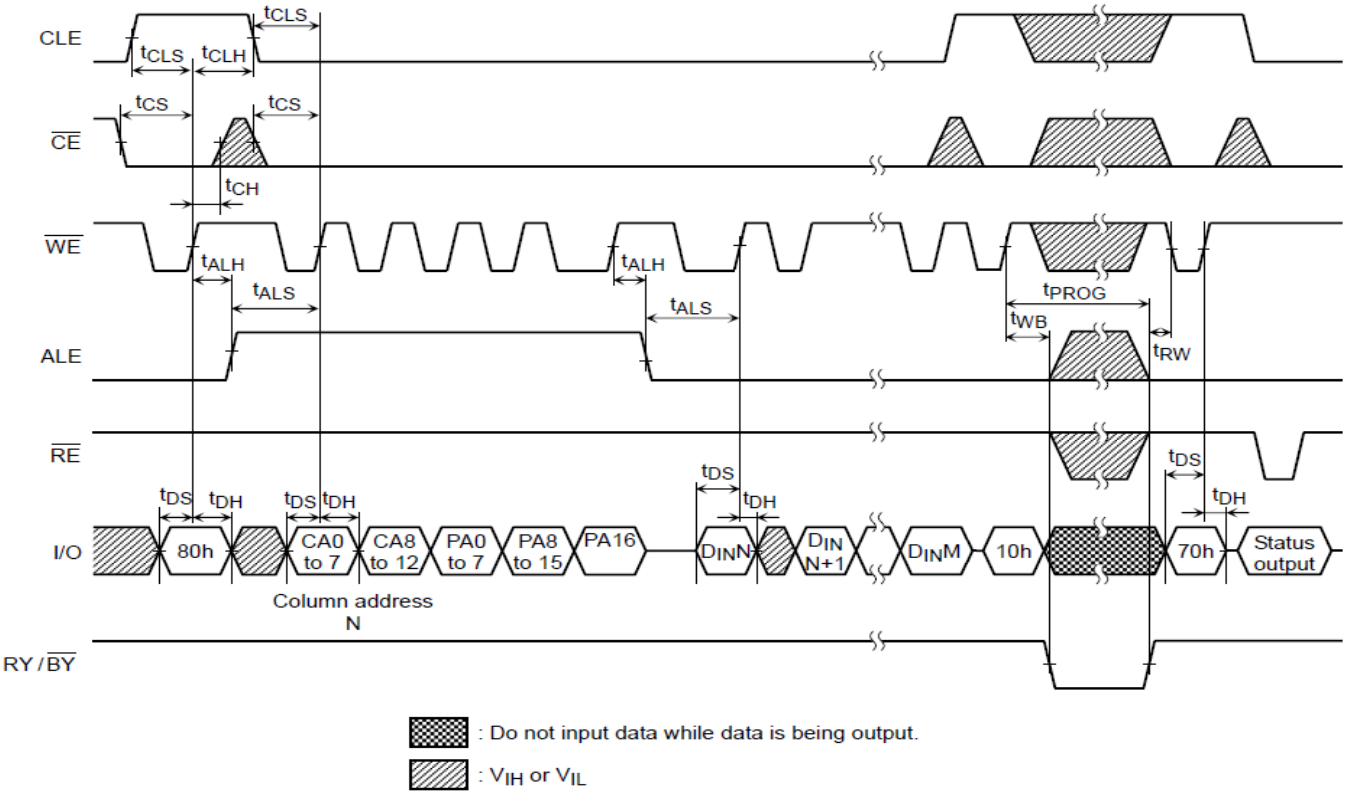
Data Output Timing Diagram



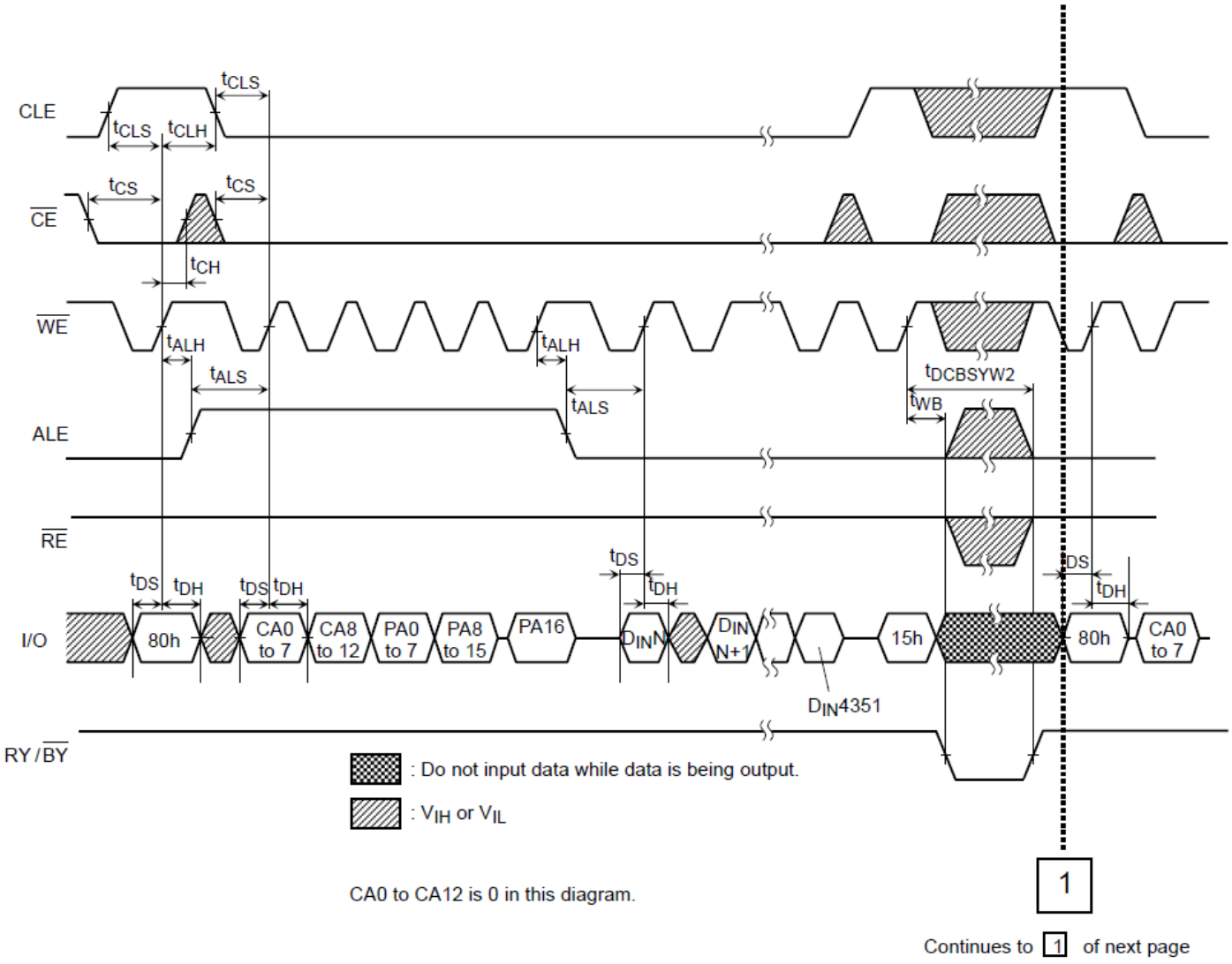
Auto-Program Operation Timing Diagram



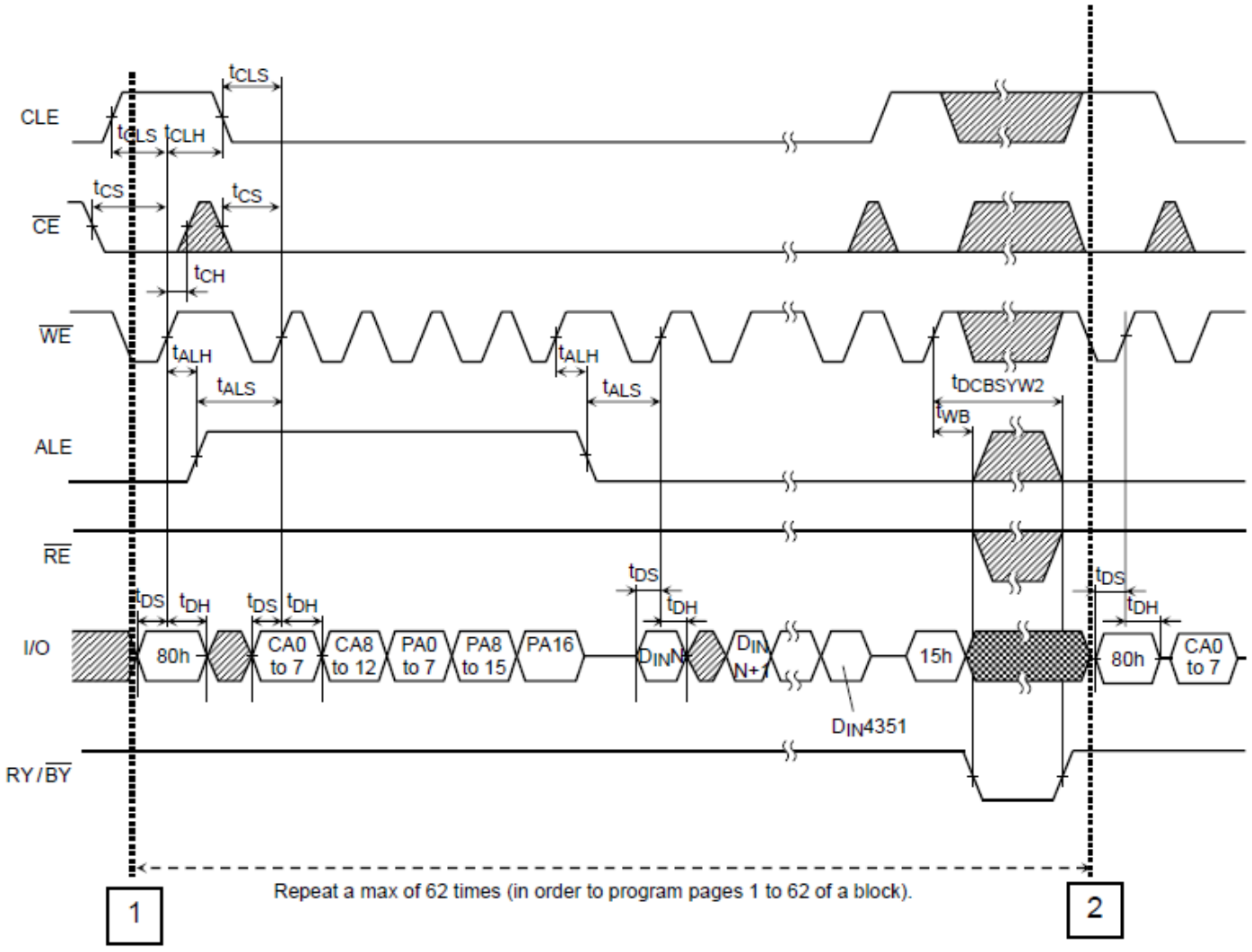
: Do not input data while data is being output.

: V_{IH} or V_{IL}

Auto-Program Operation with Data Cache Timing Diagram (1/3)



Auto-Program Operation with Data Cache Timing Diagram (2/3)



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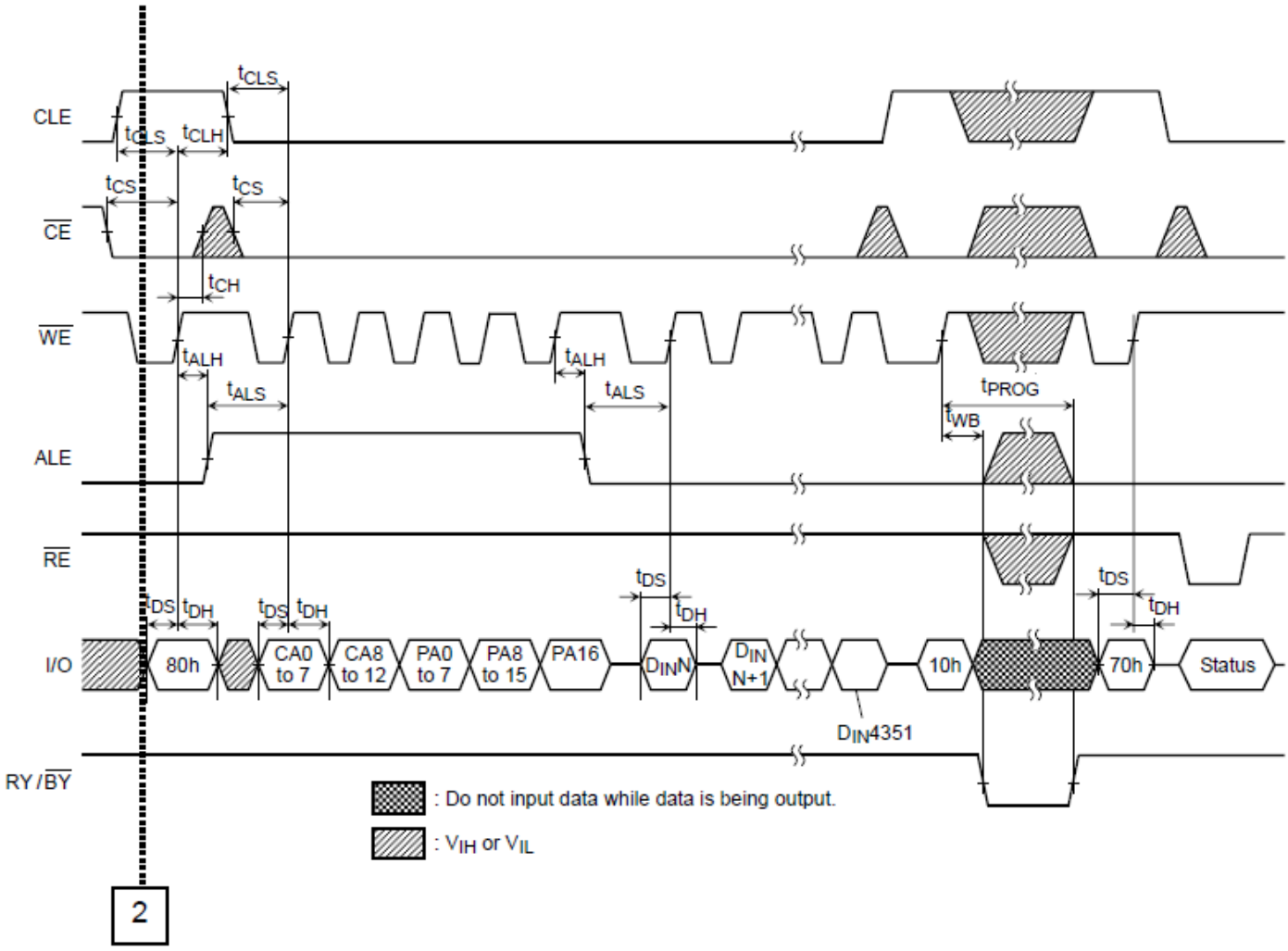
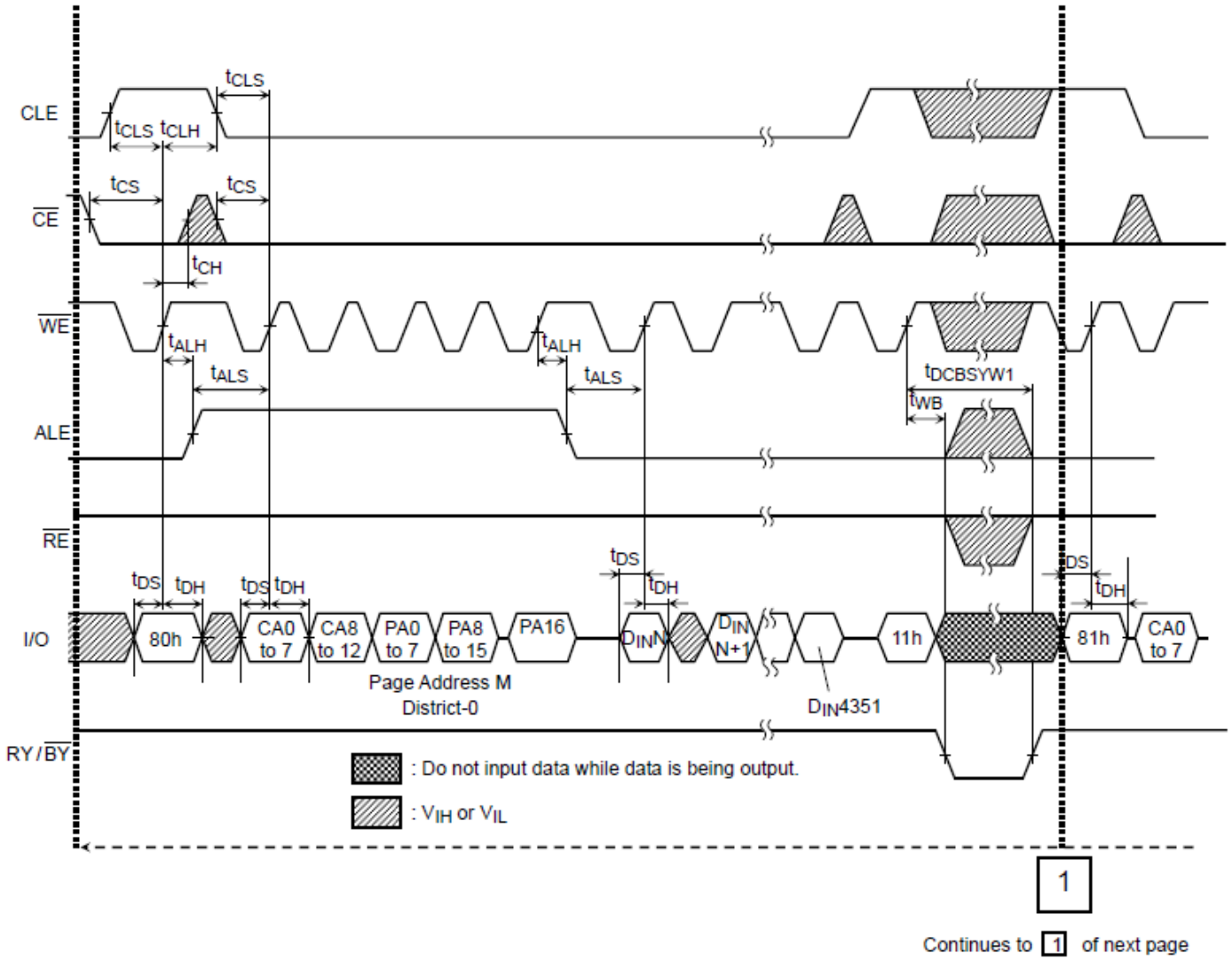
: Do not input data while data is being output.

: V_{IH} or V_{IL}

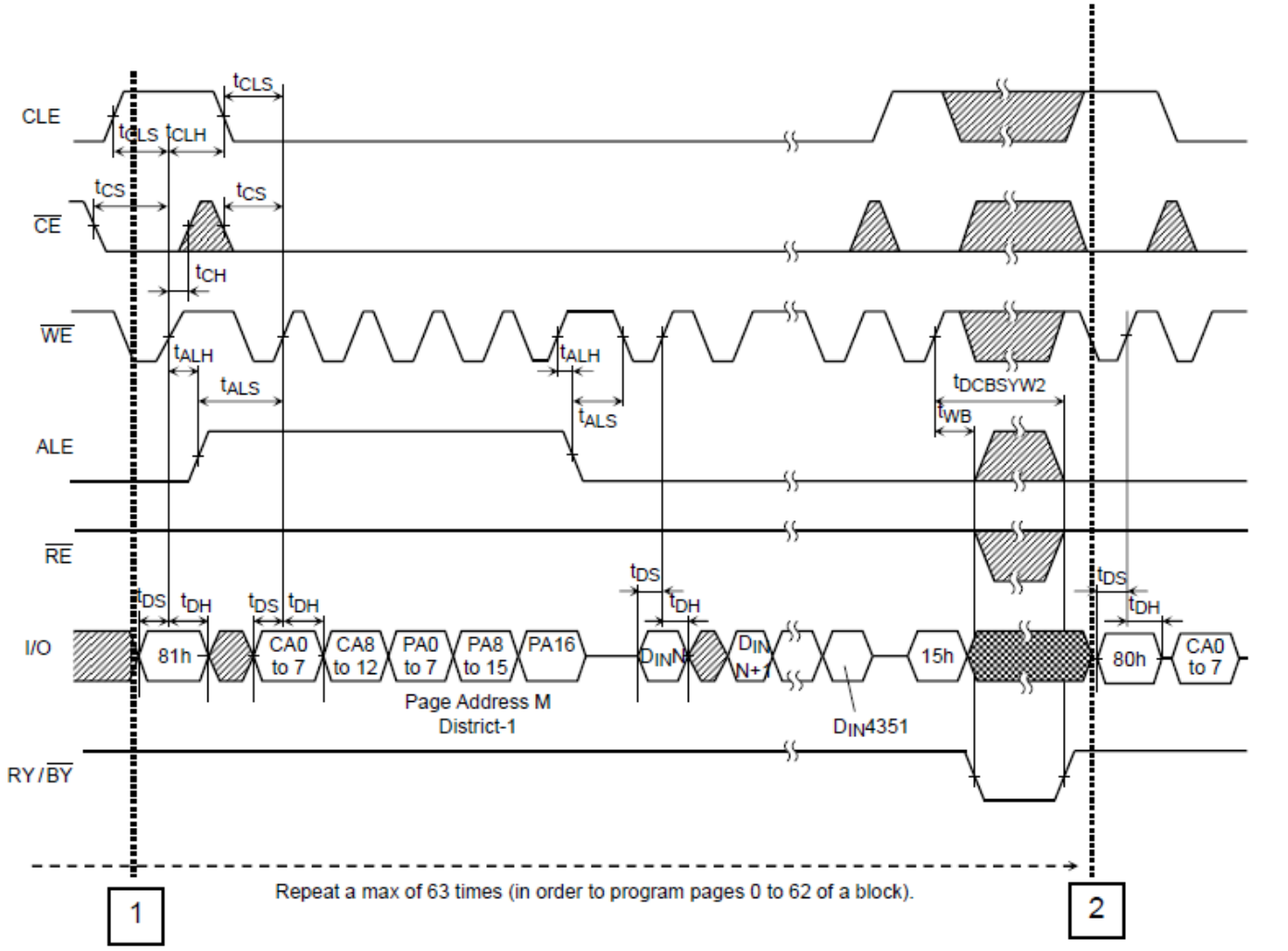
Auto-Program Operation with Data Cache Timing Diagram (3/3)



Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



Multi-Page Program Operation with Data Cache Timing Diagram (2/4)



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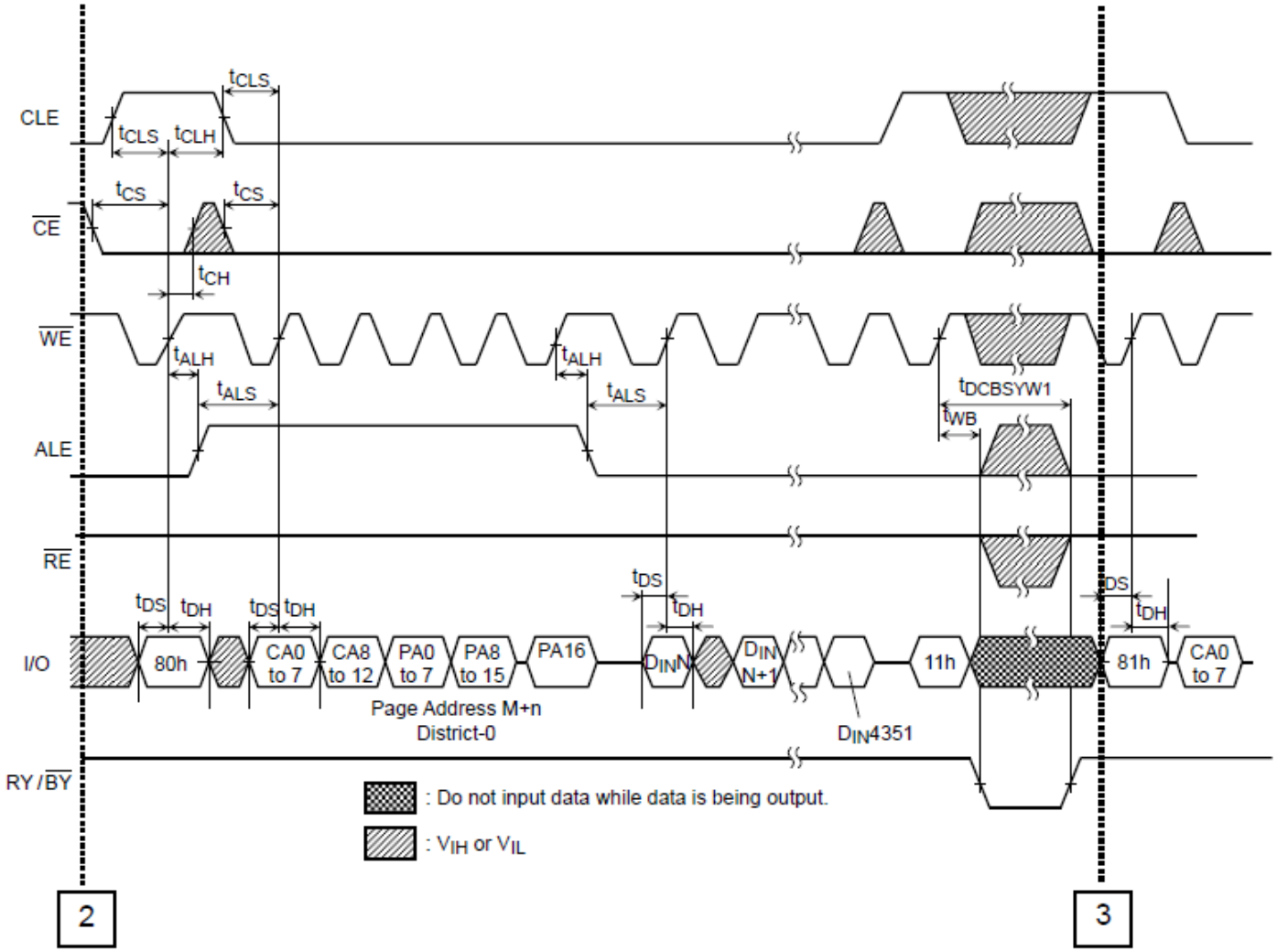
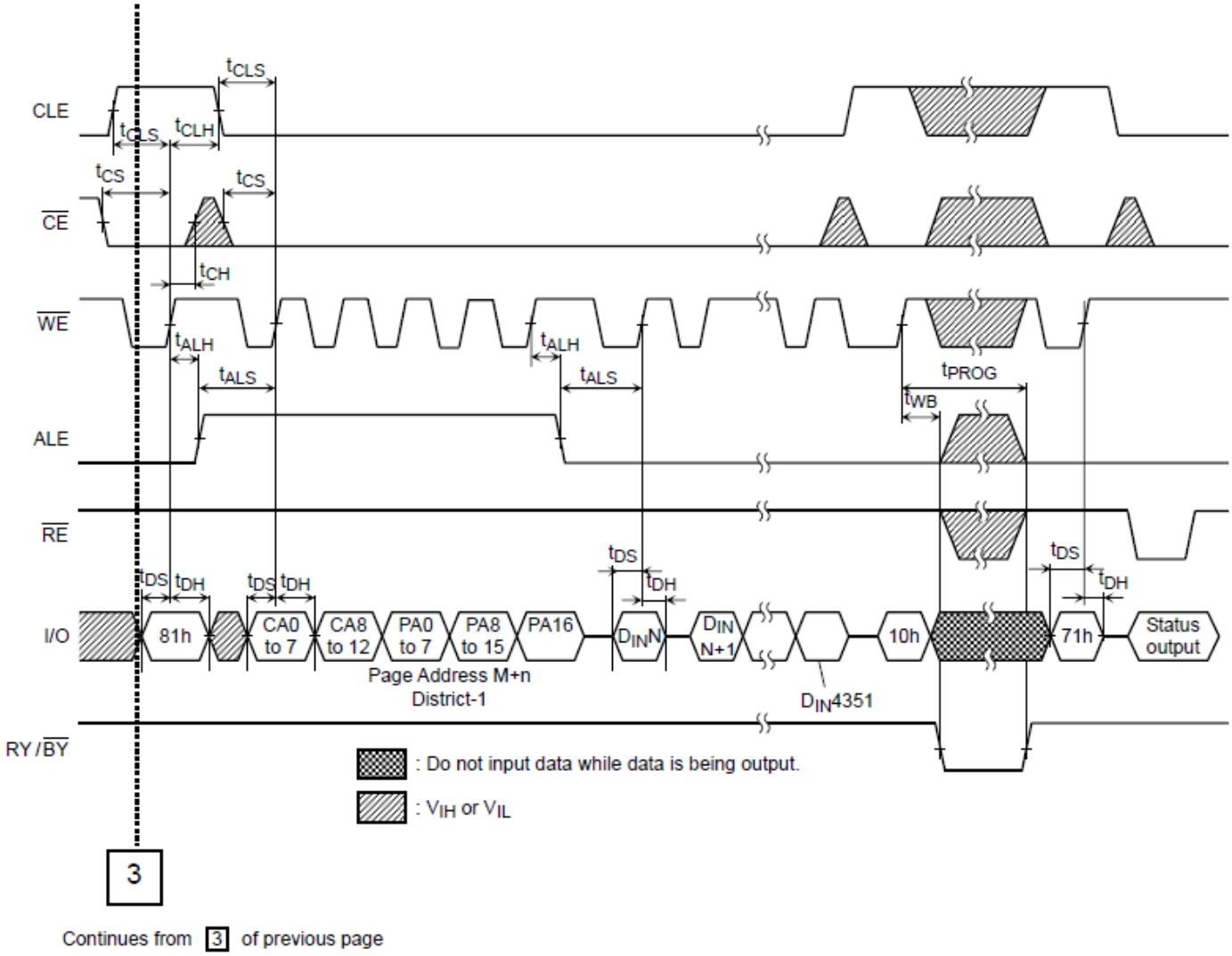
: Do not input data while data is being output.

: V_{IH} or V_{IL}

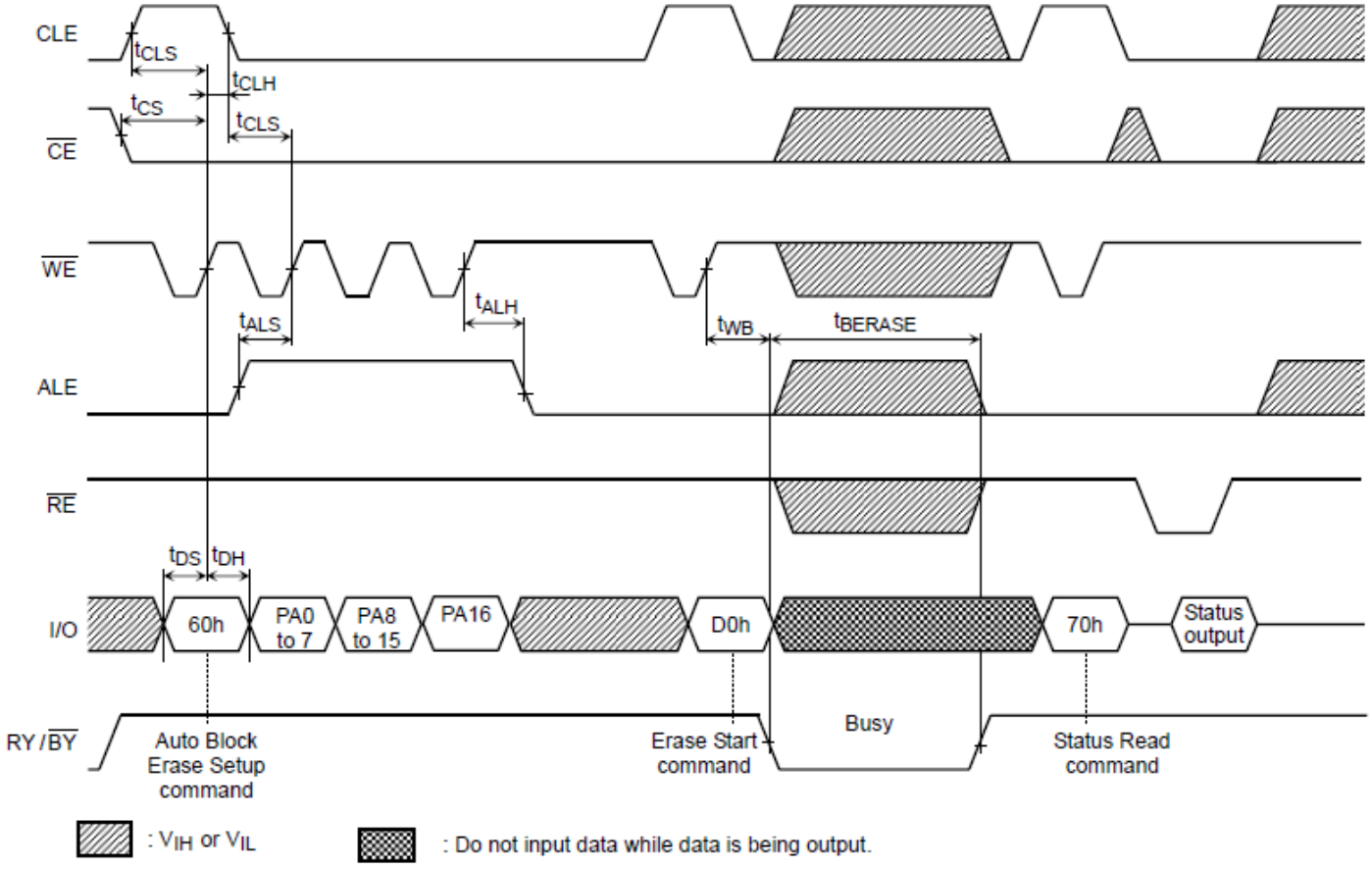
Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



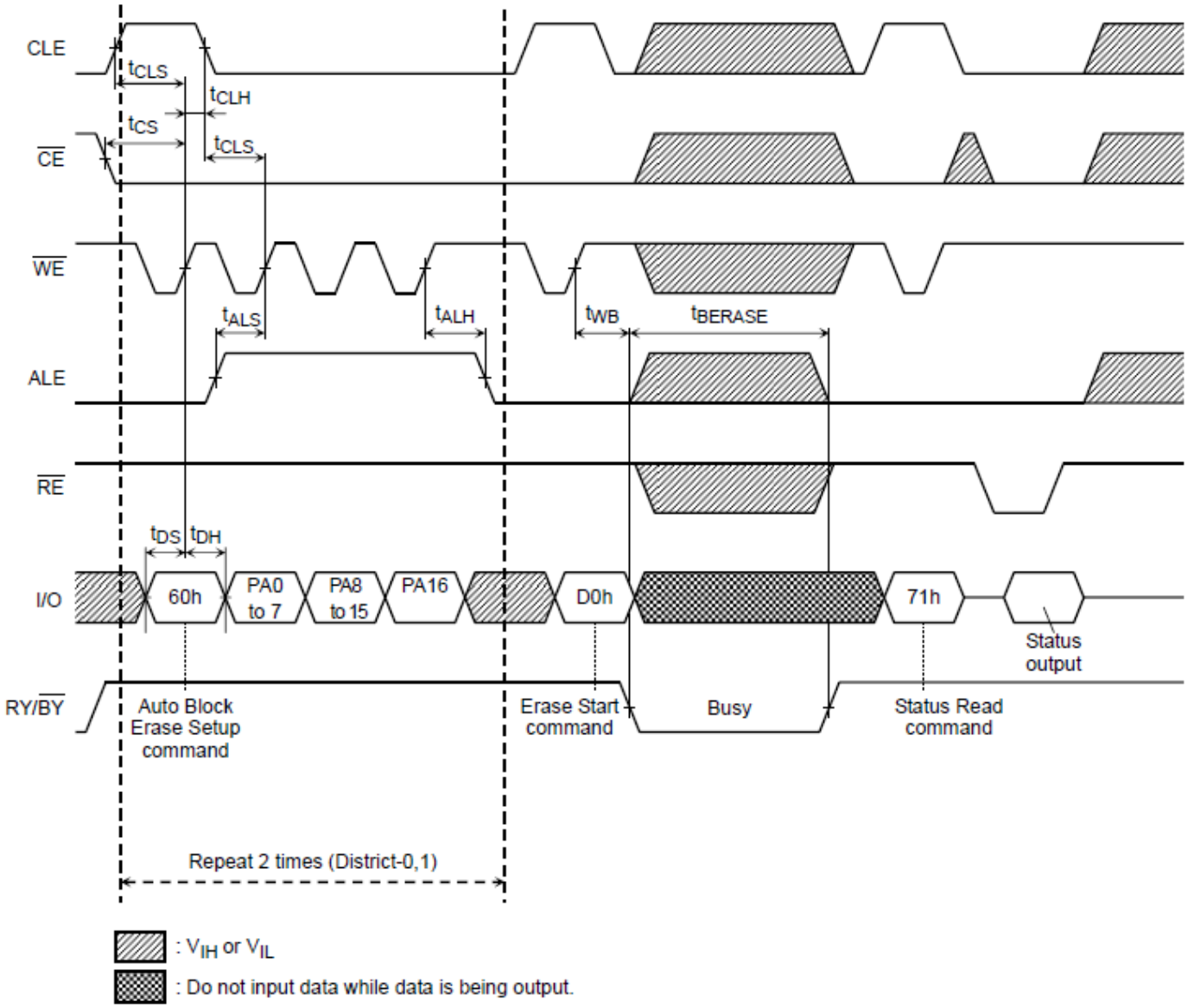
Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



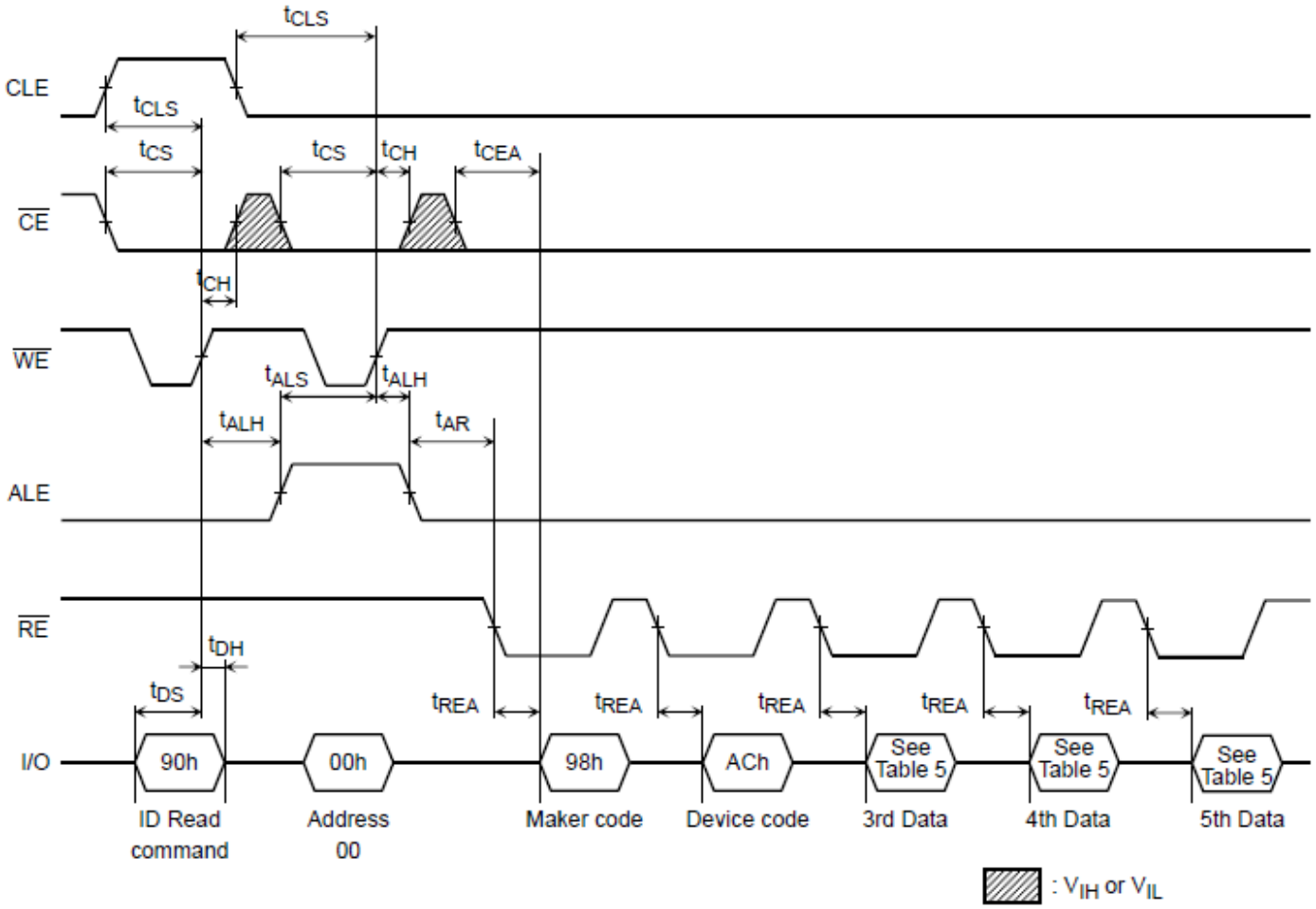
Auto Block Erase Timing Diagram



Multi Block Erase Timing Diagram



ID Read Operation Timing Diagram



AC TEST CONDITIONS

PARAMETER	CONDITION
	V_{CC}: 1.7 to 1.95V
Input level	0V to Vcc
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	C_L (30 pF) + 1 TTL

PROGRAMMING AND ERASING CHARACTERISTICS (Ta = RT to 85℃, VCC = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	-	300	700	µs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	-	0.5	1	µs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	-	-	700	µs	(2)
N	Number of Partial Program Cycles in the Same Page	-	-	4		(1)
t_{BERASE}	Block Erasing Time	-	3.5	10	ms	

(1) Refer to Application Note (12) toward the end of this document.

(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

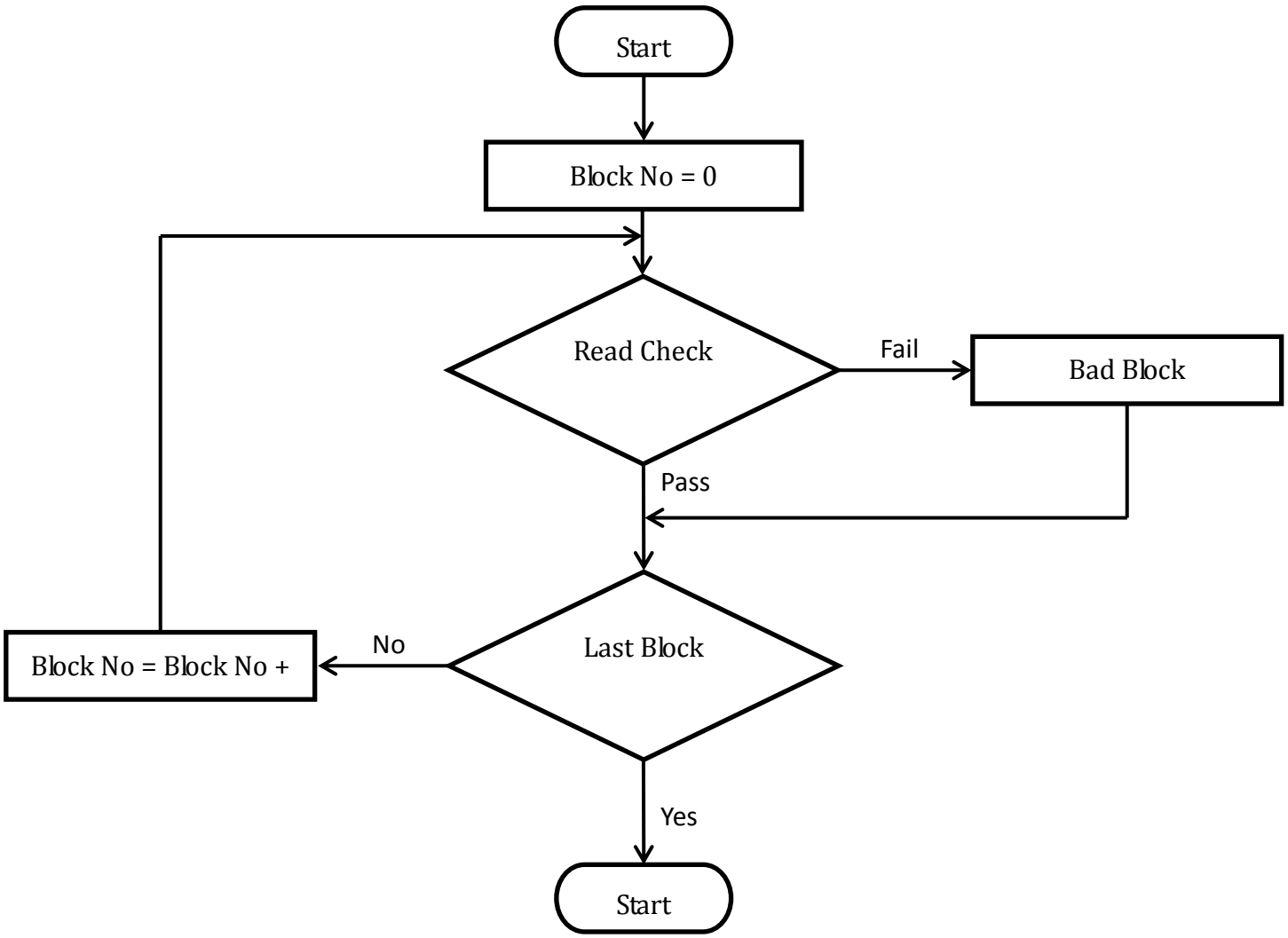
Invalid Blocks (Bad Blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized: Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system. A bad block does not affect the performance of good blocks because it is isolated from the bit line by select gates.

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages. Please read one column of any page in each block. If the data of the column is 00(Hex), define the block as a bad block.



Reliability Guidance

The reliability guidance is intended to notify some guidance related to using NAND flash with 8bit ECC for each 512bytes. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

4Gb LP DDR2 SDRAM(128Mb x32)

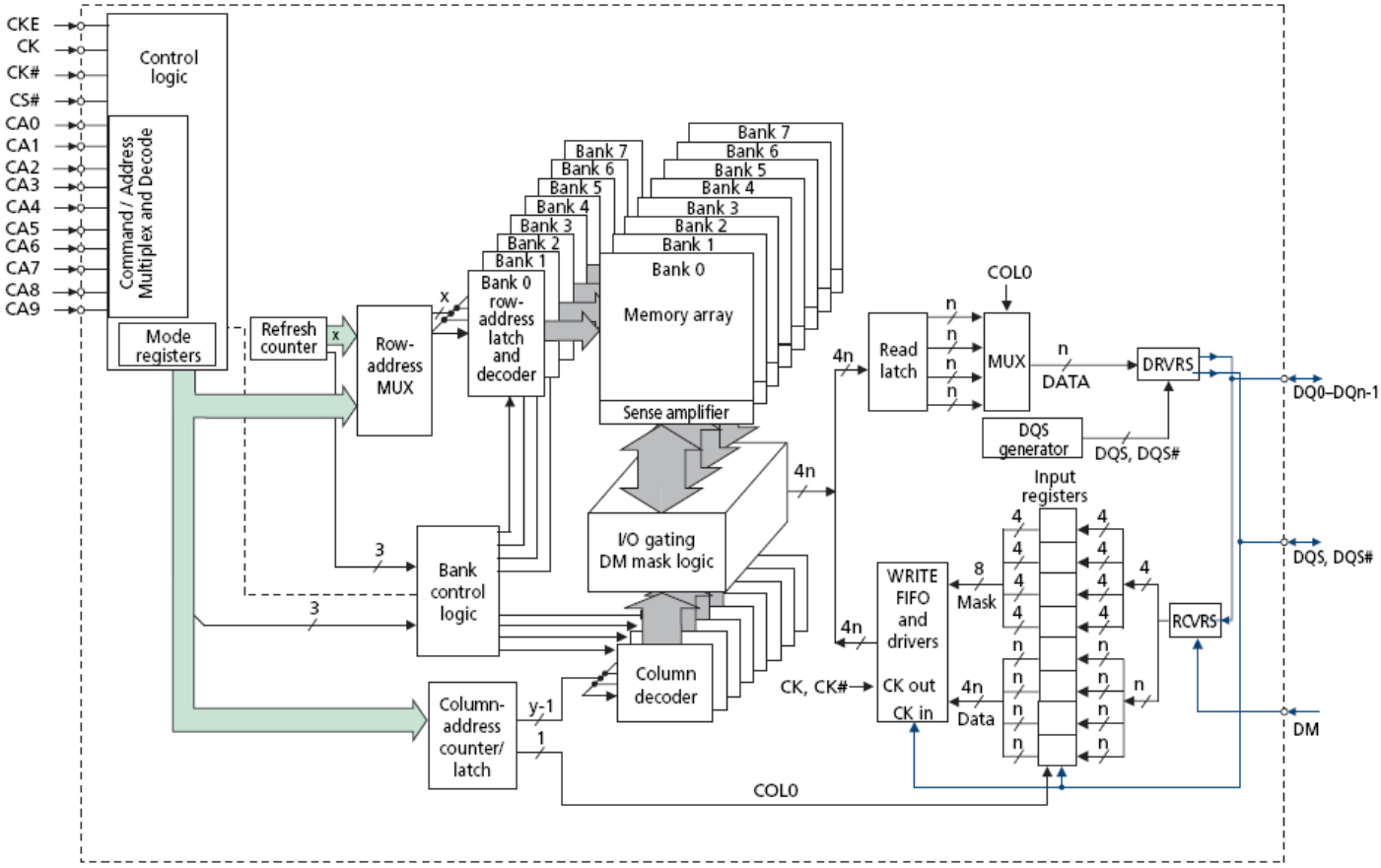
Description

The 4Gb Mobile LPDDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296 bits. The device is internally configured as an eight-bank DRAM. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1,024 columns by 32 bits.

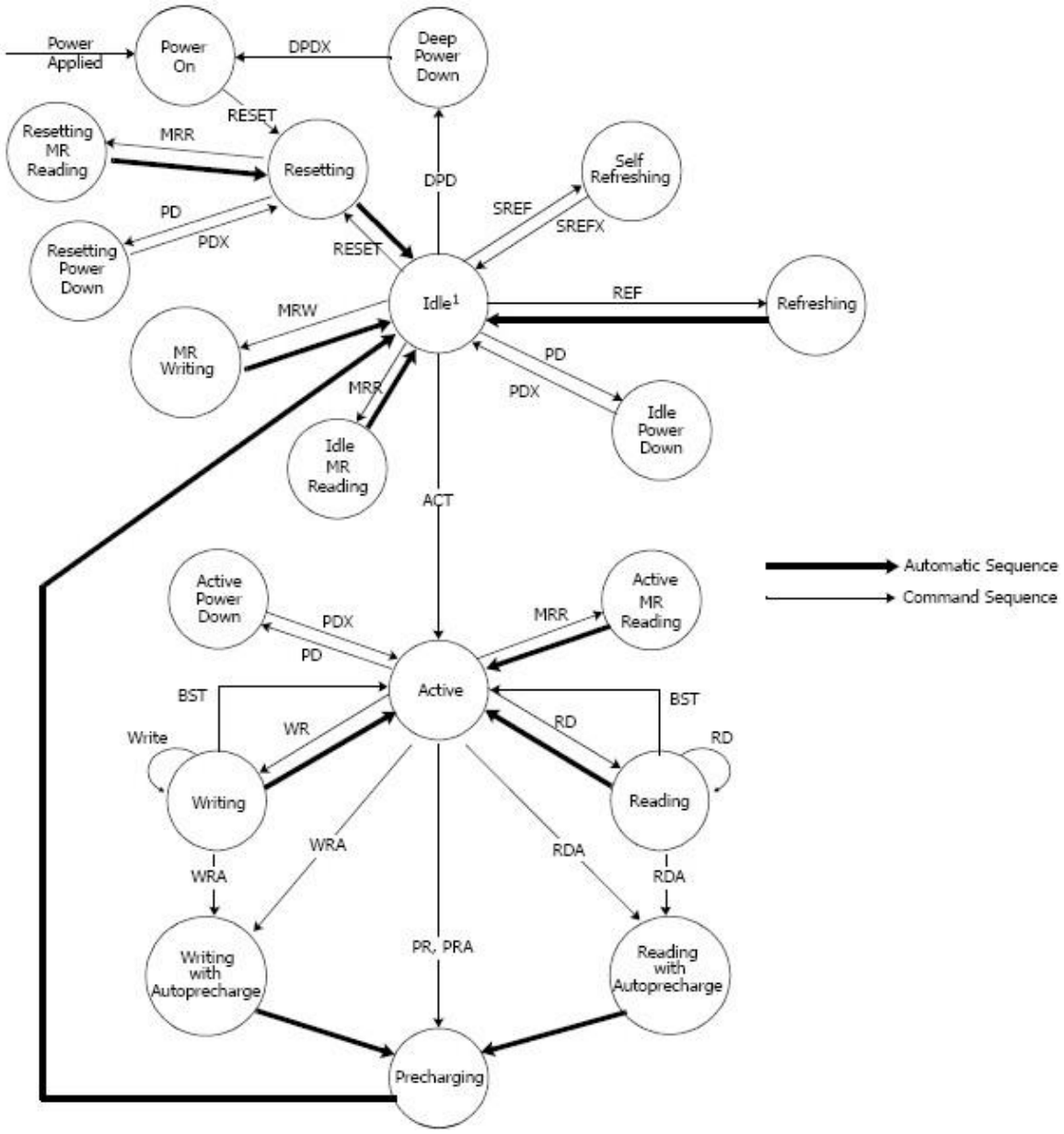
The device uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

To achieve high-speed operation, the device uses the double data rate architecture and adopt 4n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the device effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the device are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Functional Block Diagram



Simplified State Diagram

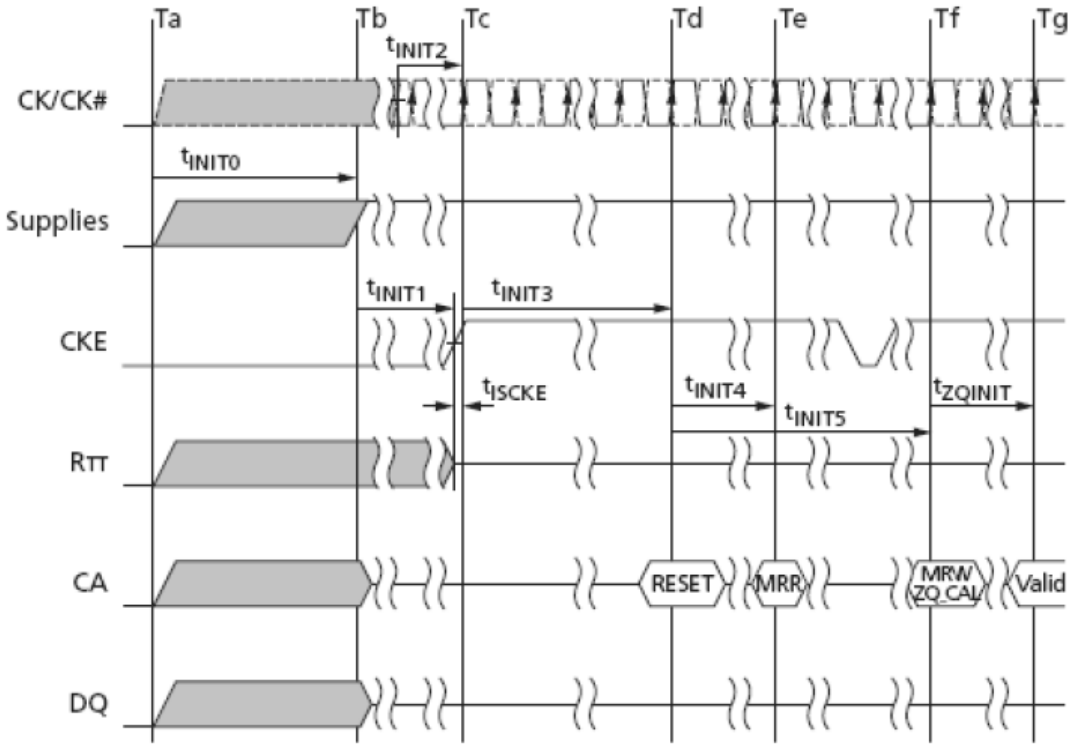


Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	PD	Enter Power Down	REF	Refresh
RD(A)	Read (w/ Autoprecharge)	PDX	Exit Power Down	SREF	Enter self refresh
WR(A)	Write (w/ Autoprecharge)	DPD	Enter Deep Power Down	SREFX	Exit self refresh
PR(A)	Precharge (All)	DPDX	Exit Deep Power Down		
MRW	Mode Register Write	BST	Burst Terminate		
MRR	Mode Register Read	RESET	Reset is achieved through MRW command		

Notes: For LPDDR2 SDRAM in the idle state, all banks are precharged.

Power-Up, Initialization and Power-Off

LPDDR2 devices must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.



Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, these steps are mandatory.

1. Voltage Ramp: While applying power (after Ta), CKE must be held LOW (≤ 0.2 × VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS and /DQS voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK, /CK, /CS, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided bellow.

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2 - 200mV
	VDD1 and VDD2 must be greater than VDDCA - 200mV
	VDD1 and VDD2 must be greater than VDDQ - 200mV
	VREF must always be less than all other supply voltages

Notes:

1. Ta is the point when any power supply first reaches 300mV.

2. Noted conditions apply between Ta and power-down (controlled or uncontrolled).

3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.

4. Power ramp duration tINIT0 (Tb - Ta) must not exceed 20ms.

5. For supply and reference voltage operating conditions..

6. The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Beginning at Tb, CKE must remain LOW for at least tINIT1 = 100 ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 × tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, /CS, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge.

If any MRRs are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 = 200µs (Td).

2. RESET Command: After tINIT3 is satisfied, the MRW RESET command must be issued (Td).

An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands.

3. MRRs and Device Auto Initialization (DAI) Polling: After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications.

Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set before proceeding.
As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration: After tINIT5 (Tf), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). For LPDDR2 devices that do not support ZQ calibration, this command will be ignored.

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after tZQINIT.

5. Normal Operation: After tZQINIT (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set

to configure the memory for the target frequency and memory configuration. After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop Events.

Initialization Timing Parameters

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Power Ramp Time	—	20	ms
tINIT1	Minimum CKE low time after completion of power ramp	100	—	ns
tINIT2	Minimum stable clock before first CKE high	5	—	tCK
tINIT3	Minimum idle time after first CKE assertion	200	—	us
tINIT4	Minimum idle time after Reset command, this time will be about 2 x tRFCab + tRPab	1	—	us
tINIT5	Maximum duration of Device Auto-Initialization	—	10	us
tCKb	Clock cycle time during boot	18	100	ns

Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-Off Sequence

Use the following sequence to power off the device. Unless specified otherwise, these steps are mandatory. While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DM, DQS, and /DQS voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, /CK, /CS, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Power Supply Conditions

Between	Applicable Conditions

Tx and Tz	VDD1 must be greater than VDD2—200mV
	VDD1 must be greater than VDDCA—200mV
	VDD1 must be greater than VDDQ—200mV
	VREF must always be less than all other supply voltages

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed 10ms. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Power-Off Timing

Symbol	Parameter	Min	Max	Unit
tPOFF	Maximum power-off ramp time	—	20	ms

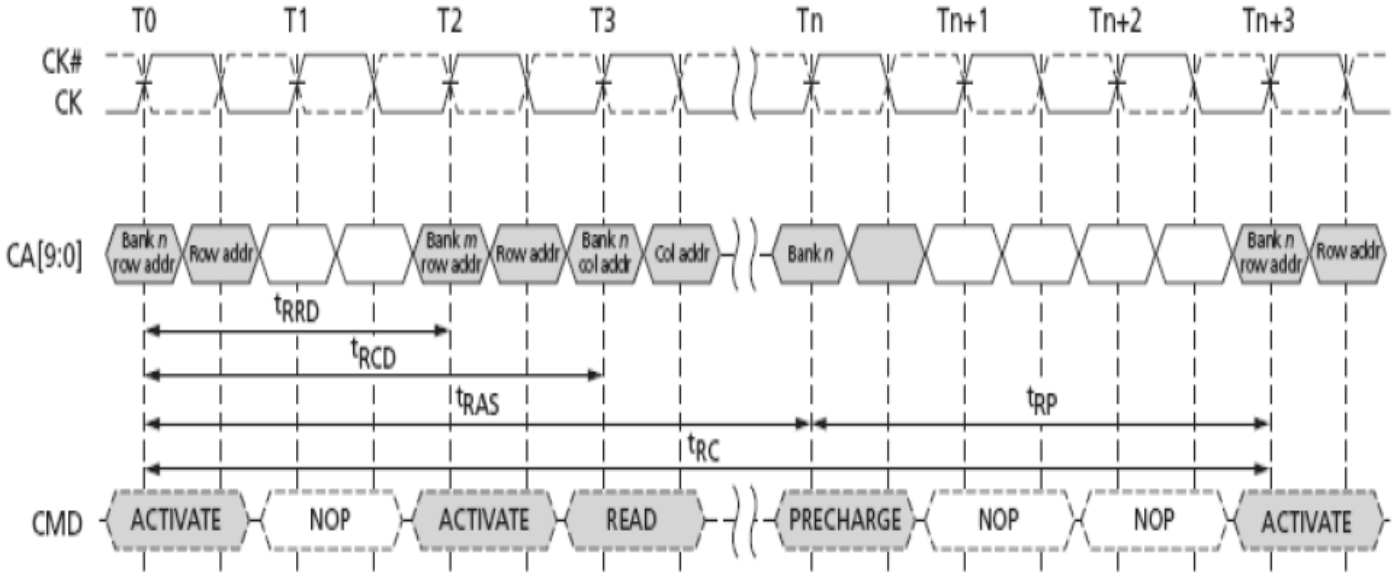
Active

The Active command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0-BA2 are used to select the desired bank. The row addresses R0-R14 is used to determine which row in the selected bank. The Active command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the active command is sent. Once a bank has been active, it must be precharged before another Active command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between two successive ACTIVE commands on the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between two successive ACTIVE commands on different banks is defined by tRRD.

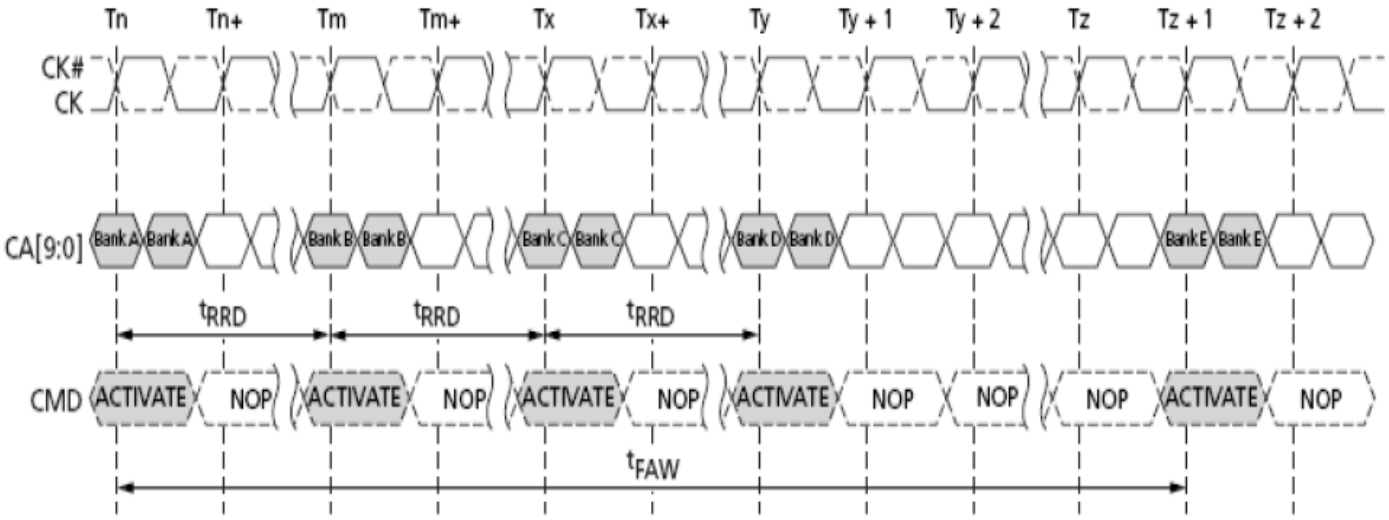
Certain restriction on operation of the 8 bank devices must be observed. One for restricting the number of sequential Active commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by diving tFAW[ns] by tCK[ns], and rounding up to the next integer value. A an example of the rolling window, if RU{(tFAW / tCK)} is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

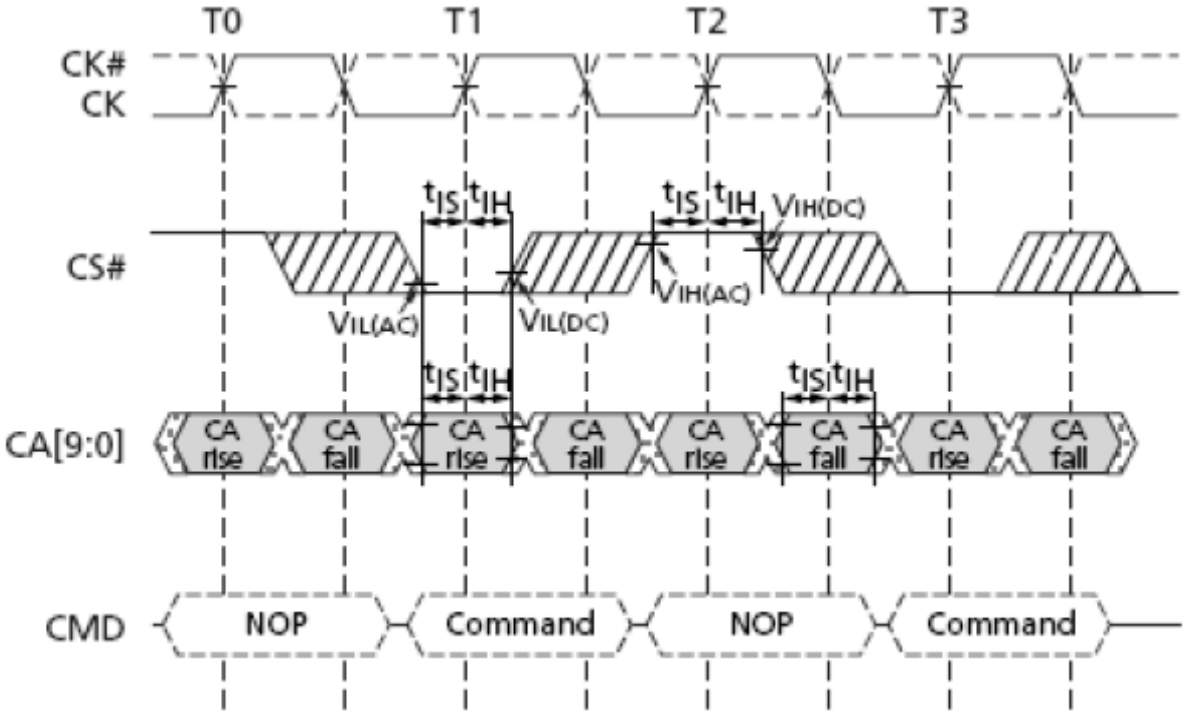
8 bank device Precharge All allowance: tRP for a Precharge All command for an 8 Bank device shall equal to tRPab, which is greater than tRPpb.



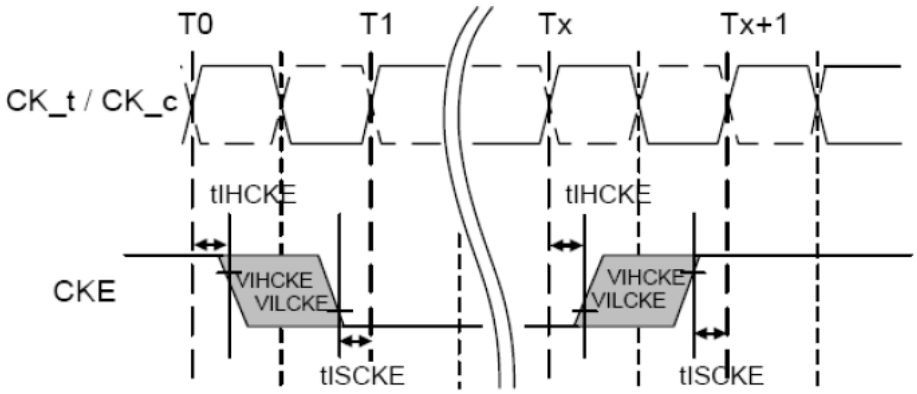
Notes: A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge.



Notes: tFAW is for 8-banks device only.



Notes: Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagram related to the CKE pin.



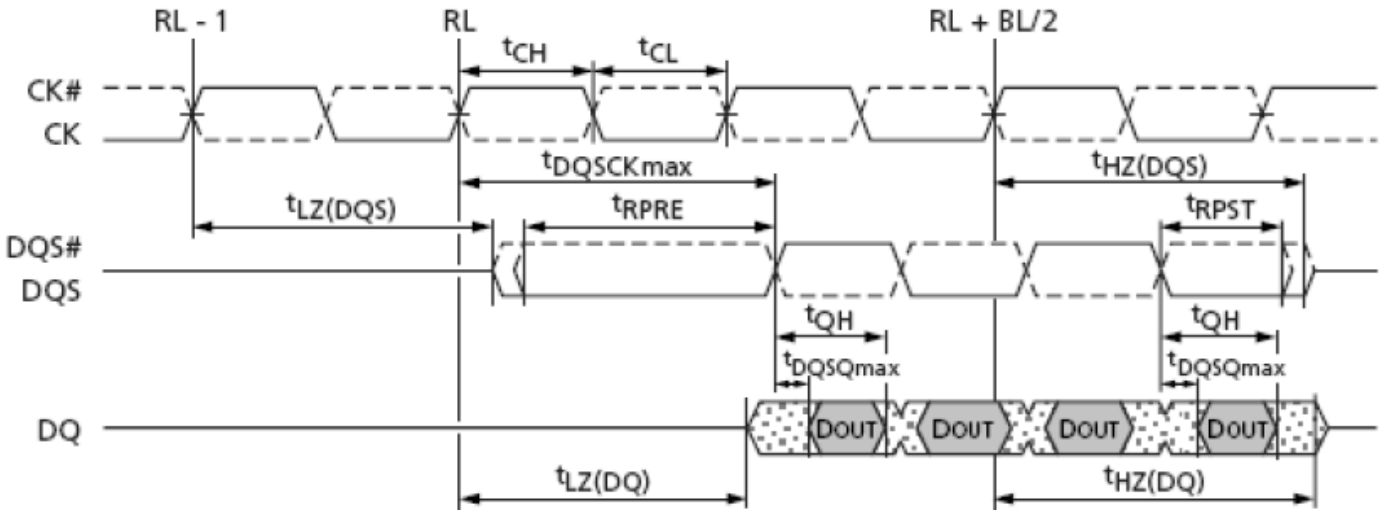
Notes:

1. After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

Read and Write Access Modes

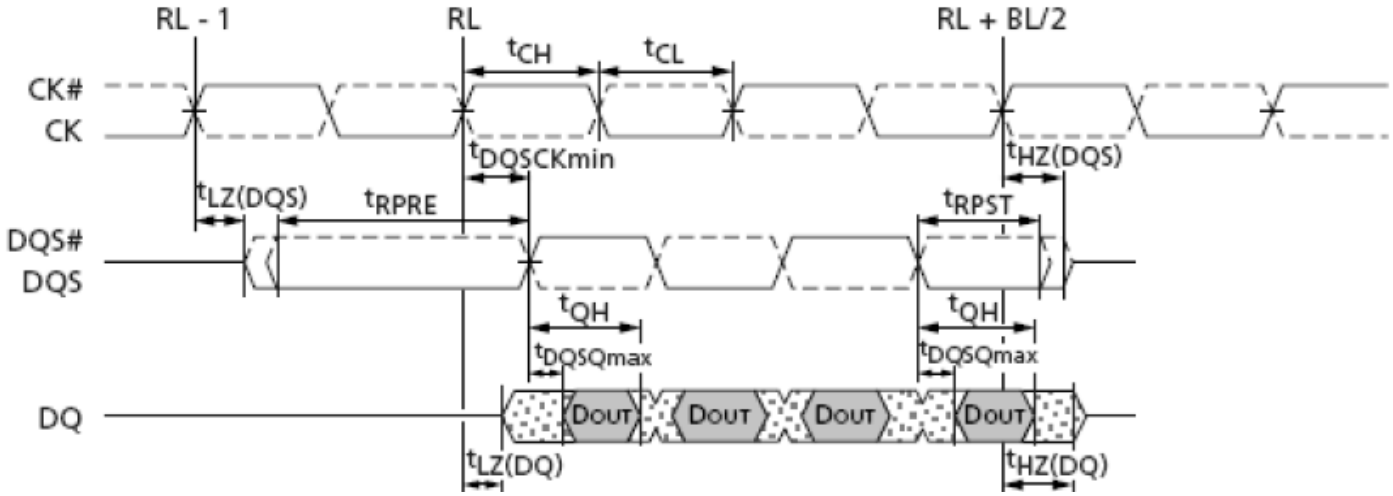
CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW). The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation, in case of BL=4 setting. In case of BL=8 and BL=16 settings, Reads may be interrupted by Reads, and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and that tCCD is met. The minimum CAS to CAS delay is defined by tCCD.

Burst Read

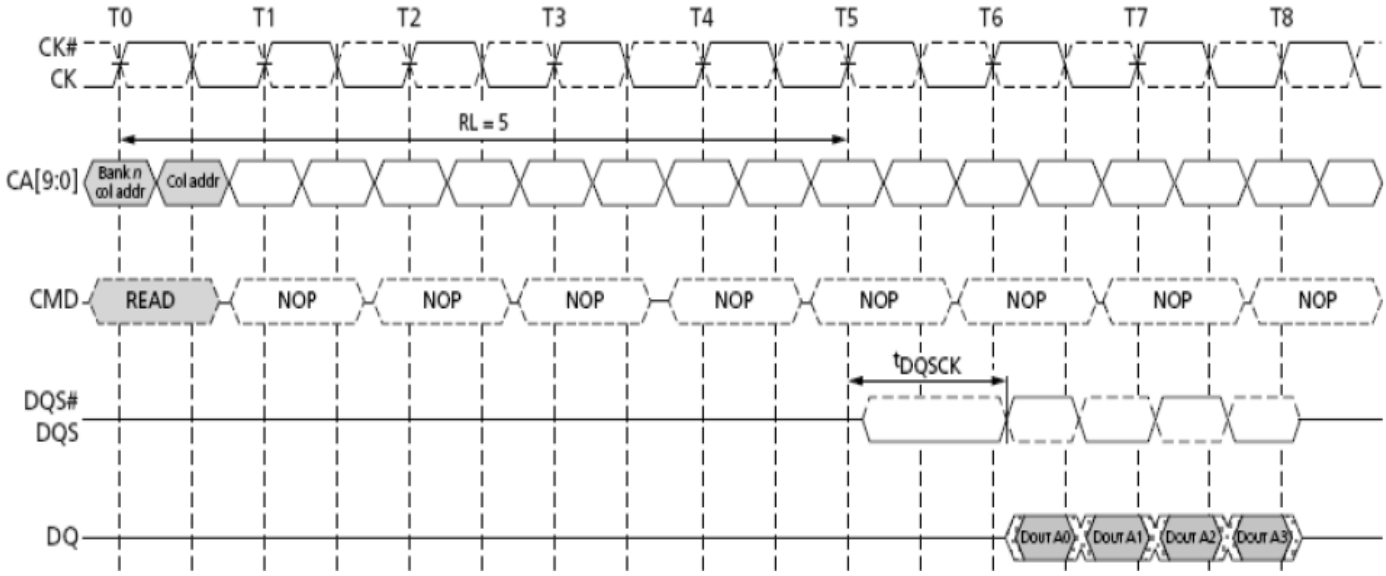


Notes: tDQSCK may span multiple clock periods. BL=4.

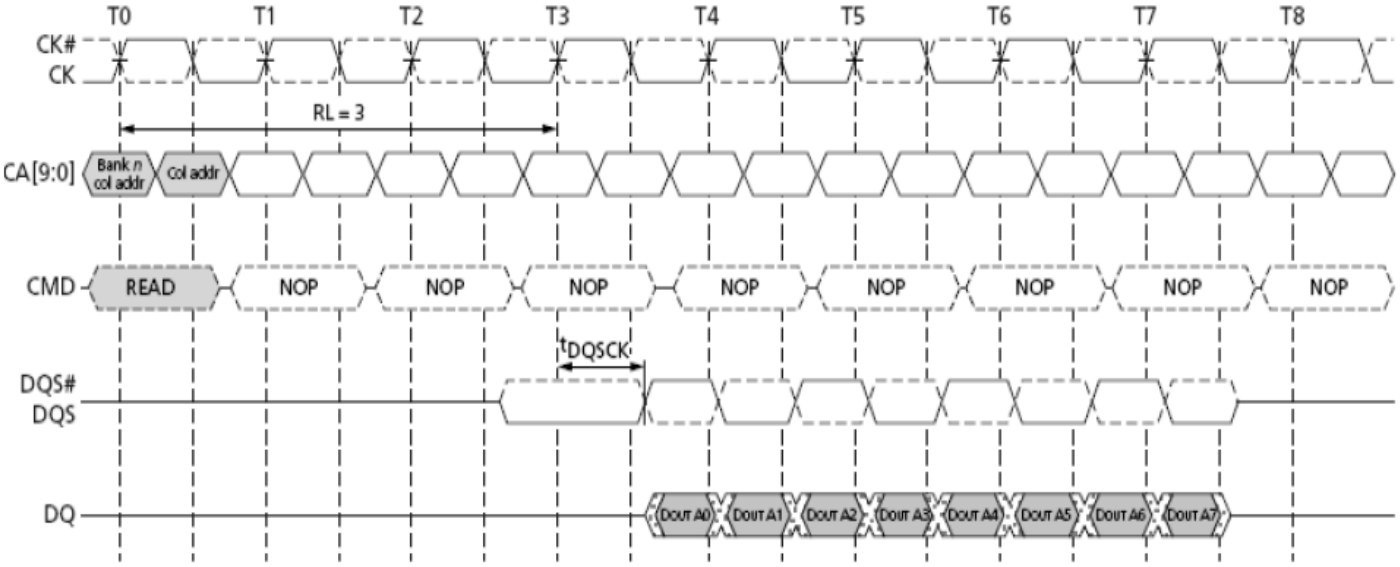
The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers. Timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS_c.



Notes: An effective BL=4

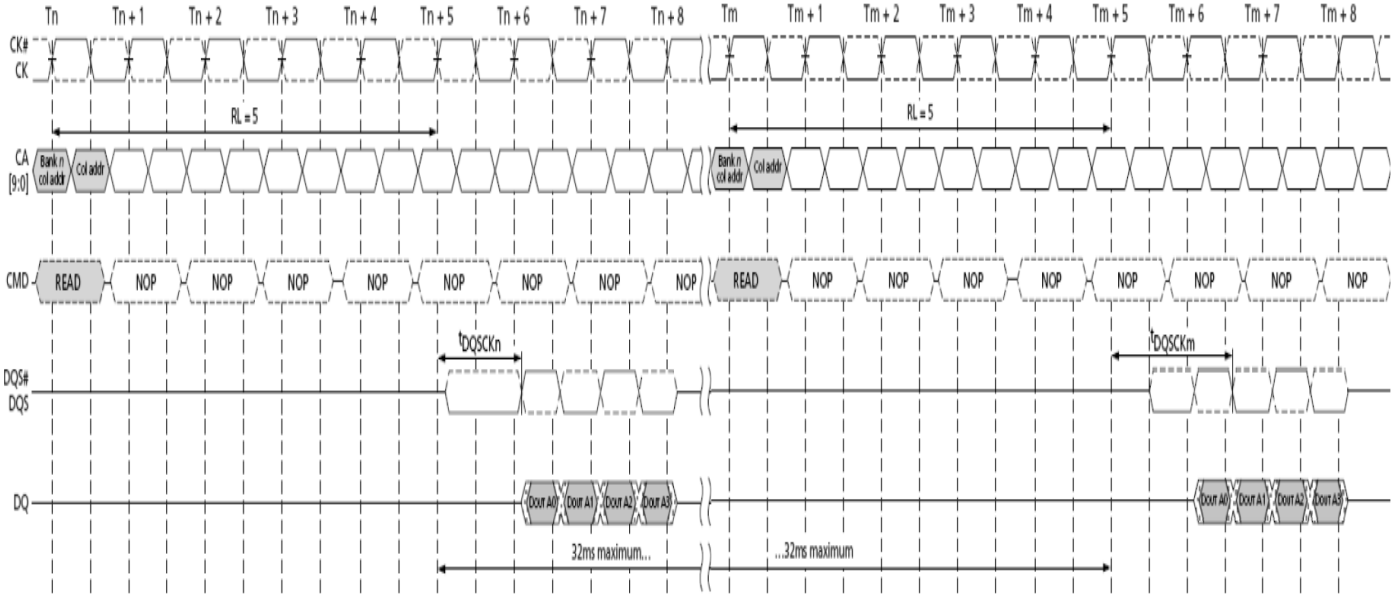


Notes: Burst read, RL=5, BL=4, tDQSCK > tCK



Notes: Burst read, RL=3, BL=8, tDQSCK < tCK

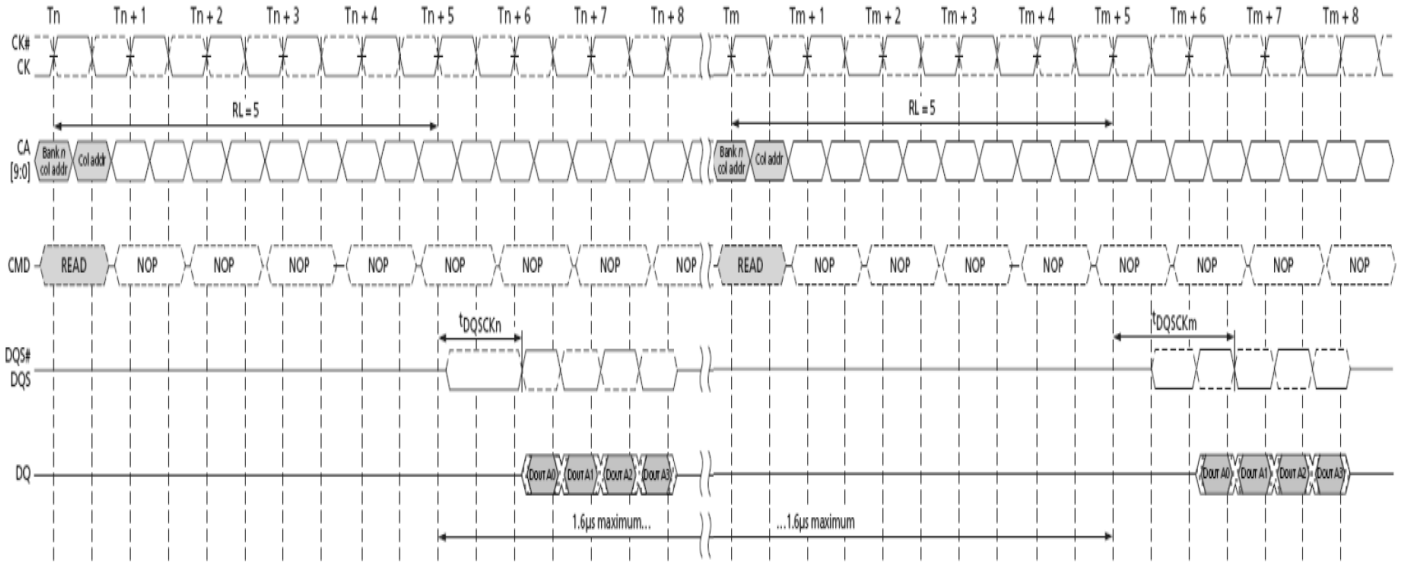
tDQSCKDL Timing



Notes:

1. tDQSCKDL=tDQSCKn – tDQSCKm
2. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any {tDQSCKn - tDQSCKm} pair within any 32ms rolling windows.

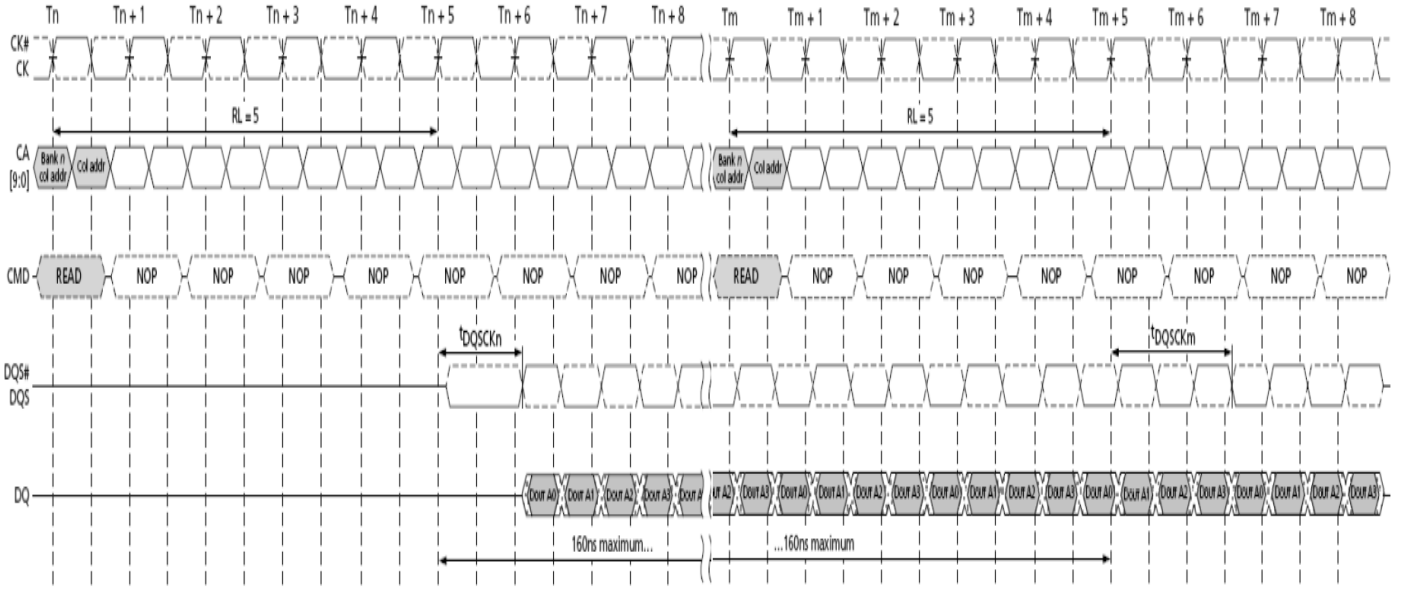
tDQSCKDM Timing



Notes:

1. tDQSCKDM = tDQSCKn - tDQSCKm
2. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any {tDQSCKn - tDQSCKm} pair within any 1.6us rolling windows.

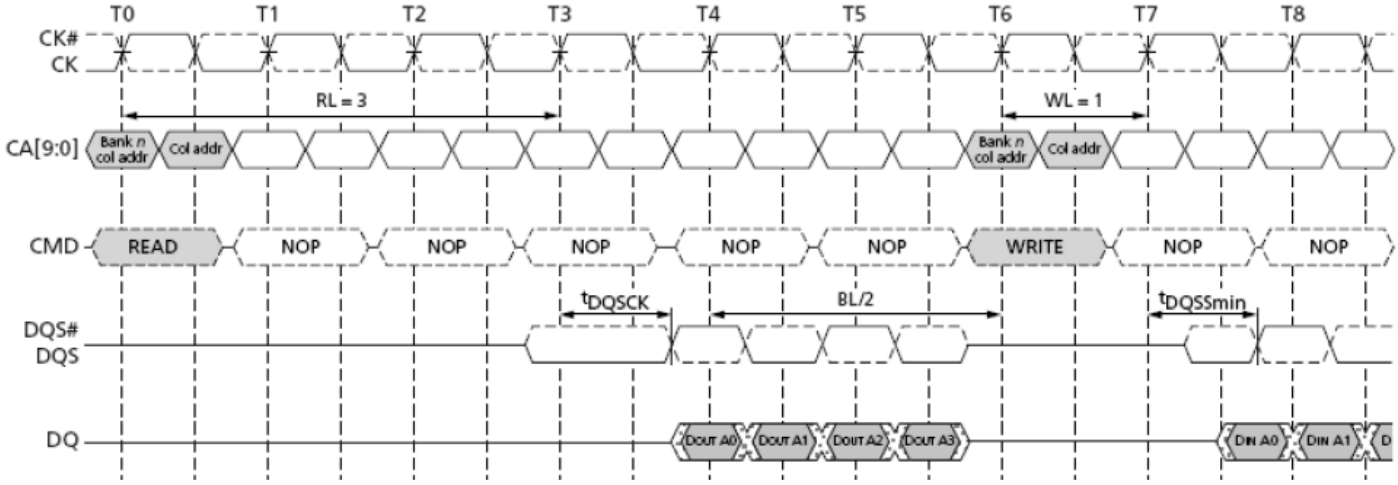
tDQSCKDS Timing



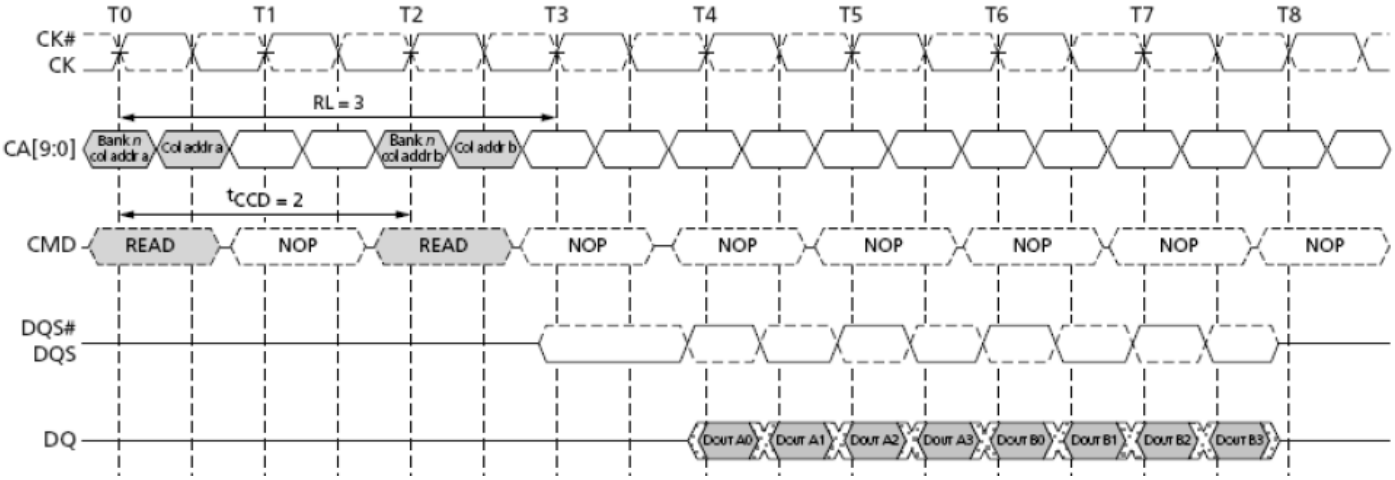
Notes:

1. tDQSCKDS = tDQSCKn - tDQSCKm
2. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any {tDQSCKn - tDQSCKm} pair for reads within a consecutive burst within any 160s rolling window.

The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 - WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used as BL to calculate the minimum READ-to-WRITE delay.



Notes: Burst read followed by burst write, RL=3, WL=1, BL=4

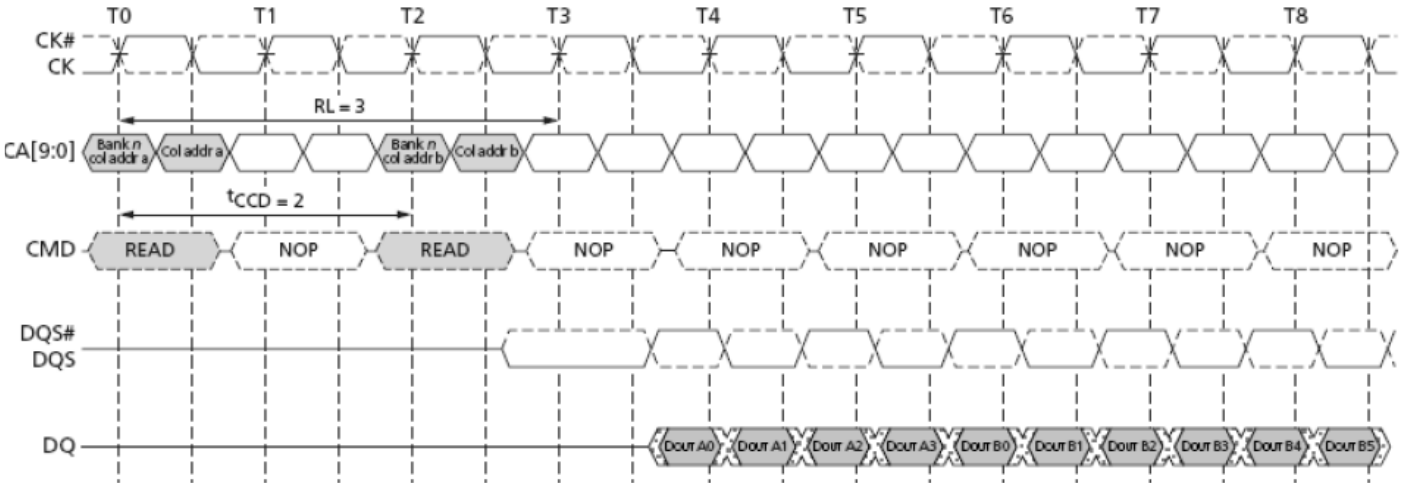


Notes: Seamless burst read: RL=3, BL=4, tCCD=2

The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 - WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used as BL to calculate the minimum READ-to-WRITE delay. The seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL=16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

Reads interrupted by a read

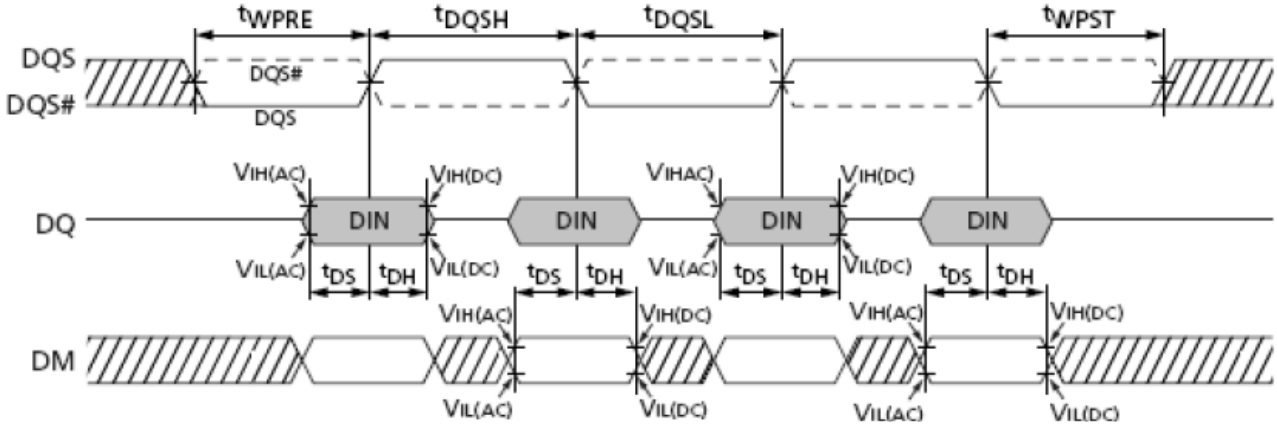
For LPDDR2-S4 devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met. For LPDDR2-S2 devices, burst reads may be interrupted by other reads on any subsequent clock, provided that tCCD is met.

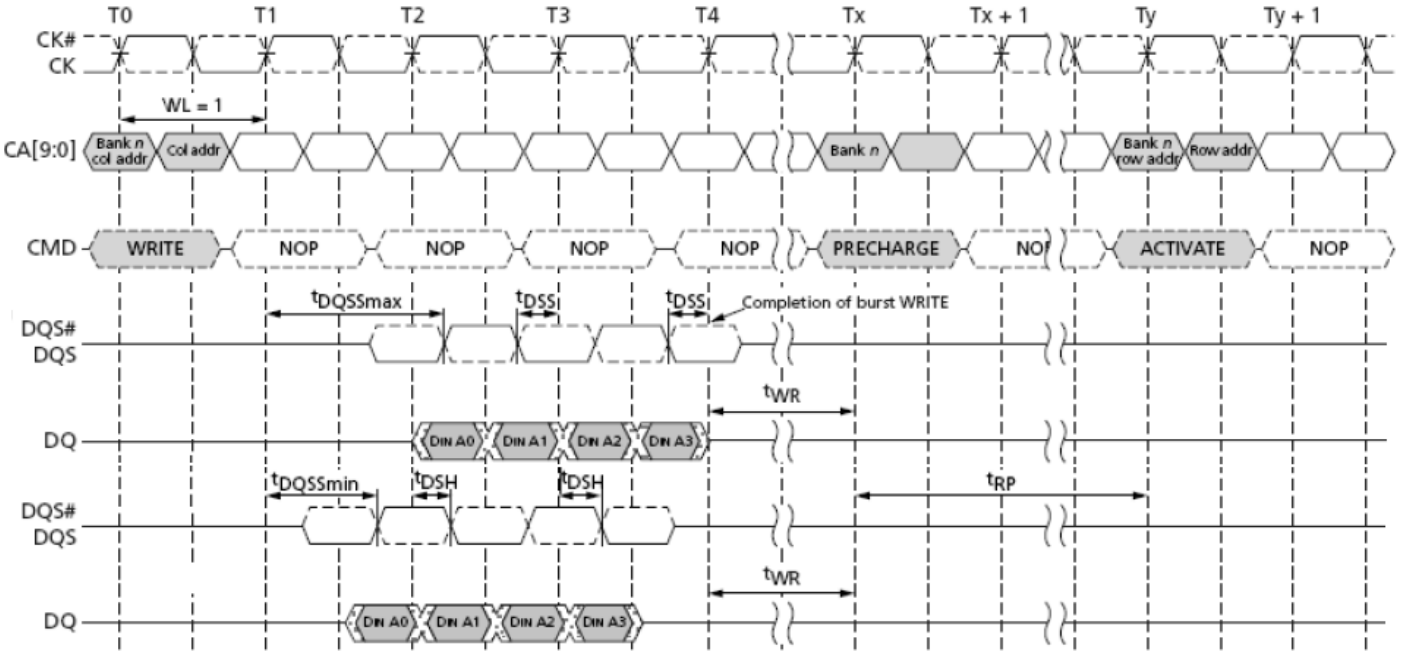


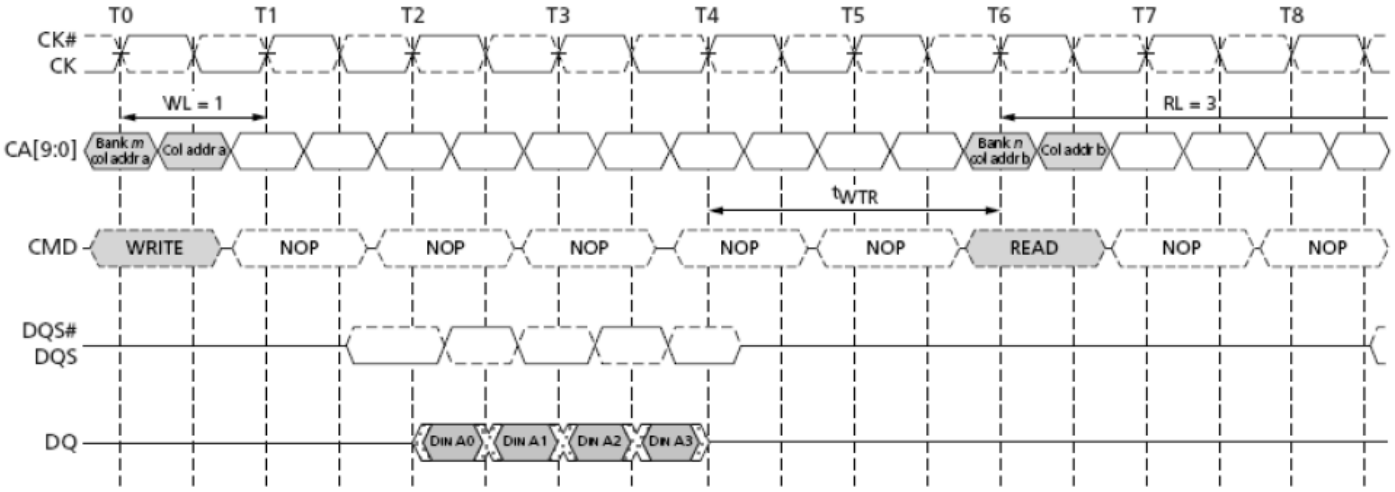
Notes: Read can only be interrupted by other reads or the BST command.

Burst Write

The burst WRITE command is initiated with /CS LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW tWPRE prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the cross-point of DQS and its complement, /DQS.

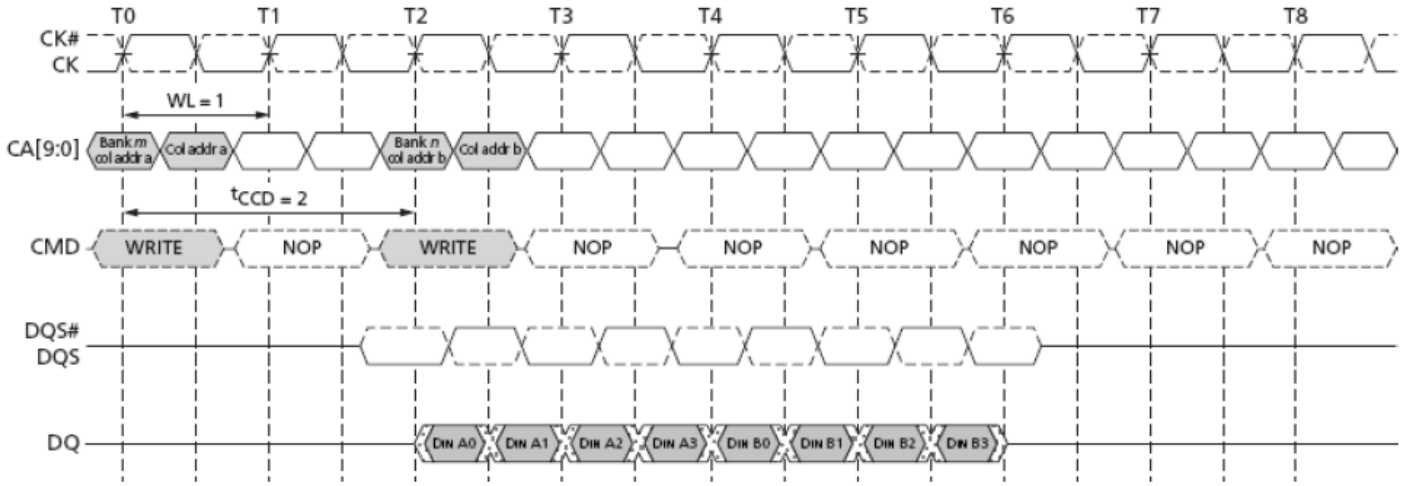






Notes:

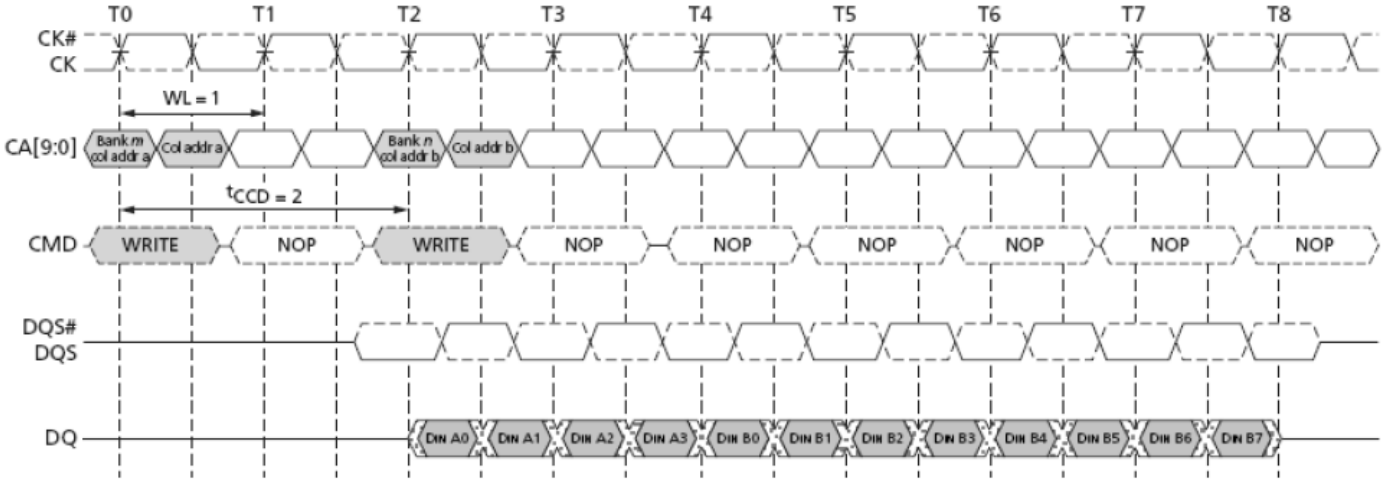
1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (tWTR / tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.



Notes: The seamless burst write operation is supported by enabling a write command every other clock for BL=4 operation, every four clocks for BL=8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Writes interrupted by a write

For LPDDR2-S4 devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that tCCD(min) is met. For LPDDR2-S2 devices, burst writes may be interrupted on any subsequent clock, provided that tCCD(min) is met.



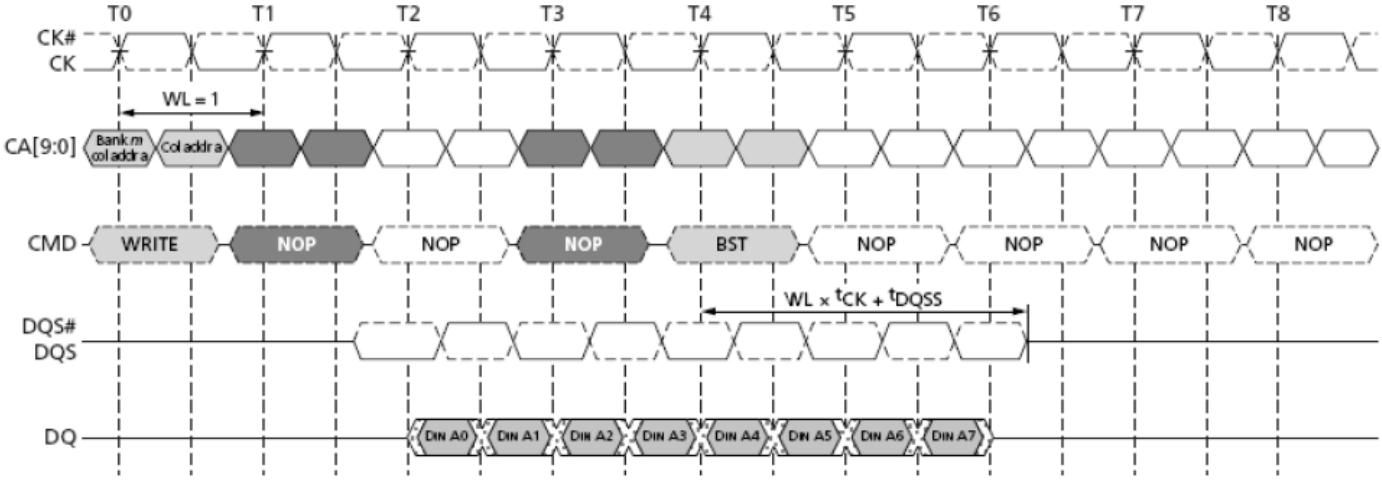
Notes:

1. WRITEs can only be interrupted by other WRITEs or the BST command.
2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

Burst Terminate (BST)

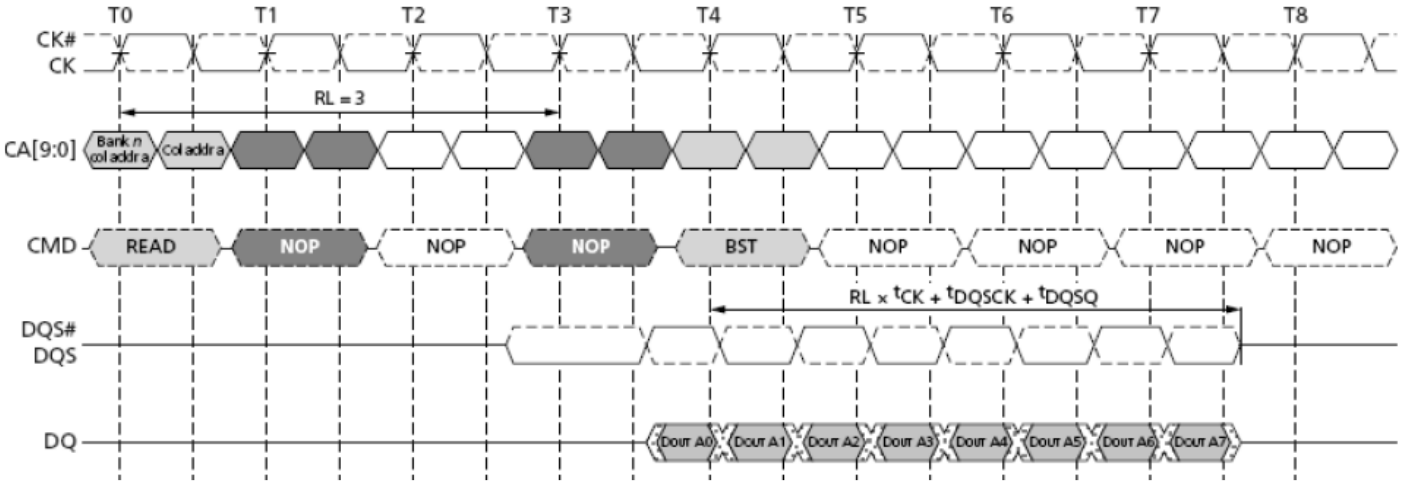
The BST command is initiated with /CS LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

1. Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).
2. If a READ or WRITE burst is truncated with a BST command, to calculate the minimum READ-to-WRITE or WRITE-to-READ delay, the effective burst length of the truncated burst should be used as the value for BL.
3. The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock where the BST command is issued. The BST command truncates an on-going write burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.
4. For LPDDR2-S4 devices, the 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of 4.
5. For LPDDR2-S2 devices, the 2-bit prefetch architecture enables BST command assertion in any cycle after a WRITE or READ command.



Notes:

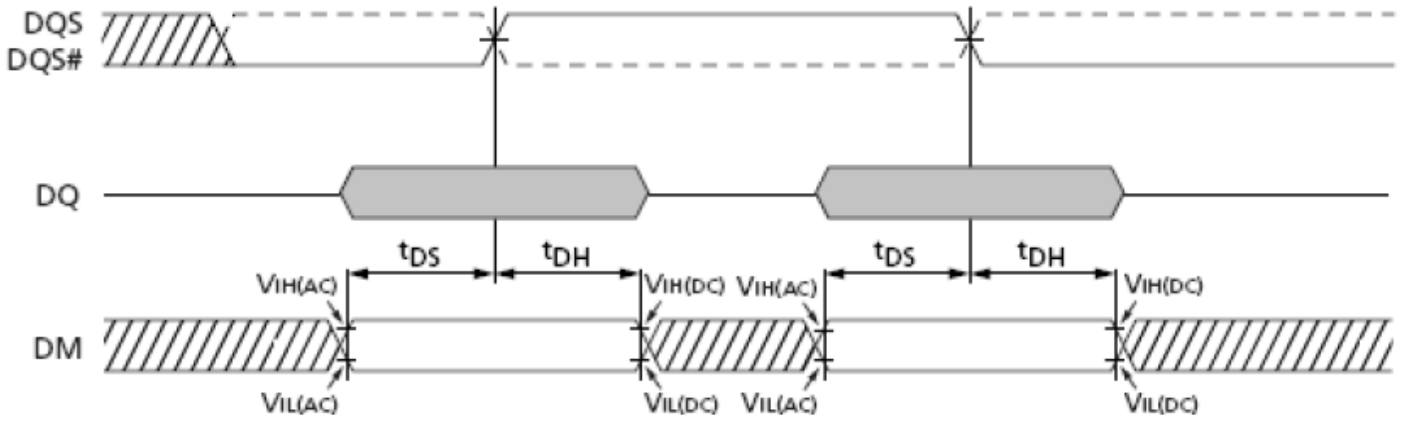
1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.



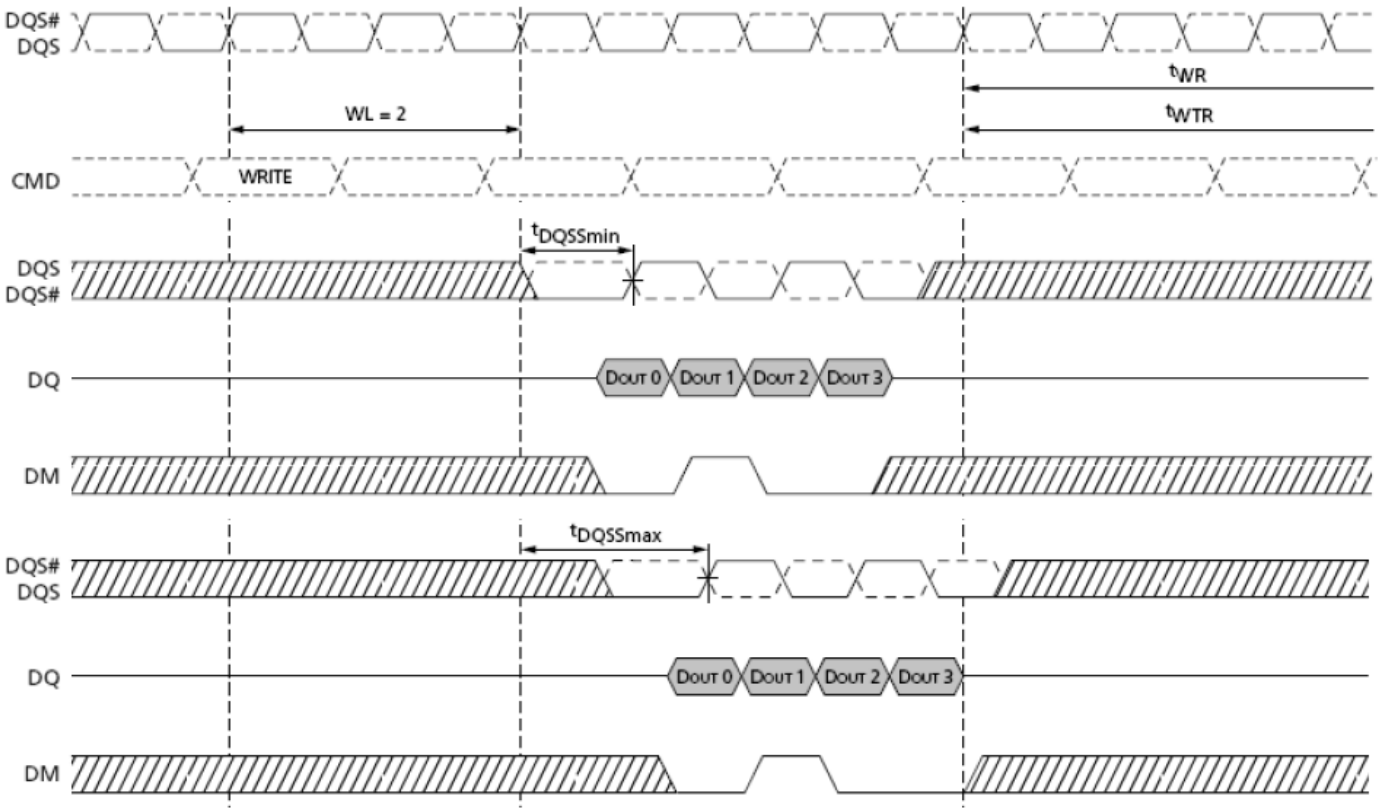
Notes:

1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.

Write Data Mask



One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.



Precharge

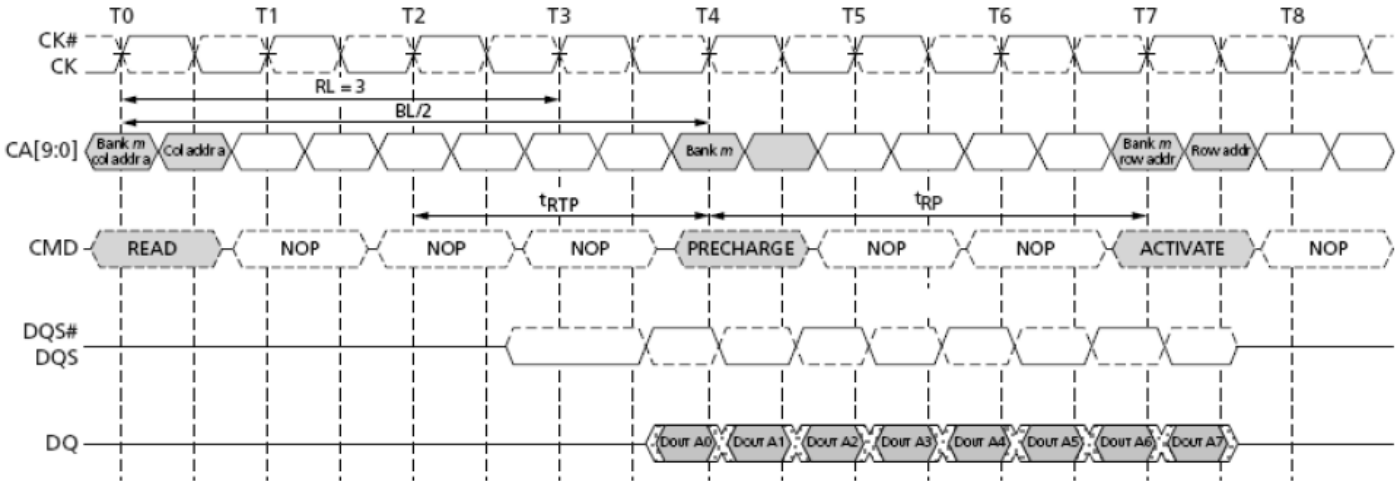
The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued. In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge for 8-bank devices (tRPab) will be longer than the Row Precharge time for a Single-Bank Precharge (tRPpb). For 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge (tRPab) is equal to the Row Precharge time for a Single-Bank Precharge (tRPpb).

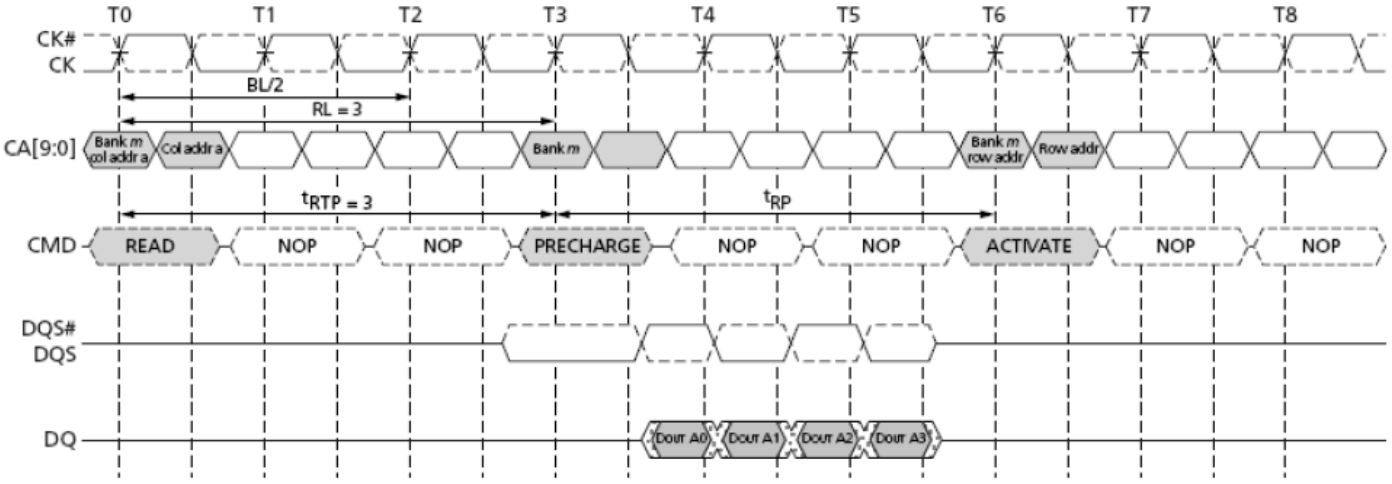
AB (CA4R)	BA2(CA9R)	BA1(CA8R)	BA0(CA7R)	Precharged Bank(s) 8-bank
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	don't care	don't care	don't care	All Banks

Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command can not be issued until after tRAS is satisfied. For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising cloak edge that initiates the last 4-bit precharge of a Read command. For LPDDR2-S2 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 2-bit prefetch of a Read command. This time is called tRTP (Read to Precharge).

For LPDDR2-S2 devices, tRTP begins BL/2 – 1 clock after the Read command. For LPDDR2-S4 devices, tRTP begins BL/2 – 2 clock cycles after the Read command. If the burst is truncated by a BST command, the effective “BL” ahsll be used to calculate when tRTP begins.

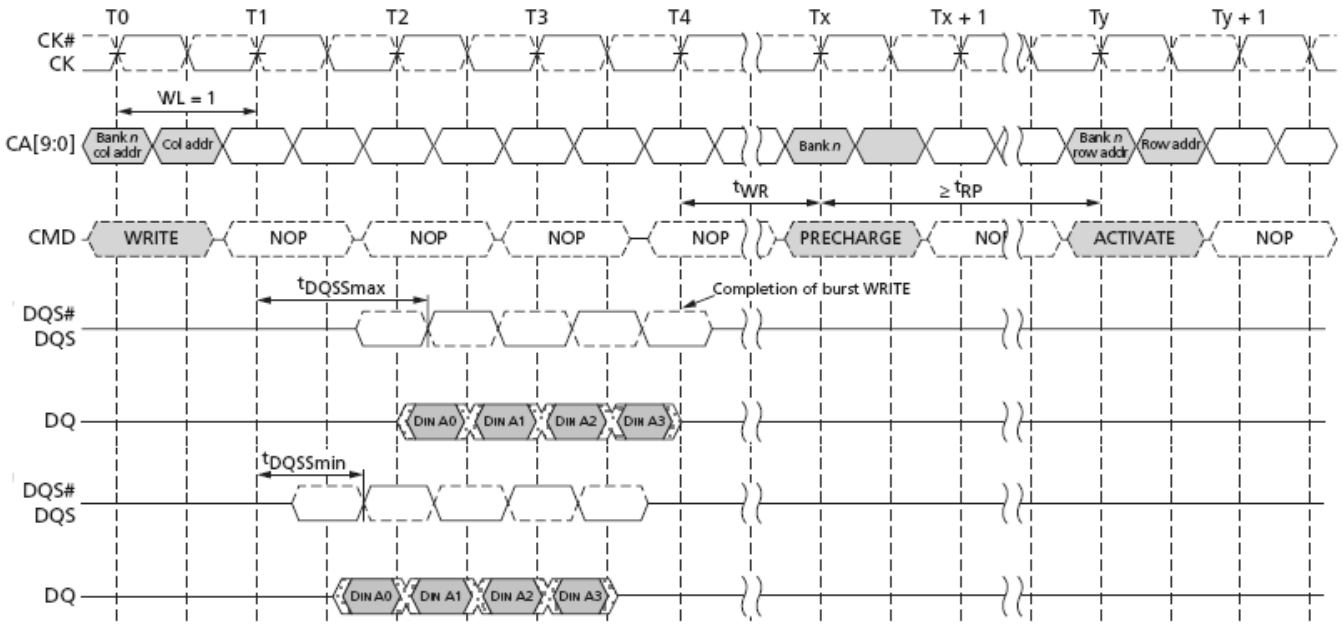




Burst Write operation followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the Precharge command. No Precharge command to the same bank should be issued prior to the tWR delay. LPDDR2-S2 devices write data to the array in prefetch pairs (prefetch = 2) and LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been completely. Therefore, the write recovery time (tWR) starts different boundaries for LPDDR2-S2 and LPDDR2-S4 devices.

For LPDDR2-S2 devices, minimum Write to Precharge command spacing to the same bank is WL + RU(BL/2) + 1 + RU(tWR/tCK) clock cycles. For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1+ RU (tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.



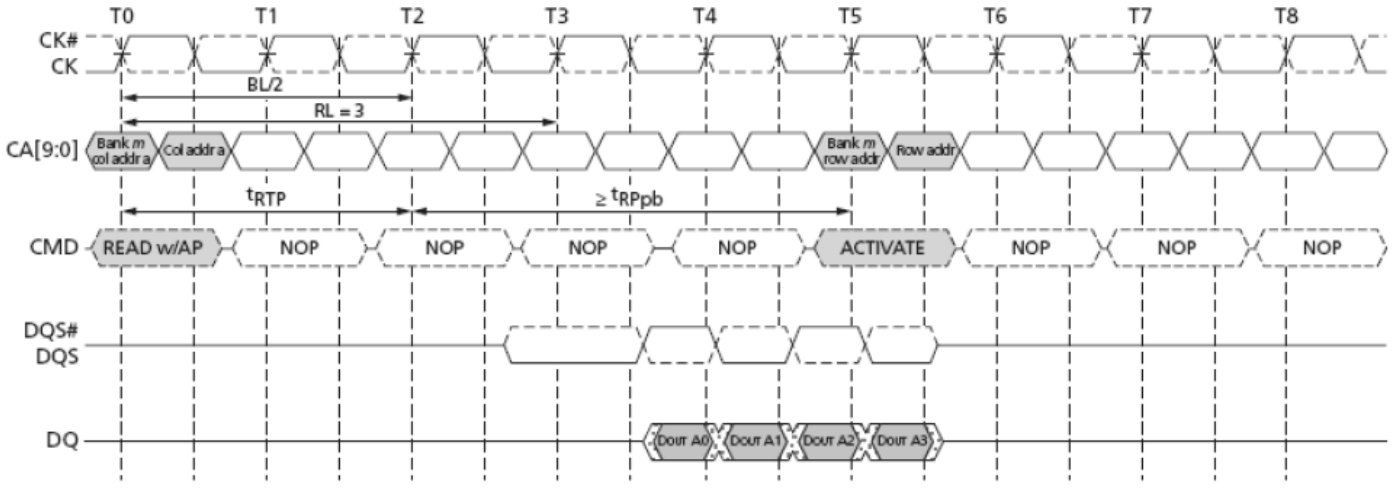
Auto Precharge

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is LOW when the Read or Write command is issued, the normal Read or Write burst operation is executed and the bank remains active at the completion of the burst. If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. LPDDR2-S2 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 – 1 + RU(tRTP/tCK) clock cycles later than the Read with AP command. LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 – 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater. A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously:

1. The RAS precharge time (tRP) has been satisfied from the clock at which the auto-precharge begins.
2. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

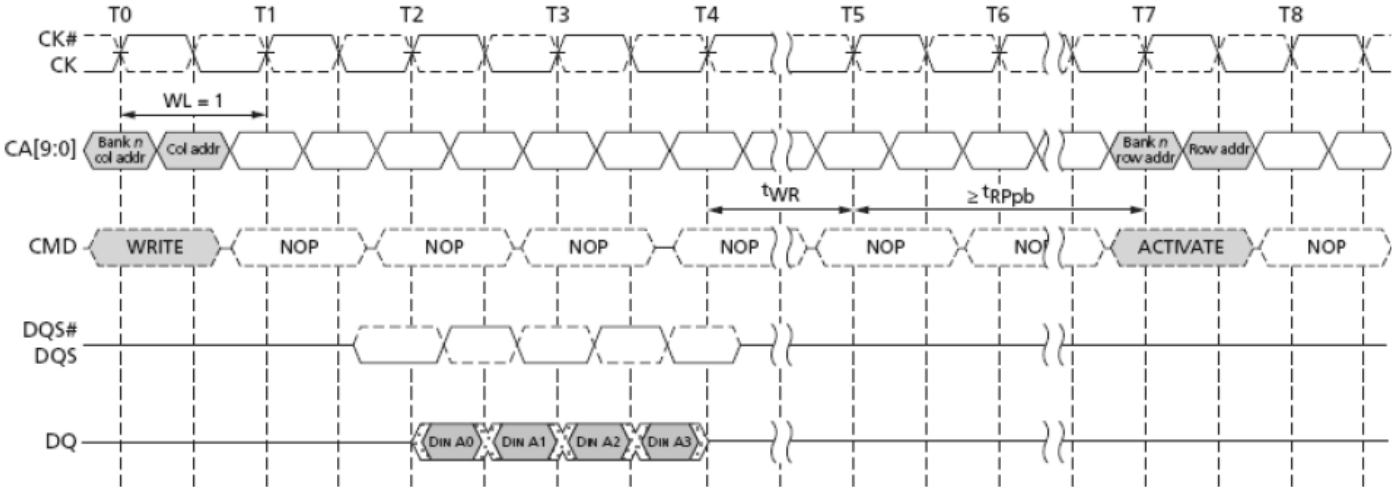


Burst Write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto-precharge operation on the rising edge which is tWR cycles after the completion of the burst write. A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied:

1. The RAS precharge time (tRP) has been satisfied from the clock at which the auto-precharge begins.

2. The RAS cycle time (tRC) from the previous bank activation has been satisfied.



Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(RTP/ CK)) - 2 + RU(tRPpb/tCK)	clks	1
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + RU(tWR/tCK) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRP /tCK)	clks	1
		pb		
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

Notes:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command

issued to that bank.

2. Any command issued during the minimum delay time as specified above table is illegal.
3. After read with AP, seamless read operations to different banks are supported. After write with AP, seamless write operations to different banks are supported. Read w/AP and Write a/AP may not be interrupted or truncated.

Refresh Command

The Refresh Command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of the clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh Command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-…". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command.

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command. The REFpb command may not be issued to the memory until the following conditions are met:

1. tRFCab has been satisfied after the prior REFab command.
2. tRFCpb has been satisfied after the prior REFpb command.
3. tRP has been satisfied after the prior Precharge command to that given bank.

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command. The target bank is inaccessible during the Per Bank Refresh cycle (tRFCpb), however other banks within the device are accessible and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank Refresh cycle has completed, the affected bank will be in the idle state. As shown in the table, after issuing REFpb:

1. tRFCpb must be satisfied before issuing a REFab command.
2. tRFCpb must be satisfied before issuing an ACTIVE command to a same bank.
3. tRRD must be satisfied before issuing an ACTIVE command to a different bank.
4. tRFCpb must be satisfied before issuing another REFpb command.

An all Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in idle state when REFab is issued (for instance, by Precharge All Bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. As shown in the table, the REFab command

may not be issued to the memory until the following conditions have been met:

1. tRFCab has been satisfied after the prior REFab command.
2. tRFCpb has been satisfied after the prior REFpb command.
3. tRP has been satisfied after the prior Precharge commands.

When the All Bank Refresh cycle has completed, all banks will be in the idle state. As shown in the table, after issuing REFab:

1. the tRFCab latency must be satisfied before issuing an ACTIVATE command.
2. the tRFCab latency must be satisfied before issuing a REFab or REFpb command.

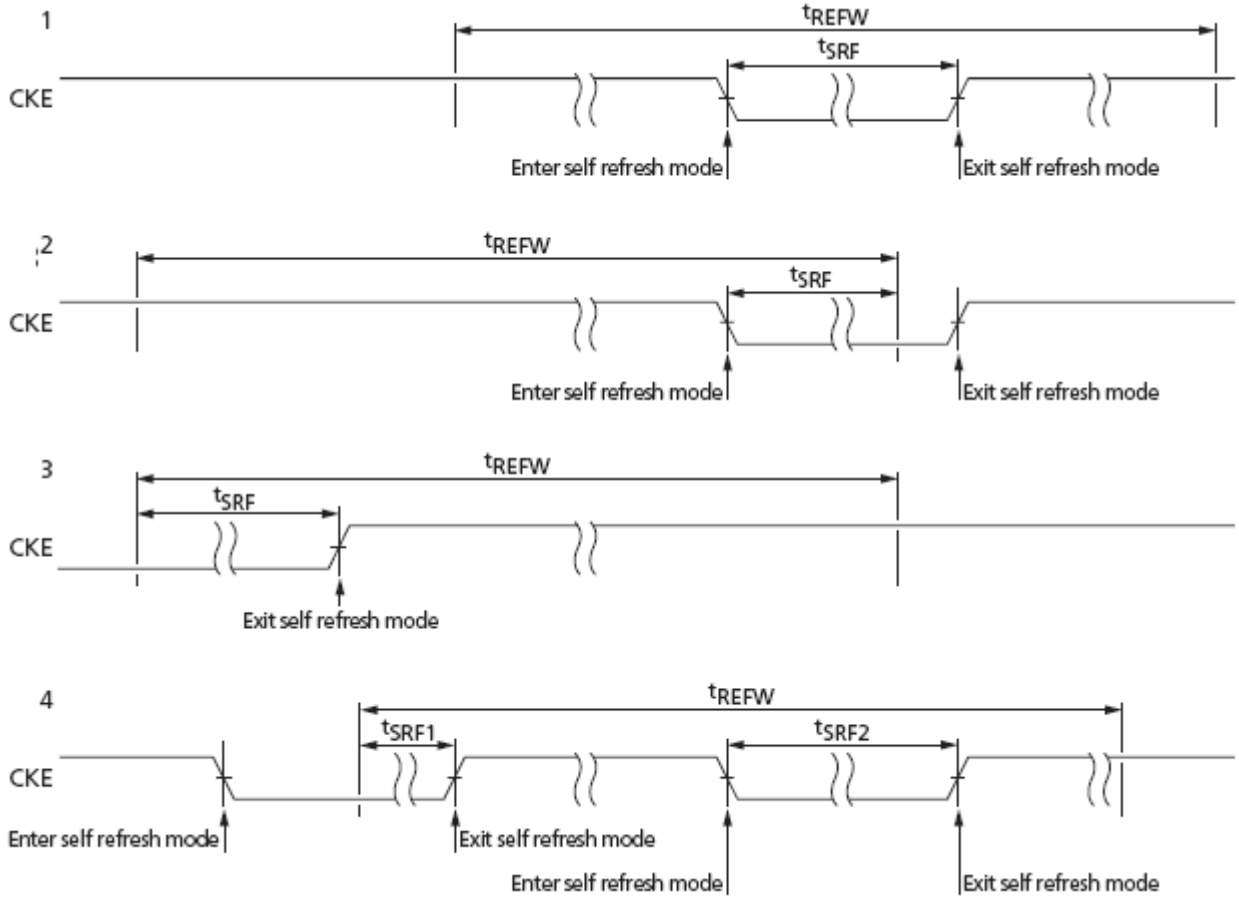
Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate cmd to *any* bank .	
		REFpb	
tRFCab	REFpb	REFab	
		Activate cmd to *same* bank as REFpb	
		REFpb	
tRRD	REFpb	Activate cmd to *different* bank than REFpb	
	Activate	REFpb affecting an idle bank (different bank than Activate)	1
		Activate cmd to *different* bank than prior Activate	

Notes:

1. A bank must be in the idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the idle state.

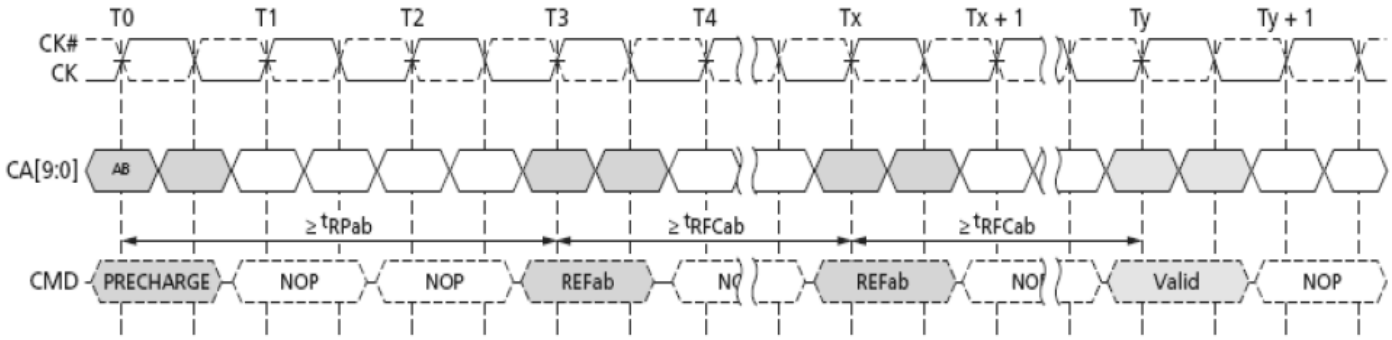
Refresh Requirements

1. Minimum number of Refresh commands: LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (tREFW = 32 ms @ MR4[2:0] = 011 or TC ≤ 85°C). For actual values per density, and the resulting average refresh interval (tREFI). For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.
2. Burst Refresh limitation: To limit maximum current consumption, a maximum of REFab commands may be issued in any rolling tREFBW (tREFBW = 4 x 8 x tRFCab). This condition does not apply if REFpb commands are used.
3. Refresh Requirements and Self-Refresh: If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:
   R* = R - RU{tSRF / tREFI} = R - RU{R * tSRF / tREFW}; where RU stands for the round-up function
4. Minimum number of Refresh commands: LPDDR2 requires a minimum number, R, of REFRESH (REFab)

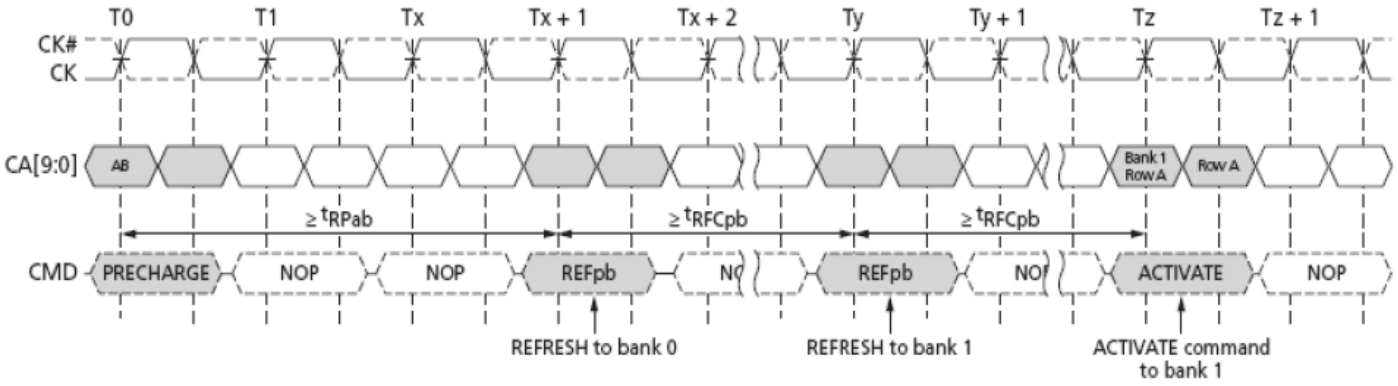


Notes:

1. Time in self refresh mode is fully enclosed in the refresh window (tREF).
2. At self-refresh entry.
3. At self-refresh exit.
4. Several intervals in self refresh during one tREFW interval. In this example, tSRF = tSRF1 + tSRF2.



Notes: All bank refresh operation



Notes:

1. In the beginning of this example, the REFpb bank is pointing to Bank0.

2. Operations to other banks than the bank being refreshed are allowed during the tREFpb period.

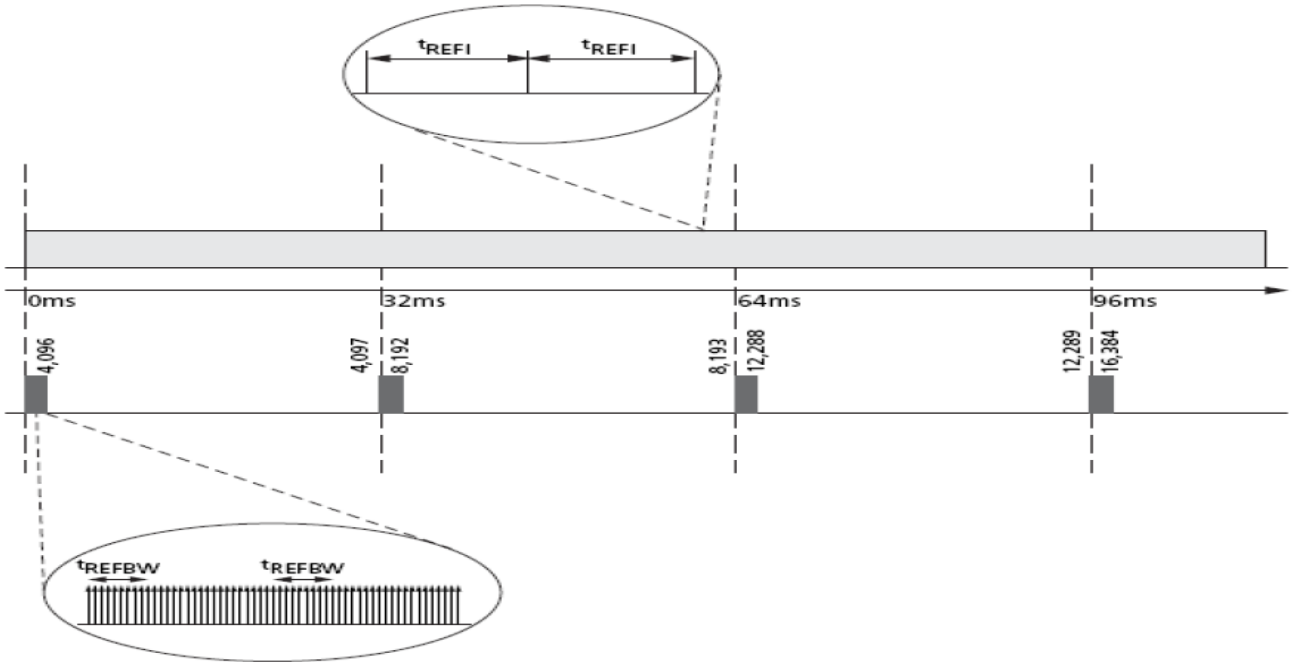
LPDDR2-S4 devices allow significant flexibility in scheduling REFRESH commands, as long as the boundary conditions above are met. In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by tREFW - (R / 8) * tREFBW = tREFW - R * 4 * tRFCab. Tj <= 85℃ this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms.

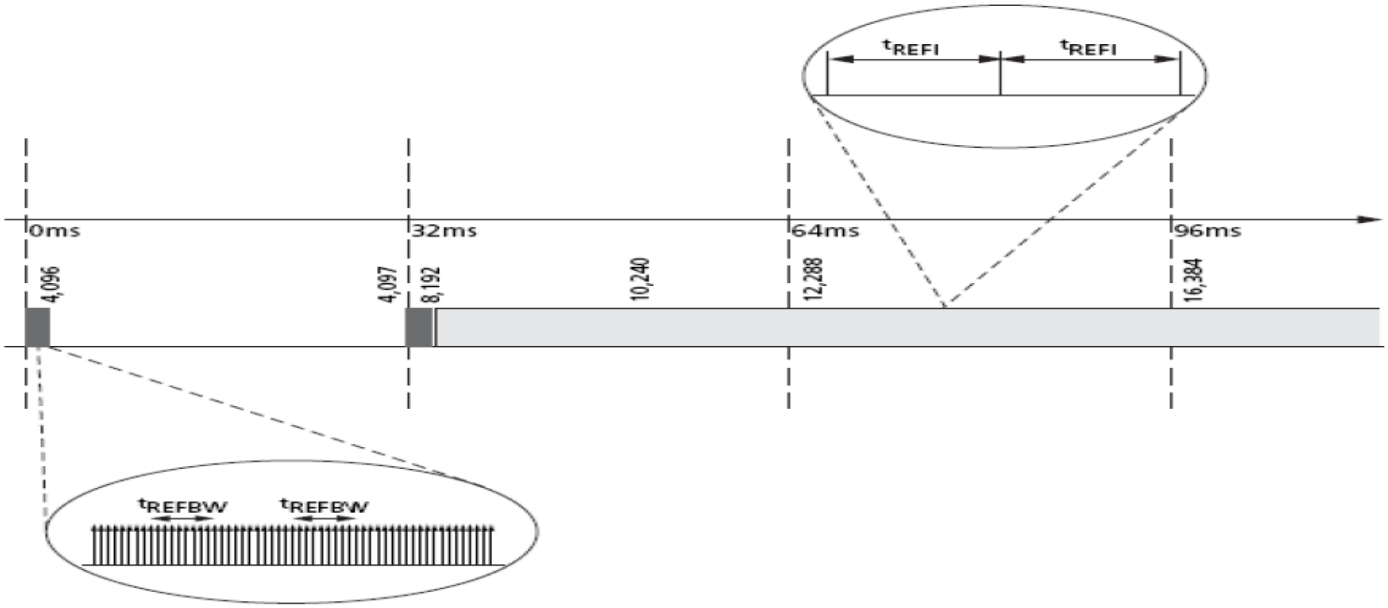
While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition. If this transition happens directly after the burst refresh phase, all rolling tREFW intervals will have at least the required number of refreshes.

As an example of a non-allowable transition, the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimum number of REFRESH commands is not satisfied.

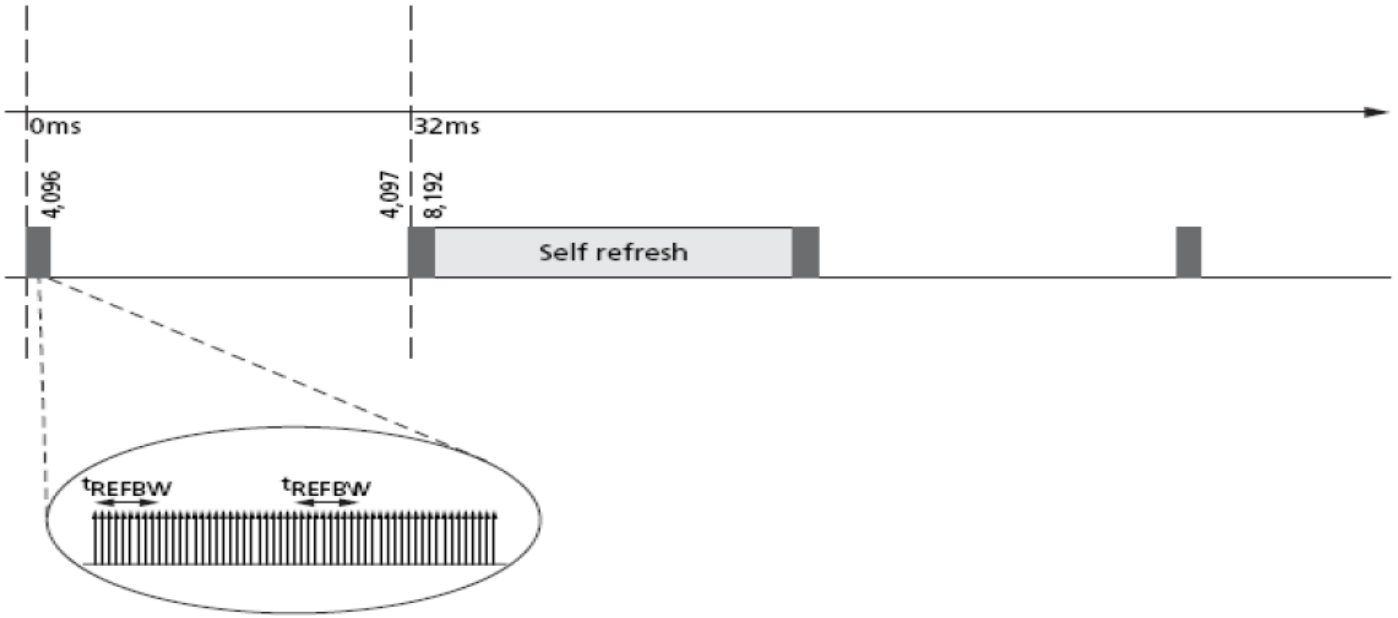
The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern and begin with the burst phase upon exit from Self-Refresh.



Notes: For a device Tj less than or equal to 85 ℃ the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.



Note: in a 1Gb LPDDR2 device @ Tj less than or equal to 85 ℃ the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have one refresh command per 0.52us followed by ~30 ms without any REFRESH command.



Self-Refresh Operation

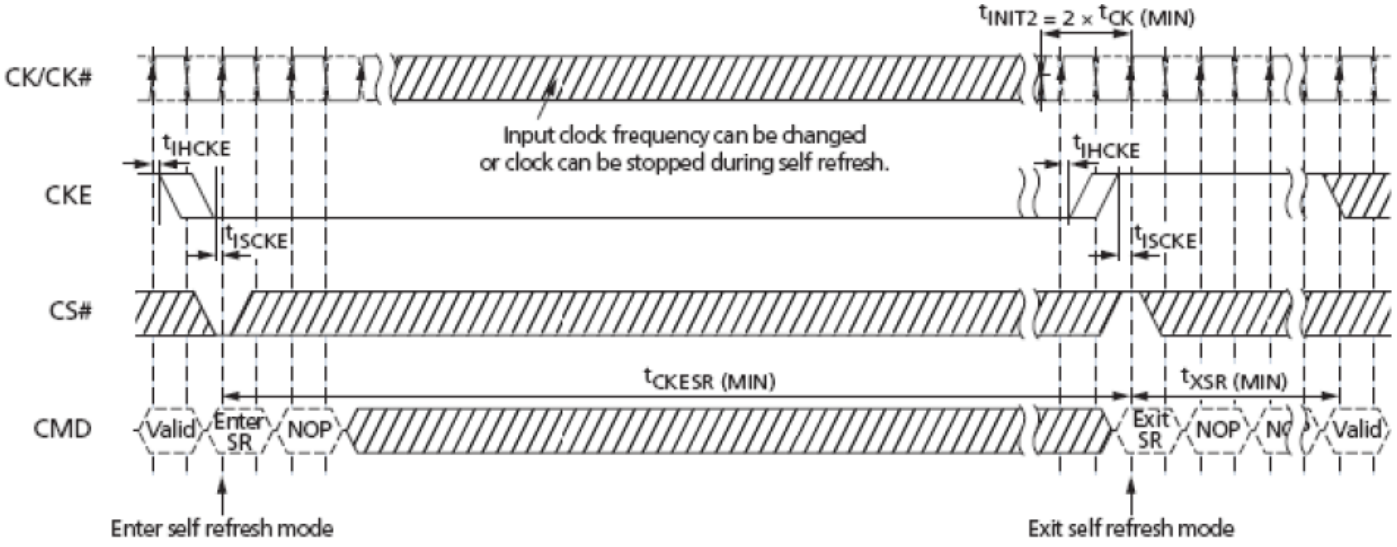
The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-SX devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-SX devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperature. Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self-refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefQD and VrefCA may be at any level within minimum and maximum levels. However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits. The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period, once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self

Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.



Notes:

1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 5 clocks (tINIT2) of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the all banks idle state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven High.
4. A valid command maybe issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

Partial Array Self-Refresh: Bank Masking

Each bank of LPDDR2 SDRAM can be independently configured whether a self-refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to entire bank is not blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, the array space being refreshed within that bank is determinate by the programmed status of the segment mask bit.

Partial Array Self-Refresh: Segment Masking

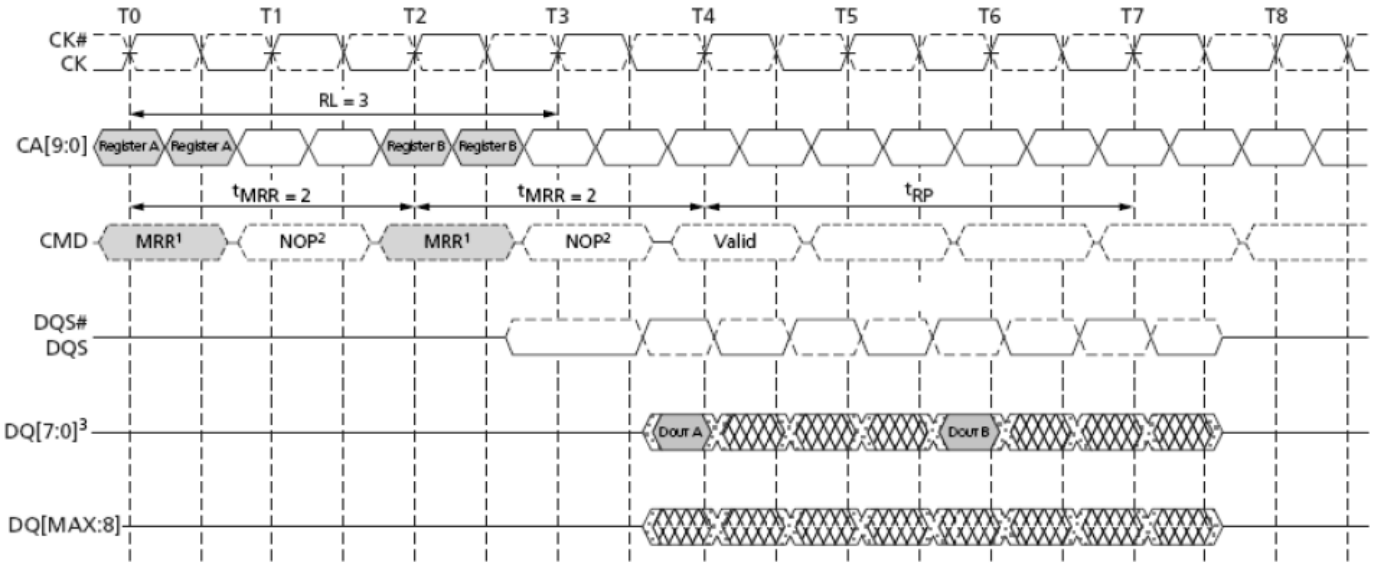
When the mask bit to an address range (represented as a segment) is programmed as masked, a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled. A segment-masking scheme can be used in place of or in combination with a bank masking scheme in LPDDR2-S4 SDRAM. Each segment-mask bit setting is applied across all banks.

	Segment Mask (MR17)	Bnak 0	Bank 1	Bank 2	Bank 3	Bnak 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for LPDDR SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in “DQ Calibration”. All DQS shall be toggled for the duration of the Mode Register Read burst.

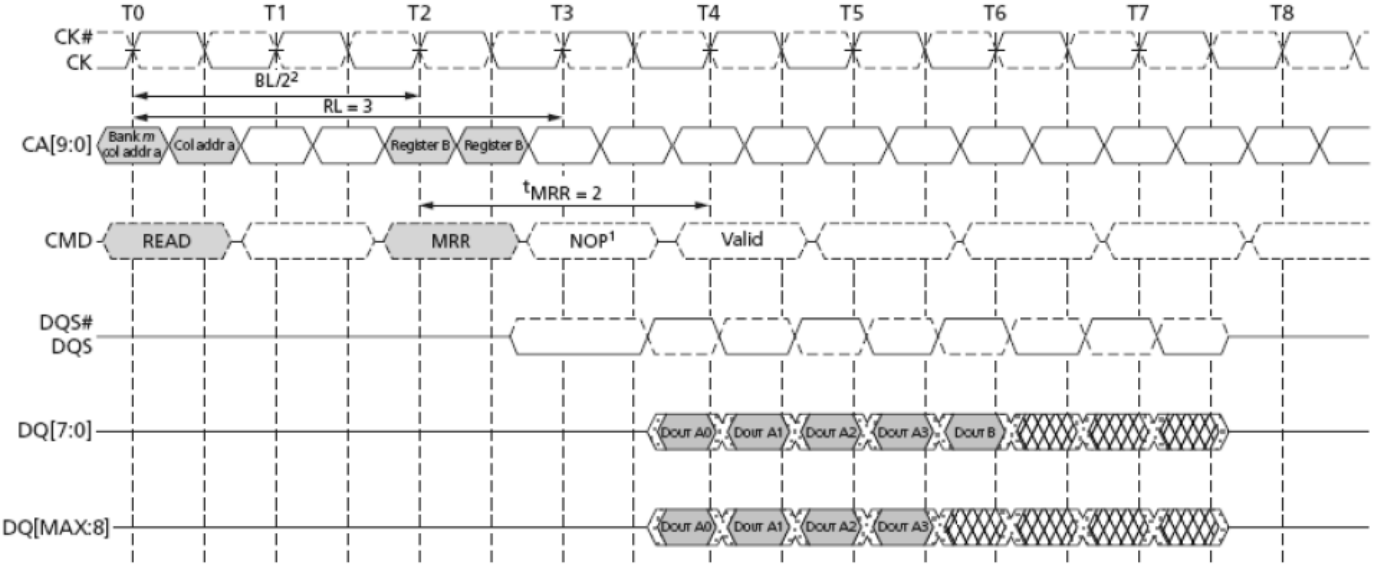
The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.



Notes:

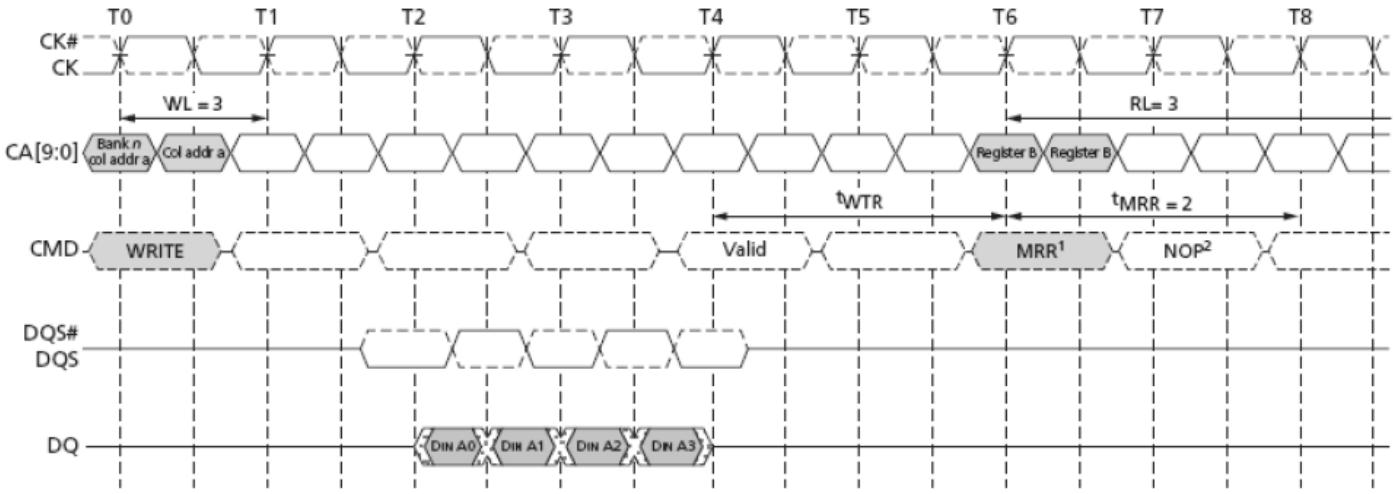
1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ Calibration.
2. Only the NOP command is supported during tMRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR. Note that if a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the value BL.



Notes:

1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. Only the NOP command is supported during tMRR.



Notes:

1. The minimum number of clocks from the burst write command to the Mode Register Read command is [WL+1+BL/2+ RU(Twtr/tCK)].
2. Only the NOP command is supported during tMRR.

Temperature Sensor

LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range (ETR), and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine if operating temperature requirements are being met. Temperature sensor data may be read from MR4 using the Mode Register Read protocol.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges. For example, TCASE could be above 85°C when MR4[2:0] equals 011B. To assure proper operation using the temperature sensor, applications must accommodate the specifications shown in bellow.

Parameter	Symbol	Max/Min	Value	Unit
System Temperature Gradient	TempGradient	Max	System Dependent	C/s
MR4 Read Interval	ReadInterval	Max	System Dependent	ms
Temperature Sensor Interval	tTSI	Max	16	ms
System Response Delay	SysRespDela y	Max	System Dependent	ms
Device Temperature Margin	TempMargin	Max	2	C

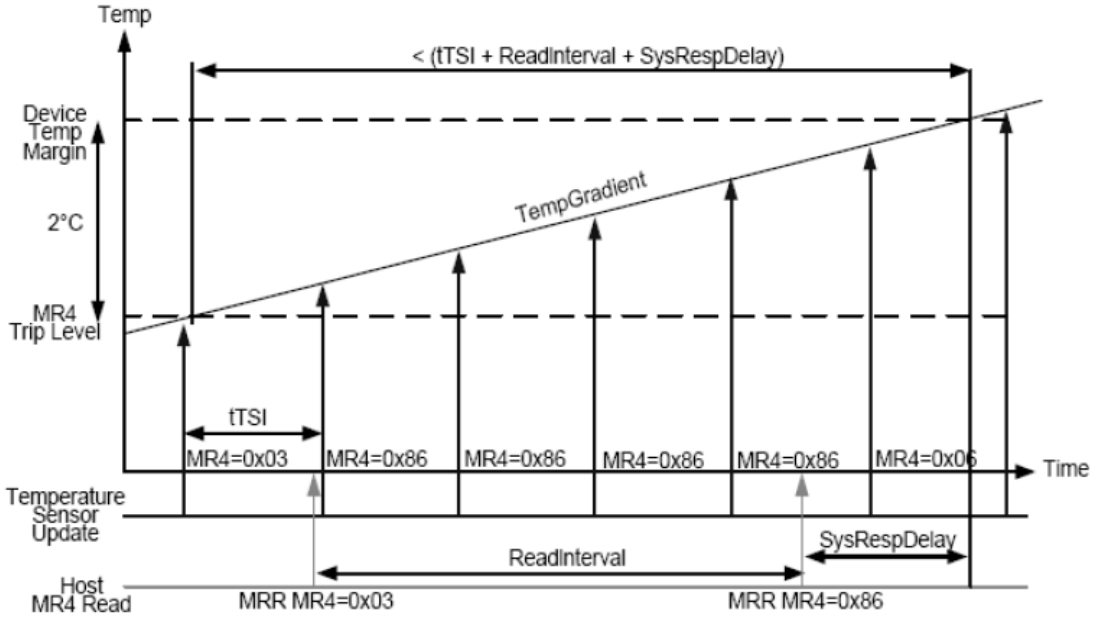
In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

TempGradient x (ReadInterval + tTSI + SysRespDelay) ≤ 2℃

For example, if TempGradient is 10℃/s and the SysRespDelay is 1 ms:

10℃/s * (ReadInterval+32ms+1ms) ≤ 2℃

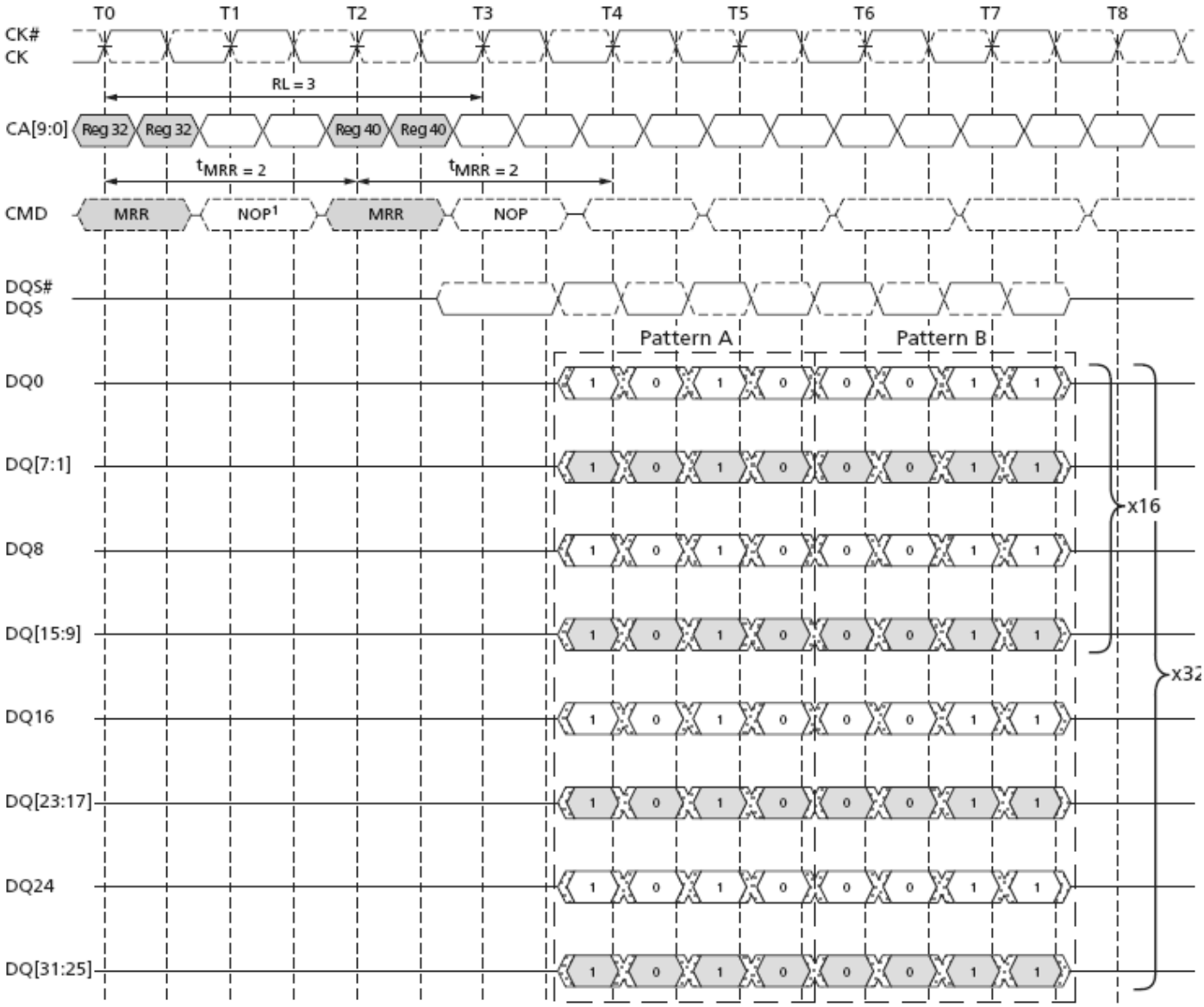
In this case, ReadInterval shall be no greater than 167ms.



DC Calibration

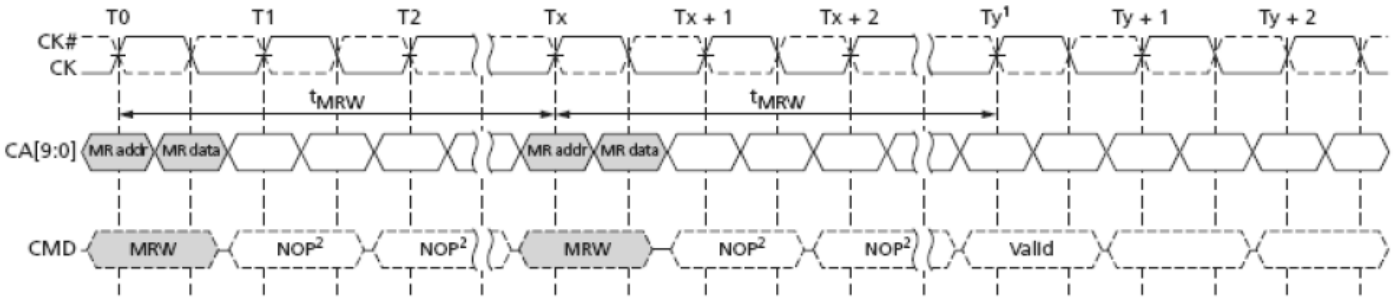
LPDDR2 devices feature a DQ calibration function that outputs one of two predefined system-timing calibration patterns. MRR to MR32 (pattern A) or MRR to MR40 (pattern B) will return the specified pattern on DQ0 and DQ8; and on DQ0, DQ8, DQ16, and DQ24 for x32 devices. For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Notes
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ callibration pattern
Pattern B	MR40	0	0	1	1	Reads to MR32 return DQ callibration pattern



Mode Register Write

The MRW command is used to write configuration data to mode registers. The MRW command is initiated with /CS LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.



Truth table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks idle	MRR	Mode Register Reading (All Banks idle)	All Banks idle
	MRW	Mode Register Writing (All Banks idle)	All Banks idle
	MRW (Reset)	Restting (Device Auto-Init)	All Banks idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) idle)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (Reset)	Not Allowed	Not Allowed

Mode Register Write Reset

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during tINIT4. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

Mode Register Write ZQ Calibration Command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration. LPDDR2-S2 devices do not support ZQ calibration; the ZQ CALIBRATION command is ignored by these devices. There are four ZQ calibration commands and related timings: tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is for initialization calibration; tZQRESET is for resetting ZQ to the default output impedance; tZQCL is for long calibration(s); and tZQCS is for short calibration(s).

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR2-S4. ZQINIT provides an output impedance accuracy of ±15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system. The ZQ reset

command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters. LPDDR2 devices are subject to temperature drift rate (TdriftrateE) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

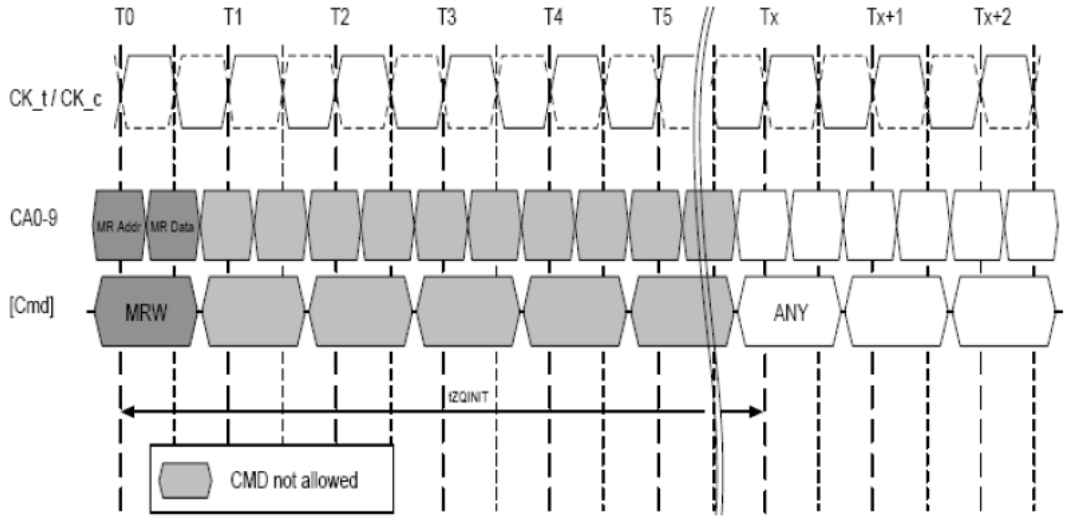
$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where Tsens = max(dRONdT) and Vsens = max(dRONdV), define the LPDDR2 temperature and voltage sensitivities. For example, if Tsens = 0.75% / C, Vsens = 0.20% / mV, Tdriftrate = 1 C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

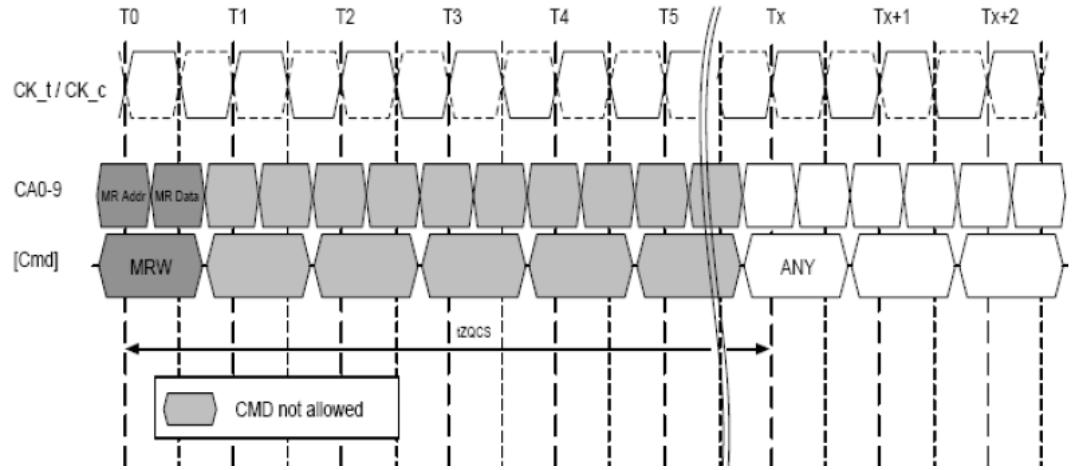
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

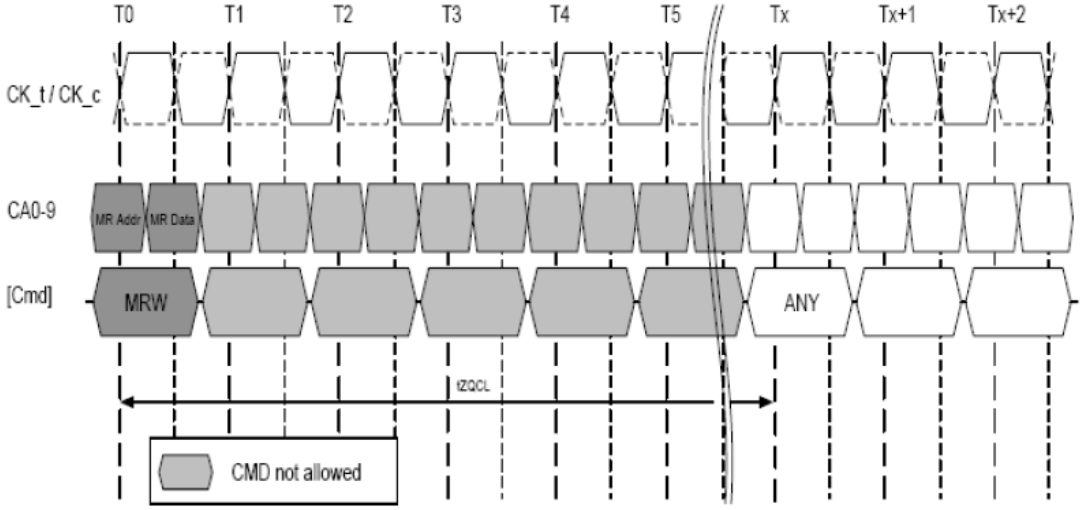
In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 shall ignore ZQ calibration commands and the device will use the default calibration settings.



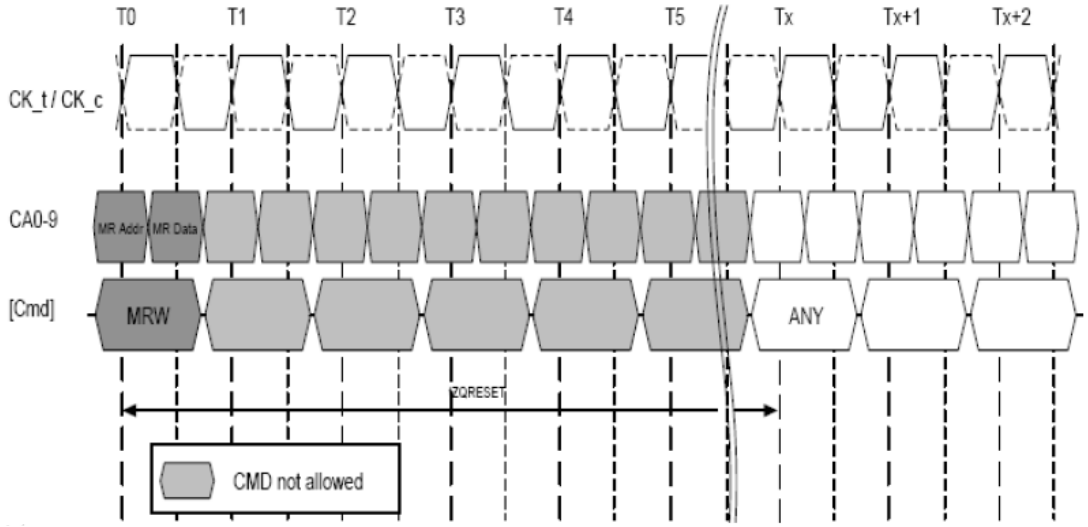
Notes: ZQ Calibration initialization timing example



Notes: ZQ Calibration short timing example



Notes: ZQ Calibration long timing example



Notes: ZQ Calibration reset timing example

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected

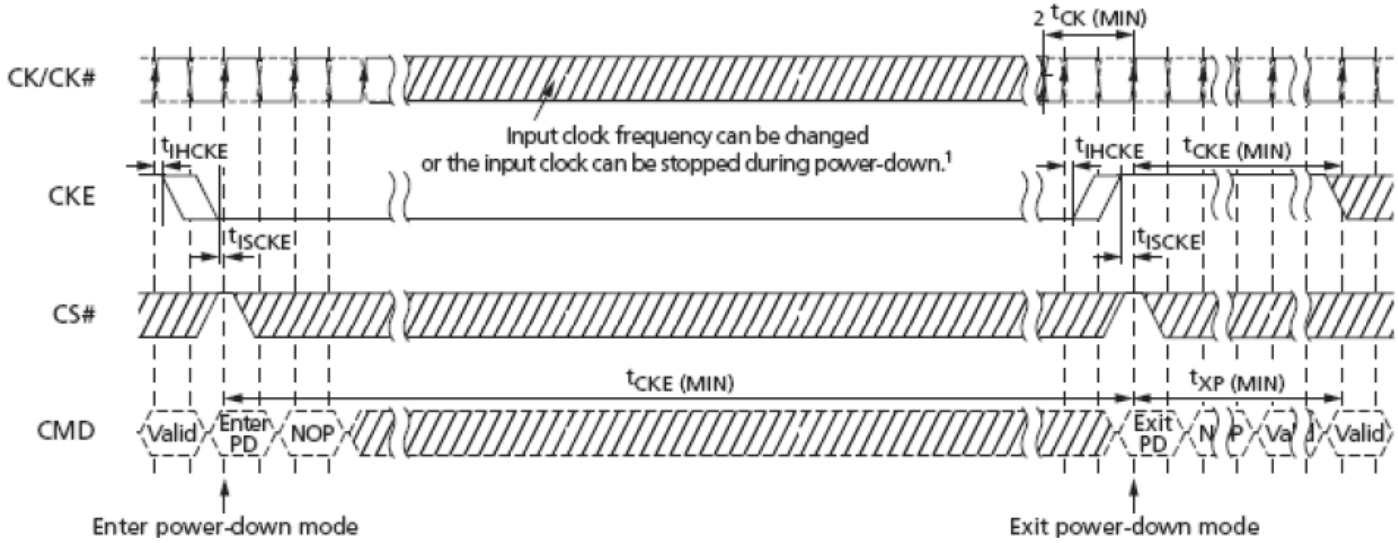
between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited.

Power-down

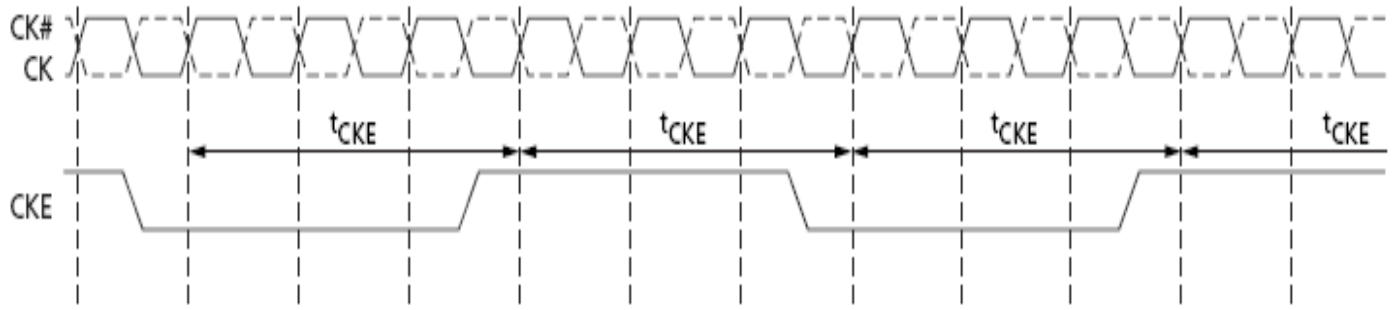
For Power-down is entered synchronously when CKE is registered LOW and /CS is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in bellow

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK, and CKE. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until tCKE is satisfied. VREFCA must be maintained at a valid level during power-down.

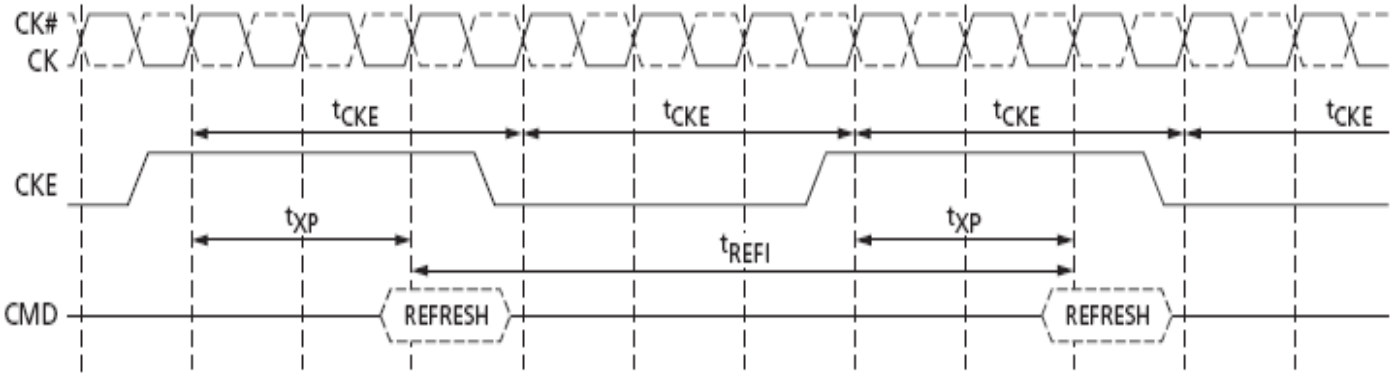
VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges. No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in section REFRESH Command. The power-down state is exited when CKE is registered HIGH. The controller must drive /CS HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH.



Notes: Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of 2 stable clocks complete.

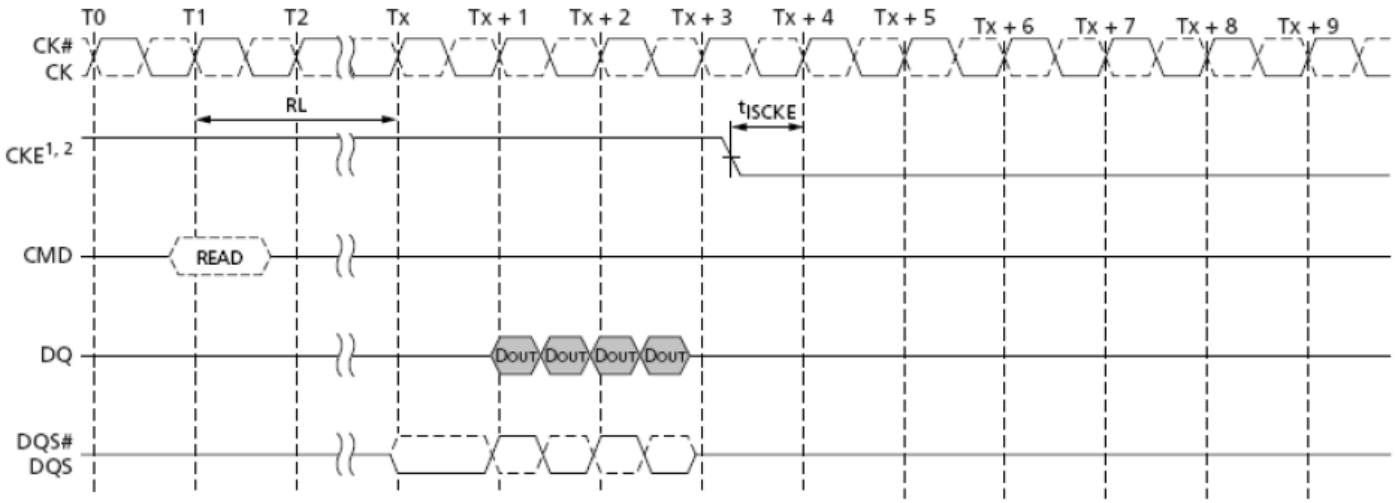


Notes: CKE intensive environment



Notes:

1. REF to REF timing in CKE intensive environment
2. The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRM guarantees all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

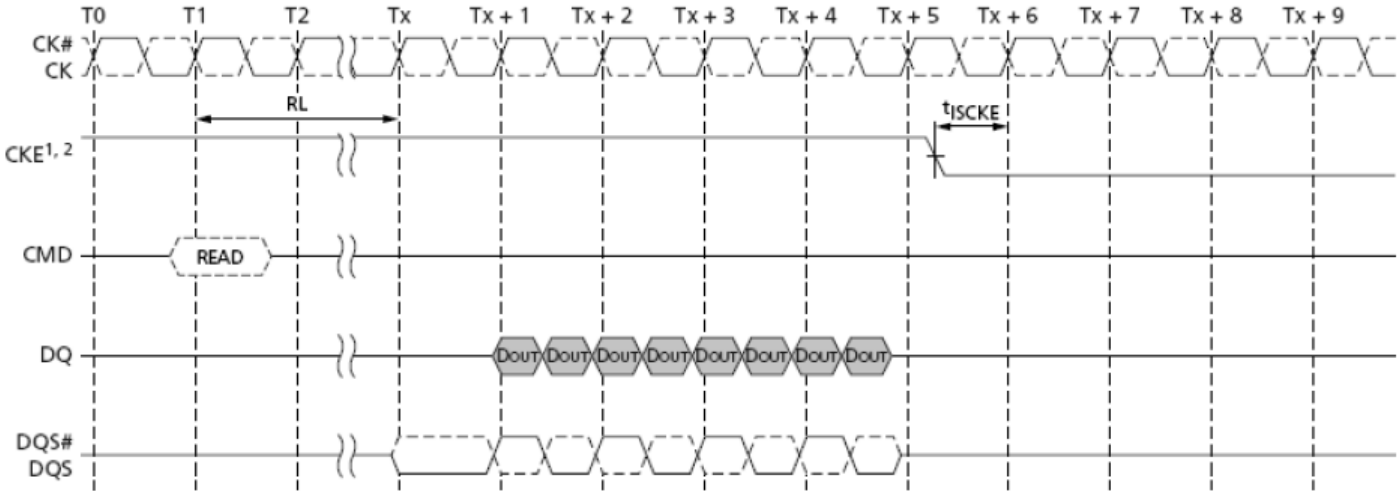


Notes:

1. Read to Power-down entry, BL=4.

2. CKE must be held high until the end of the burst operation.

3. CKE maybe registered low RL+RU(tDQSCK(MAX)/tCK)+BL/2+1 clock cycles after the clock on which the read command is registered.

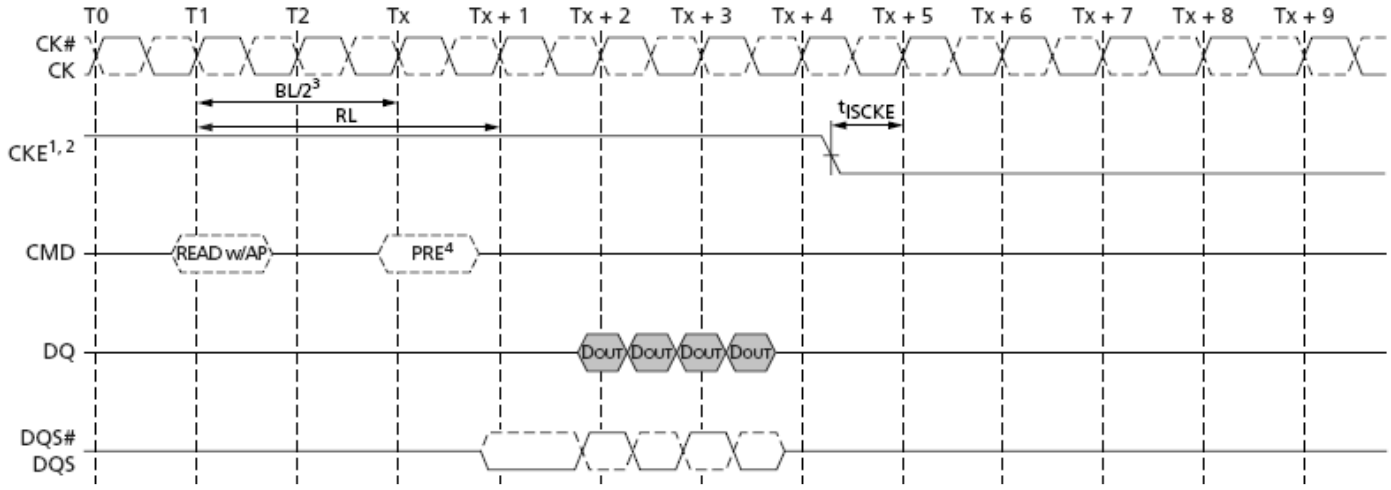


Notes:

1. Read to Power-down entry, BL=8.

2. CKE must be held high until the end of the burst operation.

3. CKE maybe registered low RL+RU(tDQSCK(MAX)/tCK)+BL/2+1 clock cycles after the clock on which the read command is registered.



Notes:

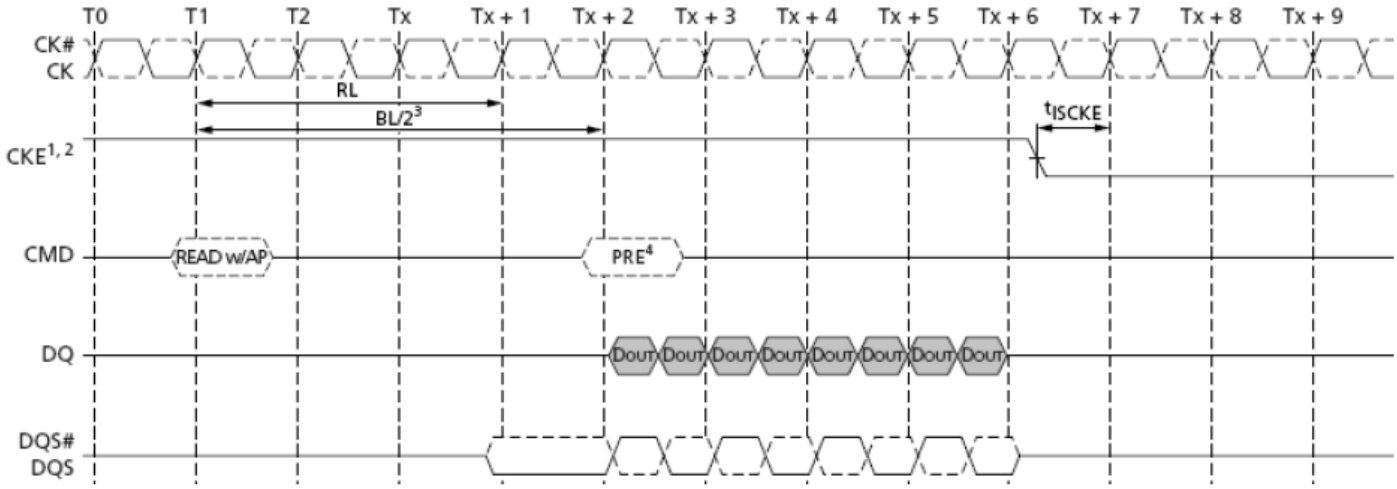
1. Read with auto-precharge to power-down entry, BL=4.

2. CKE must be held high until the end of the burst operation.

3. CKE can be registered LOW at RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.

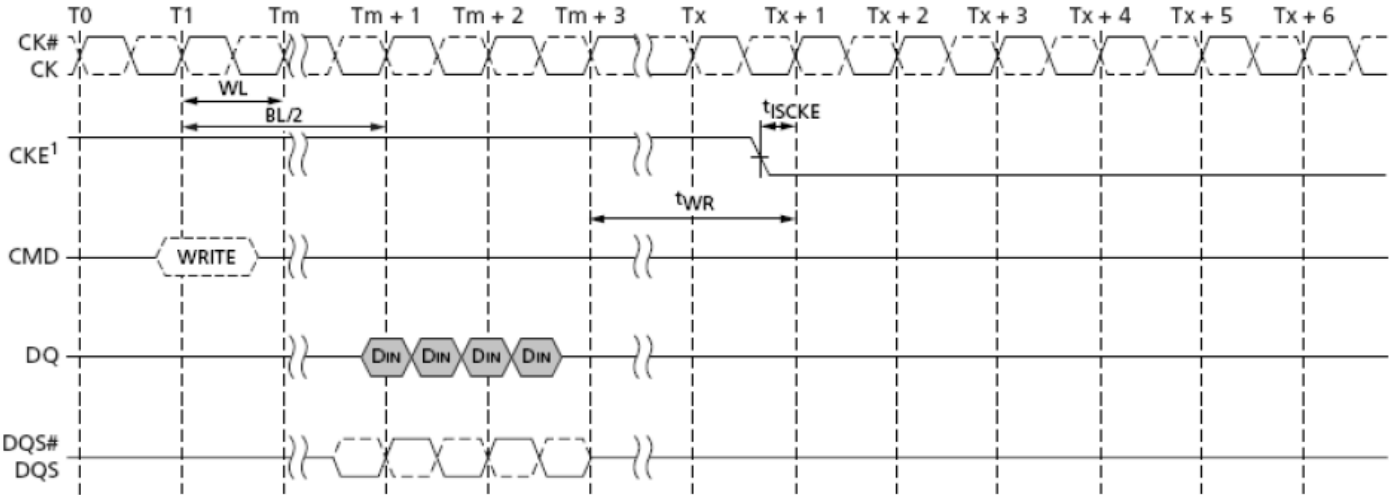
4. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.

5. Start internal PRECHARGE.



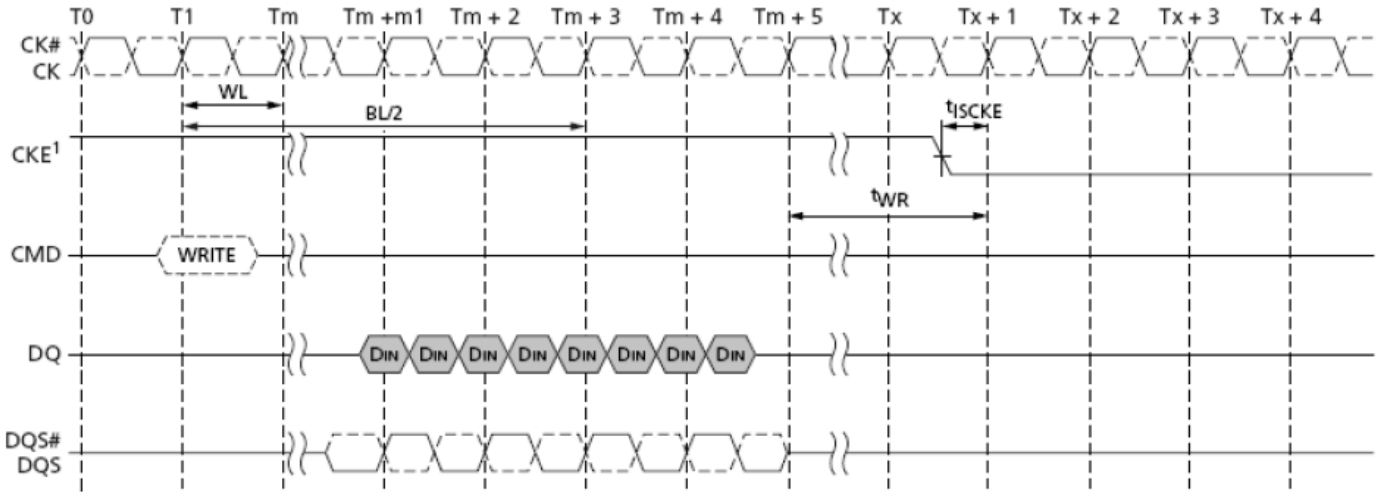
Notes:

1. Read with auto-precharge to power-down entry, BL=8.
2. CKE must be held high until the end of the burst operation.
3. CKE can be registered LOW at RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.
4. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
5. Start internal PRECHARGE.



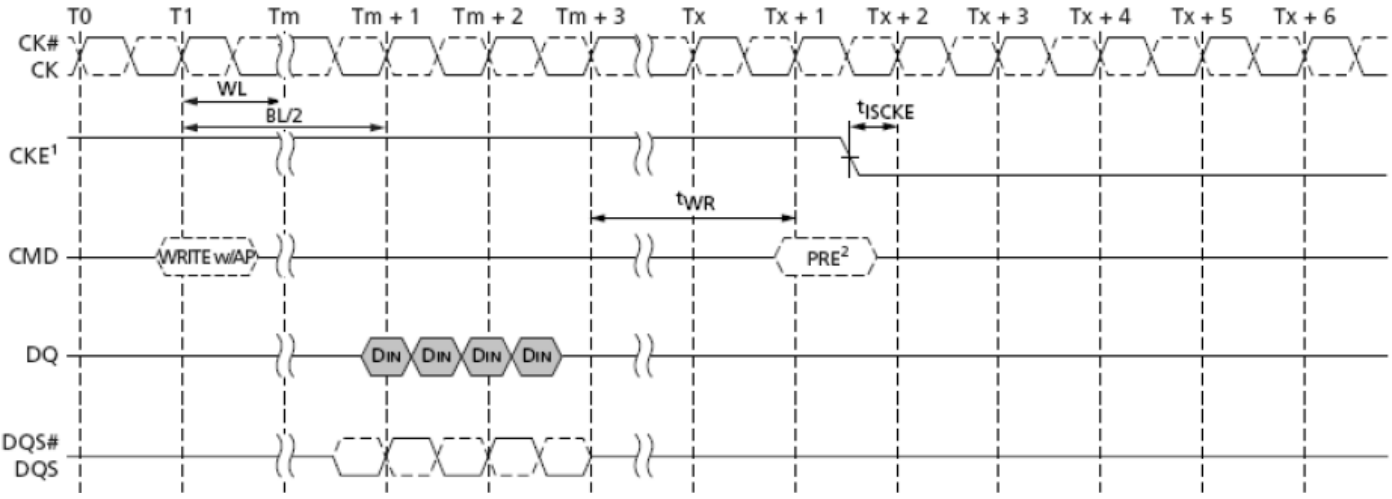
Notes:

1. Write to power-down entry, BL=4.
2. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the WRITE command is registered.



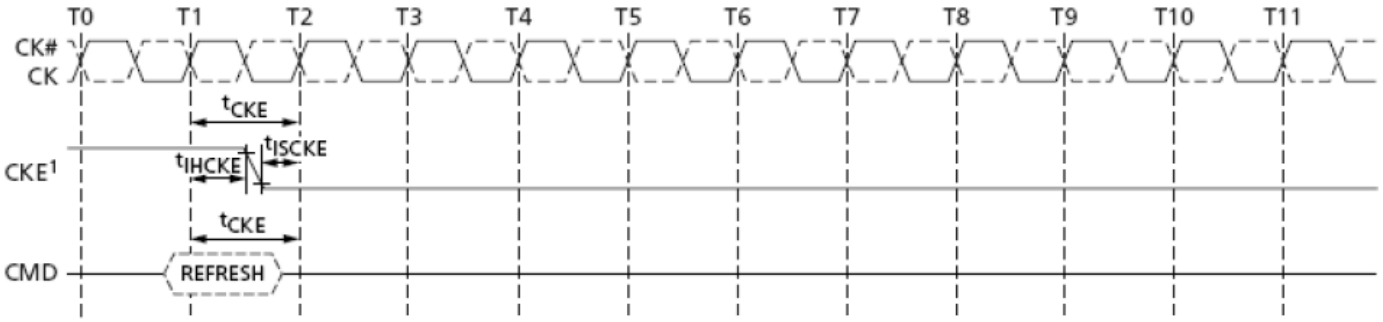
Notes:

1. Write to power-down entry, BL=8.
2. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the WRITE command is registered.



Notes:

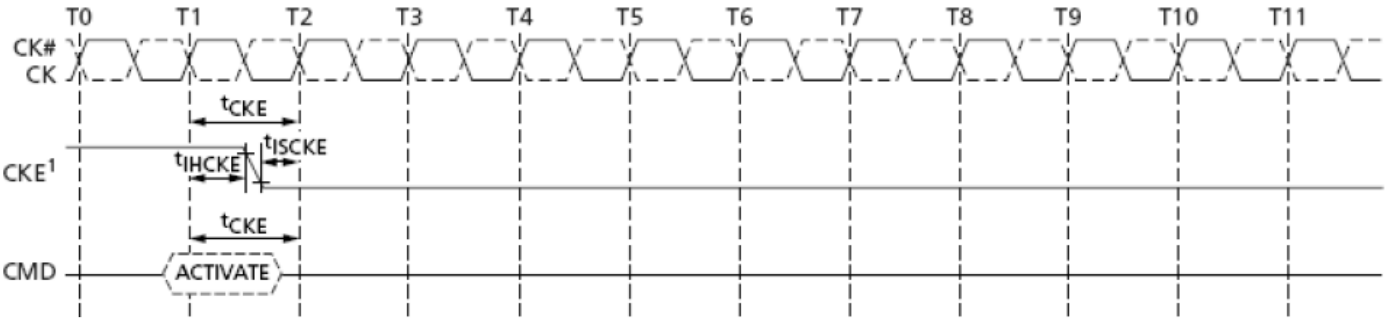
1. Write with auto-precharge to power-down entry, BL=4.
2. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK)+1 clock cycles after the clock on which the WRITE command is registered.
3. Start internal PRECHARGE.



Notes:

1. Refresh command to power-down entry.

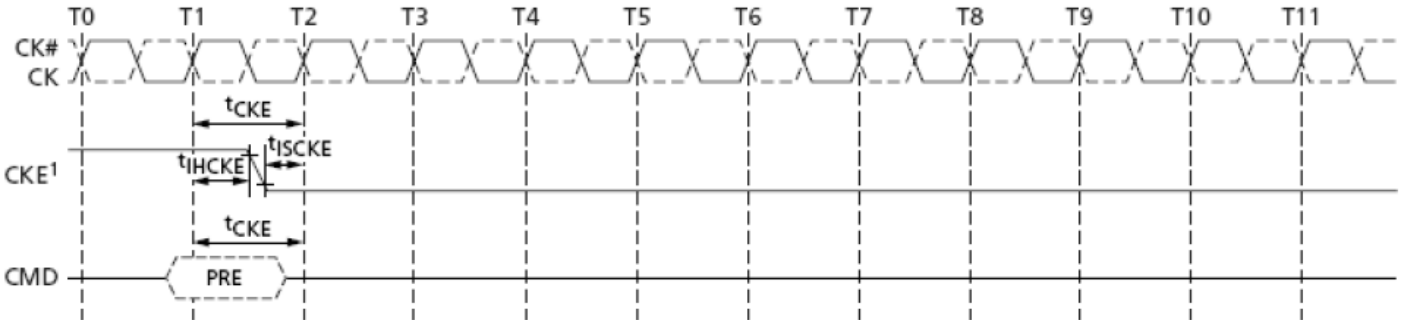
2. CKE may go LOW tIHCKE after the clock on which the refresh command is registered.



Notes:

1. Activate command to power-down entry.

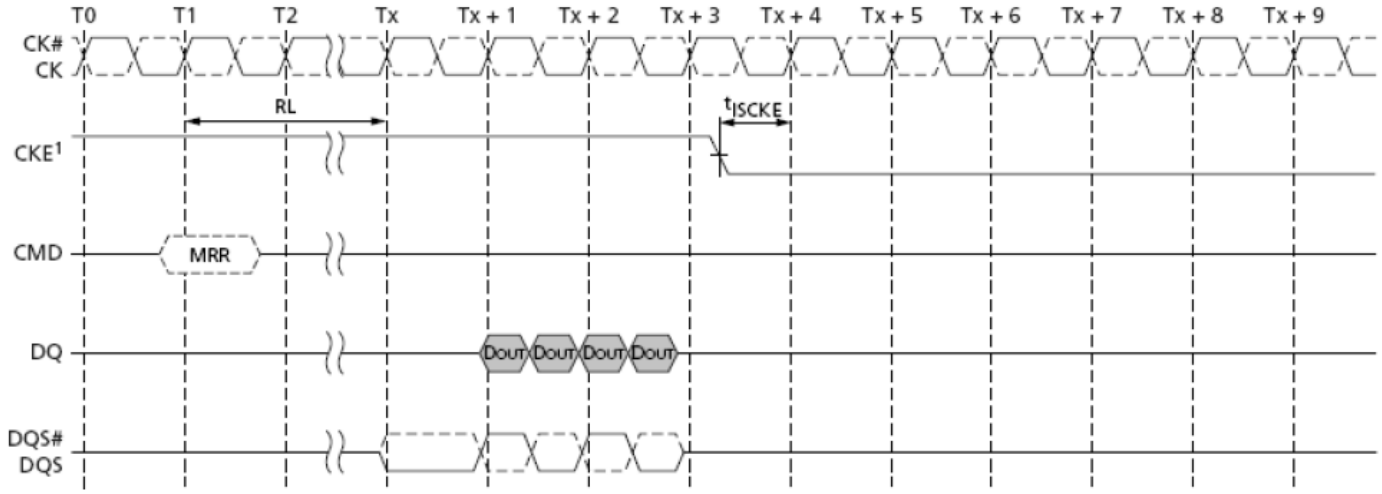
2. CKE may go LOW tIHCKE after the clock on which the activate command is registered.



Notes:

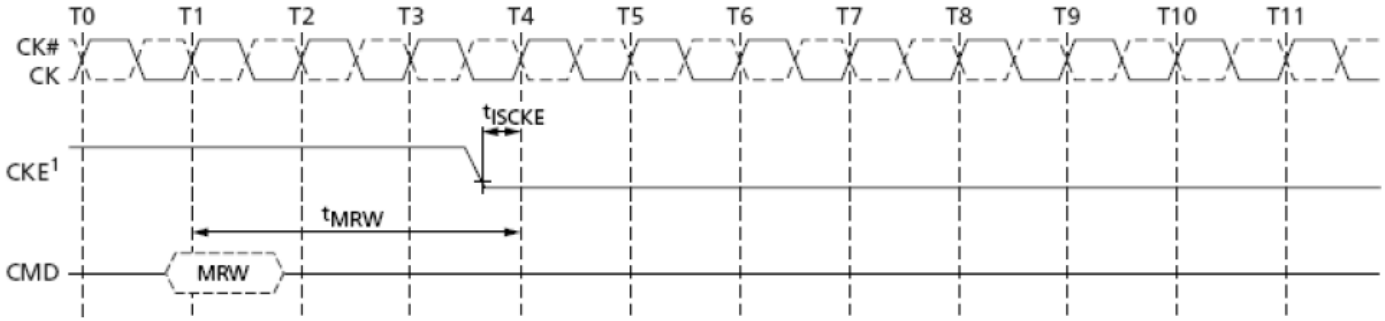
1. Precharge command to power-down entry.

2. CKE may go LOW tIHCKE after the clock on which the precharge command is registered.



Notes:

1. Mode Register Read to power-down entry.
2. CKE maybe registered Low RL+RU(tDQSCK/tCK)+BL/2+1 clock cycles after the clock on which the Mode Register Read command is registered.



Notes:

1. Mode Register Write to power-down entry.
2. CKE maybe registered LOW tMRW after the clock on which the Mode Register Write command is registered.

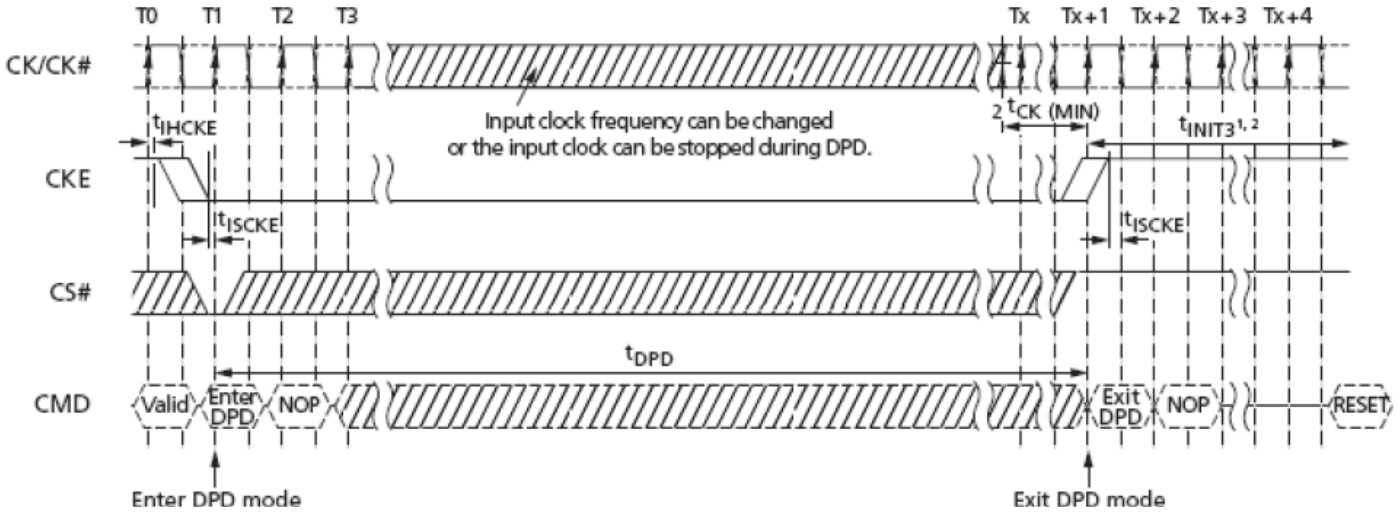
Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, auto-precharge, or Refresh is in progress, but deep power-down IDD spec will not be applied until finishing those operations.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum

levels. However prior to exiting Deep Power-Down, Vref must be within specified limits.

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode. The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.



Input Clock Stop and Frequency Change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

1. tCK(MIN) and tCK(MAX) are met for each clock cycle.
2. Refresh Requirements apply during clock frequency change.
3. During clock frequency change, only REFab or REFpb commands may be executing.
4. Any Activate, or Precharge commands have executed to completion prior to changing the frequency.
5. The related timing conditions (tRCD, tRP) have been met prior to changing the frequency.
6. The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW.
7. The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. Refresh Requirements apply during clock stop.
3. During clock stop, only REFab or REFpb commands may be executing.
4. Any Activate, or Precharge commands have executed to completion prior to stopping the clock.
5. The related timing conditions (tRCD, tRP) have been met prior to stopping the clock.
6. The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW.
7. The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

1. tCK(MIN) and tCK(MAX) are met for each clock cycle.
2. Refresh Requirements apply during clock frequency change.
3. Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency.
4. The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency.
5. CS_n shall be held HIGH during clock frequency change.
6. During clock frequency change, only REFab or REFpb commands may be executing.
7. The LPDDR2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. CS_n shall be held HIGH during clock clock stop.
3. Refresh Requirements apply during clock stop.
4. During clock stop, only REFab or REFpb commands may be executing;
5. Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock.
6. The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock.
7. The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

NOP Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Mode Register Definition

Mode Register Assignment and Definition

Each register is denoted as R, if it can be read but not written, W if it can be written but not read, and R/W if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00H	Device Info.	R	(RFU)						DI	DAI
1	01H	Device Feature1	W	nWR (for AP)			WC	BT	BL		
2	02H	Device Feature2	W	(RFU)					RL & WL		
3	03H	I/O Config-1	W	(RFU)					DS		
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06H	Basic Config-2	R	Revision ID1							

7	07H	Basic Config-3	R	Revision ID2		
8	08H	Basic Config-4	R	I/O width	Density	Type
9	09H	Test Mode	W	Vendor-Specific Test Mode		
10	0AH	IO Calibration	W	Calibration Code		
11~15	0BH~0FH	(reserved)		(RFU)		
16	10H	PASR_BANK	W	Bank Mask		
17	11H	PASR_Seg	W	Segment Mask		
18-19	12H-13H	(Reserved)		(RFU)		
20-31	18H-1FH	Reserved for NVM				
32	20H	DQ calibration pattern A	R	See Data Calibration Pattern Description		
33-39	21H-27H	(Do Not Use)				
40	28H	DQ calibration pattern B	R	See Data Calibration Pattern Description		
41-47	29H-2FH	(Do Not Use)				
48-62	30H-3EH	(Reserved)		(RFU)		
63	3FH	Reset	W	X		
64-126	40H-7EH	(Reserved)		(RFU)		
127	7FH	(Do Not Use)				
128-190	80H-BEH	(Reserved for Vendor Use)		(RFU)		
191	BFH	(Do Not Use)				
192-254	C0H-FEH	(Reserved for Vendor Use)		(RFU)		
255	FFH	(Do Not Use)				

Notes:

1. RFU bits shall be set to 0 during Mode Register writes.
2. RFU bits shall be read as 0 during Mode Register reads.
3. All Mode Registers from that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Devcie Information (MA<7:0> = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)						DI	DAI	
OP1		DI (Device Information)				Read-only		0B: S4 SDRAM
								1B: Do Not Use
OP0		DAI (Device Auto-Initialization Status)				Read-only		0B: DAI complete
								1B: DAI still in progress

MR1_Devcie Feature 1 (MA<7:0> = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
nWR (for AP)			WC	BT	BL			
OP<2:0>		BL (Burst Length)				Write-only		010B: BL4 (default)
								011B: BL8
								100B: BL16
								All others: reserved
OP3		BT*1 (Burst Type)				Write-only		0B: Sequential (default)
								1B: Interleaved
OP4		WC (Wrap)				Write-only		0B: Wrap (default)
								1B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>		nWR*2				Write-only		001B: nWR=3 (default)
								010B: nWR=4
								011B: nWR=5
								100B: nWR=6
								101B: nWR=7
								110B: nWR=8
								All others: reserved

Notes:

1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled.

Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	0B	0B	wrap	any	4	0	1	2	3												
x	x	1B	0B				2	3	0	1												
x	x	x	0B	nw	any		y	y+1	y+2	y+3												
C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	0B	0B	0B	wrap	seq	8	0	1	2	3	4	5	6	7								
x	0B	1B	0B				2	3	4	5	6	7	0	1								
x	1B	0B	0B				4	5	6	7	0	1	2	3								
x	1B	1B	0B				6	7	0	1	2	3	4	5								
x	0B	0B	0B		int		0	1	2	3	4	5	6	7								
x	0B	1B	0B				2	3	0	1	6	7	4	5								
x	1B	0B	0B				4	5	6	7	0	1	2	3								
x	1B	1B	0B				6	7	4	5	2	3	0	1								
x	x	x	0B	nw	any		illegal (not allowed)															
0B	0B	0B	0B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B	0B	1B	0B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0B	1B	0B	0B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0B	1B	1B	0B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1B	0B	0B	0B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1B	0B	1B	0B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1B	1B	0B	0B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1B	1B	1B	0B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
x	x	x	0B		int		illegal (not allowed)															
x	x	x	0B	nw	any		illegal (not allowed)															

Notes :

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1~C0
3. For BL=8, the burst address represents C2~C0.
4. For BL=16, the burst address represents C3~C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown below.

Non-Wrap Restrictions

Width	4Gb
Cannot cross full page boundary	
X32	3FE, 3FF, 000, 001

Cannot cross sub-page boundary	
X32	none

Notes:

1. Non-wrap BL= 4 data orders shown are prohibited.

MR2_Devcie Feature 2 (MA<7:0> = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				RL & WL				
OP<3:0>		RL & WL (Read Latency & Write Latency)				Write-only		0001B: RL3 / WL1 (default)
								0010B: RL4 / WL2
								0011B: RL5 / WL2
								0100B: RL6 / WL3
								0101B: RL7 / WL4
								0110B: RL8 / WL4
								All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				DS				
OP<3:0>		DS (Drive Strength)				Write-only		0000B: reserved
								0001B: 34.3 ohm typical
								0001B: 34.3 ohm typical
								0010B: 40.0 ohm typical (default)
								0011B: 48.0 ohm typical
								0100B: 60.0 ohm typical
								0101B: reserved
								0110B: 80.0 ohm typical
								All others: reserved

MR4_Device Temperature (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
TUF	(RFU)				SDRAM Refresh Rate			
OP<2:0>	SDRAM Refresh Rate					Read-only		000B: 4 x tREFI, SDRAM Low Temp. operating limit exceeded
								001B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW,
								010B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW,
								011B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW (<= 85C)
								100B: RFU
								101B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, don't re-rate SDRAM AC timing
								110B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, derate SDRAM AC timing
								111B: SDRAM High temperature operating limit exceeded
OP7	TUF (Temperature Update Flag)					Read-only		0B: OP<2:0> value has not changed since last read of MR4.
								1B: OP<2:0> value has changed since last read of MR4.

Notes:

1. A Mode Register Read from MR4 will reset OP7 to 0.
2. OP7 is reset to 0 at power-up.
3. If OP2 equals 1, the device temperature is greater than 85C.
4. OP7 is set to 1, if OP2~OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP<2:0> = 000B or 111B.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. The tDQSCK parameter must be derated .. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in Temperature Sensor.

MR5_Basic Configuration 1 (MA<7:0> = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
LPDDR2 Manufacturer ID								

MR6_Basic Configuration 2 (MA<7:0> = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID1								
OP<7:0>	Revision ID1					Read-only		00000000B: A-version

MR7_Basic Configuration 3 (MA<7:0> = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID2								
OP<7:0>	Revision ID2					Read-only		00000000B: A-version

MR8_Basic Configuration 4 (MA<7:0> = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
I/O width		Density				Type		
OP<1:0>		Type				Read-only		00B: S4 SDRAM
								01B: S2 SDRAM
								10B: N NVM
								11B: Reserved
OP<5:2>		Density				Read-only		0000B: 64Mb
								0001B: 128Mb
								0010B: 256Mb
								0011B: 512Mb
								0100B: 1Gb
								0101B: 2Gb
								0110B: 4Gb
								0111B: 8Gb
								1000B: 16Gb
								1001B: 32Gb
								0101B: 2Gb
								All others: reserved
OP<7:6>		I/O width				Read-only		00B: x32
								01B: x16
								10B: x8
								11B: not used

MR9_Test Mode (MA<7:0> = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Vendor-specific Test Mode								

MR10_Calibration (MA<7:0> = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	

Calibration Code			
OP<7:0>	Calibration Code	Write-only	0xFF: Calibration command after initialization
			0xAB: Long calibration
			0x56: Short calibration
			0xC3: ZQ Reset
			All others: Reserved

Notes:

1. Host processor shall not write MR10 with Reserved values.
2. LPDDR2 devices shall ignore calibration command, when a Reserved values is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see MRW ZQ Calibration Command) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. Devices that do not support calibration ignore the ZQ calibration command.

MR11:15_(Reserved) (MA<7:0> = 0BH- 0FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR16_PASR_Bank Mask (MA<7:0> = 010H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	

Bank Mask (4-Bank or 8-Bank)			
OP<7:0>	Bank Mask Code	Write-only	0B: refresh enable to the bank (=unmasked, default)
			1B: refresh blocked (=masked)

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Segment Mask								
OP<7:0>		Segment Mask Code			Write-only			0B: refresh enable to the bank (=unmasked, default)
								1B: refresh blocked (=masked)

Segment	OP	Bank Mask	4Gb
			R13:11
0	0	XXXXXXX1	000B
1	1	XXXXXX1X	001B
2	2	XXXXX1XX	010B
3	3	XXXX1XXX	011B
4	4	XXX1XXXX	100B
5	5	XX1XXXXX	101B
6	6	X1XXXXXX	110B
7	7	1XXXXXXX	111B

MR18:19_(Reserved) (MA<7:0> = 012H- 013H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	

RFU	

MR20:47_(Do Not Use) (MA<7:0> = 014H- 02FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do not use								

MR48:62_(Reserved) (MA<7:0> = 030H- 03EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR63_Reset (MA<7:0> = 03FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
X								

MR64:126_(Reserved) (MA<7:0> = 040H- 07EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR127_(Do Not Use) (MA<7:0> = 07FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do not use								

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 080H- 0BEH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR191_(Do Not Use) (MA<7:0> = 0BFH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do not use								

MR192:254_(Reserved for Vendor Use) (MA<7:0> = 0C0H- 0FEH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR255_(Do Not Use) (MA<7:0> = 0FFH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do not use								

Command Truth Table

Command	Command Pin			CA Pins										CLK Edge
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CLK t(n-1)	CLK t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
				MA6	MA7	X								
Refresh (per bank)	H	H	L	L	L	H	L	X						
				X										
Refresh (all bank)	H	H	L	L	L	H	H	X						
				X										
Enter Self Refresh	H	L	L	L	L	H	X							
				X										
Activate	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
Write	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
				AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Read	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
				AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
Precharge	H	H	L	H	H	L	H	AB	X		BA0	BA1	BA2	
				X										
BST	H	H	L	H	H	L	L	X						
				X										
Enter Deep Power Down	H	L	L	H	H	L	X							
				X										
NOP	H	H	L	H	H	H	X							
				X										
Maintain PD, SREF, DPD	H	H	H	X										
				X										
NOP	H	H	H	X										
				X										
Maintain PD, SREF, DPD	L	L	H	X										
				X										
Enter Power Down	H	L	H	X										
				X										
Exit PD, SREF, DPD	L	H	H	X										
				X										

Notes:

1. All LPDDR2ccommands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP high during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. x means H or L (but a defined logic level).
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self Refresh and Deep Down operation.
7. CAxr refers to command/address bit x on the rising edge of clock.

8. CAxf refers to command/address bit x on the rising edge of clock.

9. CS and CKE are sampled at the rising edge of clock.

10. Per Bank Refresh is only allowed in devices with 8 banks.

11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

CKE Truth Table

Current State	CKE t(n-1)	CKE t(n)	CS	Command	Operation	Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	X	X	Maintain Resertting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Enter Self-Refresh	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:

1. CKE t(n) is the logic state of CKE at clock edge t(n); CKE t(n-1) was the logic state of CKE at previous clock edge.

2. CS is the logic state of CS at the clock rising edge n.

3. Current state is the state of the LPDDR2 device immediately prior to clock edge n.

4. Command n is the command registered at clock edge N, and Operation n is a result of Command n.

5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.

7. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.

8. The Deep Power-Down exit procedure must be followed as discussed in the DPD section of the Functional Description.

9. The clock must toggle at least once during the tXP period.

10. The clock must toggle at least once during the tXSR period.

11. x means don’t care.

12. Upon exiting Resetting Power Down, the device will return to the idle state if tINIT5 has expired.

Current State Bank n – Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (AllBank)	7
	MRW	Load value from Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle / MR Reading	
	Reset	Begin Device Auto-initialization	Resetting	7,8
	Precharge	Deactivate row in bank or banks	Precharging	9,15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active / MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKE t(n-1) and CKE t(n) are HIGH, and after tXSR or tXP has been met, if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

   Idle: The bank or banks have been precharged, and tRP has been met.

   Active: A row in the bank has been activated, and tRCD has been met. No data bursts or accesses and no register accesses are in progress.

   Reading: A READ burst has been initiated with auto precharge disabled, and has not yet terminated or been terminated.

   Writing: A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should been issued on any clock edge occurring during these states.

   Refreshing (per bank): start with registration of a REFRESH (per bank) command and ends when tRFCpb is met. After tRFCpb is met, the bank is in the idle state.

   Refreshing (all bank): start with registration of a REFRESH (all bank) command and ends when tRFCab is met. After tRFCab is met, the device is in the all banks idle state.

Idle MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in all banks idle state.

Resetting MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in all banks idle state.

Active MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the bank is in the active state.

MR writing: start with registration of the MRW command and ends when tMRW is met. After tMRW is met, the device is in the all banks idle state.

Precharge all: start with registration of PRECHARGE command and ends when tRP is met. After tRP is met, the device is in the all banks idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

   Precharging: start with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank is in the idle state.

   Row Active: start with registration of an ACTIVATE command and ends when tRCD is met. After tRCD is met, the bank is in the active state.

   Read with AP enable: start with registration of a READ command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

   Write with AP enable: start with registration of a WRITE command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, the must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.
11. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Current State Bank n – Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	–	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10,11,13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	8,16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	8,15
	Write	Select column, and start write burst to Bank m	Writing	8,14,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	8,15,16
	Write	Select column, and start write burst to Bank m	Writing	8,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-initialization	Resetting	12,17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKE t(n-1) and CKE t(n) are HIGH, and after tXSR or tXP has been met, if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

   Idle: the bank has been precharge and rRP is met.

   Active: A row in the bank has been activated and tRCD is met and data burst/accesses and no register accesses are in progress.

   Reading: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.

   Writing: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.
4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command can't be issued to another bank; it applies to the bank represented by the current state only.

6. The following states must not be interrupted by any executable command; NOP command must be applied during each clock cycle while in these states:

   Idle MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in all banks idle state.

   Resetting MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in all banks idle state.

   Active MR reading: start with registration of the MRR command and ends when tMRR is met. After tMRR is met, the bank is in the active state.

   MR writing: start with registration of the MRW command and ends when tMRW is met. After tMRW is met, the device is in the all banks idle state.

7. BST is supported only if a READ or WRITE burst is on-going.
8. tRRD must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m.
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enable.
10. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank *m* depends on the current state of bank *m* (idle, row-activating, precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

DM Operation Truth Table

Function	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

Notes:

1. Used to mask write data, provided coincident with the corresponding data.

Electrical Specifications

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units
VDD1	Voltage on VDD1 pin relative to Vss	-0.4	2.3	V
VDD2	Voltage on VDD2 pin relative to Vss	-0.4	1.6	V
VDDCA	Voltage on VDDCA pin relative to Vss	-0.4	1.6	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4	1.6	V
Vin, Vout	Voltage on any pin relative to Vss	-0.4	1.6	V
Tstg	Storage Temperature (plastic)	RT	85	C

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD2 and VDDQ / VDDCA must be within 200mV of each other at all times.
3. Voltage on any I/O may not exceed voltage on VDDQ; Voltage on any CA input may not exceed voltage on VDDCA.
4. VREF must always be less than all other supply voltages.
5. The voltage difference between any VSS, VSSQ, or VSSCA pins may not exceed 100mV.
6. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JESD51-2 standard.

Input / Output Capacitance

Symbol	Parameter	LPDDR2 1066-466		LPDDR2 400-200		
		Min	Max	Min	Max	Unit
CCK	Input capacitance: CK, /CK	1	2	1	2	pF
CDCK	Input capacitance delta: CK, /CK	0	0.2	0	0.25	pF
CI	Input capacitance: all other input-only pins	1	2	1	2	pF
CDI	Input capacitance delta: all other input-only pins	-0.4	0.4	-0.5	0.5	pF
CIO	Input/output capacitance: DQ, DQS, /DQS, DM	1.25	2.5	1.25	2.5	pF
CDDQS	Input/output capacitance delta: DQS, /DQS	0	0.25	0	0.3	pF
CDIO	Input/output capacitance delta: DQ, DM	-0.5	0.5	-0.6	0.6	pF
CZQ	Input/output capacitance: ZQ	0	0.25	0	0.25	pF

Notes:

1. VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95 LPDDR2-S4A VDD2= 1.28-1.42V
2. Absolute value of CCK - /CCK.
3. CI applies to /CS, CKE, and CA[9:0].
4. CDI = CI - 0.5 × (CCK + /CCK)
5. DM loading matches DQ and DQS.
6. MR3 I/O configuration DS OP[3:0] = 0001B (34.3 ohm typical)
7. Absolute value of CDQS and /CDQS.
8. CDIO = CIO - 0.5 × (CDQS + /CDQS) in byte-lane.
9. Maximum external load capacitance on ZQ pin: 5pF.
10. This parameter applies to die devices only (does not include package capacitance).
11. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, VSS, VSSCA, and VSSQ applied; all other pins are left floating.

Temperature Range

Symbol	Parameter / Condition	Min	Norm	Max	Unit	Notes
Tj	Junction Temperature	RT	–	85	C	

AC/DC Electrical Characteristics and Operating Conditions

DC Electrical Characteristics and Operating Conditions

Power Supply

Symbol	Parameter	Min	Norm	Max	Unit	Notes
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V	
V_{DD2}	Core Supply voltage 2 (S4A)	–	–	–	V	1
	Core Supply voltage 2 (S4B)	1.14	1.20	1.30	V	1
V_{DDCA}	Input Supply Voltage (Command / Address)	1.14	1.20	1.30	V	1
V_{DDQ}	I/O Supply voltage (DQ)	1.14	1.20	1.30	V	1
V_{REFCA}(DC)	Input reference voltage (Command / Address)	0.49 x V_{DDCA}	0.50 x V_{DDCA}	0.51 x V_{DDCA}	V	2
V_{REFDQ}(DC)	Input reference voltage (DQ)	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2

Leakage current

Symbol	Parameter	Min	Norm	Max	Unit	Notes
I_I	Input leakage current Any input 0 ≦ VIN ≦ VDDQ / VDDCA, All other pins not under test = 0V	-2	–	2	uA	
I_{VREF}	V_{REF} leakage current; V_{REFDQ} = V_{DDQ}/2 or V_{REFCA} = V_{DDCA}/2 (all other pins not under test = 0V)	-1	–	1	uA	

AC/DC Input Operating Conditions

CA inputs (Address and Command) and /CS inputs

Symbol	Parameter	LPDDR2 1066-400		LPDDR2 400-200		Unit	Notes
			Max	Min	Max		
$V_{IHCA(AC)}$	AC Input logic HIGH voltage	V_{REFCA} +220mV	–	V_{REFCA} +300mV	–	mV	
$V_{IHCA(DC)}$	DC Input logic HIGH voltage	V_{REFCA} +130mV	V_{DDCA}	V_{REFCA} +200mV	V_{DDCA}		
$V_{ILCA(AC)}$	AC Input logic LOW voltage	–	V_{REFCA} -220mV	–	V_{REFCA} -300mV	mV	
$V_{ILCA(DC)}$	DC Input logic LOW voltage	V_{SSCA}	V_{REFCA} -130mV	V_{SSCA}	V_{REFCA} -200mV	mV	
$V_{REFCA(DC)}$	Reference voltage for CA and /CS inputs	0.49 x V_{DDCA}	0.51 x V_{DDCA}	0.49 x V_{DDCA}	0.51 x V_{DDCA}	mV	

Data inputs (DQ & DM)

Symbol	Parameter	LPDDR2 1066-400		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		

$V_{IHDQ(AC)}$	AC Input logic HIGH voltage	V_{REFDQ} +220mV	–	V_{REFDQ} +300mV	–	mV	
$V_{IHDQ(DC)}$	DC Input logic HIGH voltage	V_{REFDQ} +130mV	V_{DDQ}	V_{REFDQ} +200mV	V_{DDQ}		
$V_{ILDQ(AC)}$	AC Input logic LOW voltage	–	V_{REFDQ} -220mV	–	V_{REFDQ} -300mV	mV	
$V_{ILDQ(DC)}$	DC Input logic LOW voltage	V_{SSCA}	V_{REFDQ} -130mV	V_{SSQ}	V_{REFDQ} -200mV	mV	
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	0.49 x V_{DDQ}	0.51 x V_{DDQ}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	mV	

Clock enable inputs (CKE)

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHCKE (AC)}$	CKE AC Input HIGH voltage	0.8 * V_{DDCA}	–		
$V_{ILCKE (AC)}$	CKE AC Input LOW voltage	–	0.2 * V_{DDCA}		

Notes:

1. VDD2 and VDDQ/VDDCA must be within 200mV of each other all the times.
2. VDD and VDDQ must track each other and VDDQ must be less than or equal to VDD.
3. All parameters assume proper device initialization.
4. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
5. All voltages referenced to VSS.
6. The typical value of VOX (AC) is expected to be about 0.5 x VDDQ of the transmitting device and VOX (AC) is expected to track variations in VDDQ. VOX (AC) indicates the voltage at which differential output signals must cross.
7. VREFCA and VREFDQ are expected to equal VDDCA/2 and VDDQ/2, respectively, of the transmitting device and to track variations in the DC level of the same. Peak-to-Peak noise (non-common node) on VREFCA and VREFDQ may not exceed +/- 2% of the DC value. Peak-to-Peak AC noise on VREFCA and VREFDQ may not exceed +/- 2% of VREF (DC) value. This measurement is to be taken at the nearest VREFDQ or VREFCA bypass capacitor.

IDD Specifications

64Mx32 IDD Specifications; V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V, V_{DD1} = 1.70~1.95

Symbol		Supply	Value	Unit	Notes
IDD0	IDD01	VDD1	15	mA	
	IDD02	VDD2	70		
	IDD0IN	VDDCA + VDDQ	6		
IDD2P	IDD2P1	VDD1	600	uA	
	IDD2P2	VDD2	800		
	IDD2PIN	VDDCA + VDDQ	50		
IDD2PS	IDD2PS1	VDD1	600	uA	
	IDD2PS2	VDD2	800		
	IDD2PSIN	VDDCA + VDDQ	50		
IDD2N	IDD2N1	VDD1	2	mA	
	IDD2N2	VDD2	40		
	IDD2NIN	VDDCA + VDDQ	7		
IDD2NS	IDD2N1	VDD1	1.7	mA	
	IDD2N2	VDD2	40		
	IDD2SIN	VDDCA + VDDQ	6		
IDD3P	IDD3P1	VDD1	1200	uA	
	IDD3P2	VDD2	8	mA	
	IDD3PIN	VDDCA + VDDQ	150	uA	
IDD3PS	IDD3PS1	VDD1	1200	uA	
	IDD3PS2	VDD2	8	mA	
	IDD3PSIN	VDDCA + VDDQ	150	uA	
IDD3N	IDD3N1	VDD1	2.5	mA	
	IDD3N2	VDD2	30		
	IDD3NIN	VDDCA + VDDQ	6		
IDD3NS	IDD3N1	VDD1	2	mA	
	IDD3N2	VDD2	27		
	IDD3SIN	VDDCA + VDDQ	6		
IDD4R	IDD4R1	VDD1	3	mA	
	IDD4R2	VDD2	194		
	IDD4RIN	VDDCA	25		
	IDD4RQ	VDDQ	244		
IDD4W	IDD4W1	VDD1	10	mA	
	IDD4W2	VDD2	185		

	IDD4W IN	VDDCA + VDDQ	25		
IDD5	IDD51	VDD1	40	mA	
	IDD52	VDD2	150		
	IDD5IN	VDDCA + VDDQ	6		
IDD5AB	IDD5AB1	VDD1	5	mA	
	IDD5AB2	VDD2	18		
	IDD5ABIN	VDDCA + VDDQ	8		
IDD5PB	IDD5PB1	VDD1	5	mA	
	IDD5PB2	VDD2	50		
	IDD5PBIN	VDDCA + VDDQ	8		
IDD6	IDD61	VDD1	1000	uA	
	IDD62	VDD2	3200		
	IDD6IN	VDDCA + VDDQ	50		
IDD8	IDD81	VDD1	25	uA	
	IDD82	VDD2	100		
	IDD8IN	VDDCA + VDDQ	100		

IDD6 Partial Array Self-refresh current; V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V, V_{DD1} = 1.70~1.95

PASR	Supply	Value	Unit	Notes
Full Array	VDD1	1000	uA	
	VDD2	3200		
	VDDCA + VDDQ	50		
1/2 Array	VDD1	950		
	VDD2	2700		
	VDDCA + VDDQ	50		
1/4 Array	VDD1	900		
	VDD2	2400		
	VDDCA + VDDQ	50		
1/8 Array	VDD1	850		
	VDD2	2000		
	VDDCA + VDDQ	50		

AC Timing

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Definitions and Calculations

Symbol	Description	Calculation	Notes
$t_{CK(avg)}$ and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit tCK(avg) represents the actual clock average tCK(avg) of the input clock under operation. Unit nCK represents one clock cycle of the input clock,	$t_{CK(avg)} = \left(\sum_{j=1}^{N} t_{CK_j}\right)/N$ Where $N = 200$	
$t_{CK(abs)}$	The absolute clock period, as measured from one rising		
$t_{CH(avg)}$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left(\sum_{j=1}^{N} t_{CH_j}\right)/(N \times t_{CK(avg)})$ Where $N = 200$	
$t_{CL(avg)}$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left(\sum_{j=1}^{N} t_{CL_j}\right)/(N \times t_{CK(avg)})$ Where $N = 200$	
$t_{JIT(per)}$	The single-period jitter defined as the largest deviation of any signal tCK from $t_{CK(avg)}$.		
$t_{JIT(per),act}$	The actual clock jitter for a given system.		
$t_{JIT(per),allowed}$	The specified clock period jitter allowance.		
$t_{JIT(cc)}$	The absolute difference in clock periods between two consecutive clock cycles. $t_{JIT(cc)}$ defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = max\ of \left\{t_{CK_{i+1}} - t_{CK_i}\right\}$	
$t_{ERR(nper)}$	The cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j}\right) - (n \times t_{CK(avg)})$	
$t_{ERR(nper),act}$	The actual cumulative error over n cycles for a given system.		
$t_{ERR(nper),allowed}$	The specified cumulative error allowance over n cycles.		
$t_{ERR(nper),min}$	The minimum $t_{ERR(nper)}$.	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	
$t_{ERR(nper),max}$	The maximum $t_{ERR(nper)}$.	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	
$t_{JIT(duty)}$	Defined with tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from $t_{CH(avg)}$. tCL jitter is the largest deviation of any single tCL from $t_{CL(avg)}$.	$t_{JIT(duty)} = min/max\ of\ [t_{JIT(CH)}, t_{JIT(CL)}]$ Where: $t_{JIT(CH)} = [t_{CH_i} - t_{CH(avg)}\ where\ i = 1\ to\ 200]$ $t_{JIT(CL)} = [t_{CH_i} - t_{CH(avg)}\ where\ i = 1\ to\ 200]$ $t_{JIT(CL)} = [t_{CH_i} - t_{CH(avg)}\ where\ i = 1\ to\ 200]$	

REFRESH Requirements by Device Density

Symbol	Parameter	2Gb	Unit
	Number of banks	8	
tREFW	Refresh window: TCASE ≤ 85°	32	ms
tREFW	Refresh window: 85°C < TCASE ≤ 105°C	8	ms
R	Required number of REFRESH commands (MIN)	8192	
tREFI	Average time between REFRESH commands (for reference only) TCASE ≤ 85°C	3.9	us
tREFIpb		0.4875	us
tRFCab	Refresh cycle time	130	ns
tRFCpb	Per-bank REFRESH cycle time	60	ns
tREFBW	Burst REFRESH window = 4 × 8 × tRFCab	4.16	us

LPDDR2 AC Timing Table

V_{DD2},V_{DDQ},V_{DDCA}=1.14~1.30V, V_{DD1}=1.70~1.95V

Symbol	Parameter	Min/ Max	Min t_{CK}	Speed Grade			Unit 800
				1066	800	667	
Clock parameters							
f	Frequency	max		533	400	333	MHz
^{t}CK	Clock cycle time	min		1.875	2.5	3	ns
		max		100			ns
^{t}CH	CK high-level width	min		0.45			^{t}CK
		max		0.55			^{t}CK
^{t}CL	CK low-level width	min		0.45			^{t}CK
		max		0.55			^{t}CK
^{t}HP	Half-clock period	=		min(^{t}CH, ^{t}CL)			^{t}CK
^{t}CK(avg)	Average Clock period	min		1.875	2.5	3	^{t}CK(avg)
		max		100			
^{t}CH(avg)	Average HIGH pulse width	min		0.45			^{t}CK(avg)
		max		0.55			
^{t}CL(avg)	Average LOW pulse width	min		0.45			^{t}CK(avg)
		max		0.55			
tCK(abs)	Absolute clock period	min		*tCK(avg)* MIN ± *tJIT(per)* MIN			ps
tCH(abs)	Absolute clock HIGH pulse width	min		0.43			^{t}CK(avg)
tCL(abs)	Absolute clock LOW pulse width	min		0.43			^{t}CK(avg)

Symbol	Parameter	Min/ Max	Min t_{CK}	Speed Grade			Unit
				1066	800	667	
tJIT(per), allowed	Clock period jitter (with supported jitter)	min		-90	-100	-110	ps
		max		90	100	110	ps
tERR(2per), allowed	Cumulative errors across 2 cycles	min		-132	-147	-162	ps
		max		132	147	162	ps
tERR(3per), allowed	Cumulative errors across 3 cycles	min		-157	-175	-192	ps
		max		157	175	192	ps
tERR(4per), allowed	Cumulative errors across 4 cycles	min		-175	-194	-214	ps
		max		175	194	214	ps
tERR(5per), allowed	Cumulative errors across 5 cycles	min		-188	-209	-230	ps
		max		188	209	230	ps
tERR(6per), allowed	Cumulative errors across 6 cycles	min		-200	-222	-244	ps
		max		200	222	244	ps
tERR(7per), allowed	Cumulative errors across 7 cycles	min		-209	-232	-256	ps
		max		209	232	256	ps
tERR(8per), allowed	Cumulative errors across 8 cycles	min		-217	-241	-266	ps
		max		217	241	266	ps
tERR(9per), allowed	Cumulative errors across 9 cycles	min		-224	-249	-274	ps
		max		224	249	274	ps
tERR(10per), allowed	Cumulative errors across 10 cycles	min		-231	-257	-282	ps
		max		231	257	282	ps
tERR(11per), allowed	Cumulative errors across 11 cycles	min		-237	-263	-289	ps
		max		237	263	289	ps
tERR(12per), allowed	Cumulative errors across 12 cycles	min		-242	-269	-296	ps
		max		242	269	296	ps
tERR(nper), allowed	Cumulative errors across *n* = 13, 14, 15…, 49, 50 cycles	min		*tERR(nper),allowed* MIN = (1 +0.68ln(n)) × *tJIT(per),allowed* MIN			ps
		max		*tERR (nper), allowed* MAX=(1 +0.68ln(n)) × *tJIT(per),allowed MAX*			ps
ZQ calibration parameters							
t_{ZQinit}	Calibration initialization Time	min		1			us
t_{ZQCL}	Long (Full) Calibration Time	min	6	360			ns
t_{ZQCS}	Short Calibration Time	min	6	90			ns
$t_{ZQreset}$	Calibration Reset Time	min	3	50			ns

Symbol	Parameter	Min/ Max	Min	Speed Grade	Unit

			t_{CK}	1066	800	667	
Read parameters							
t_{DQSCK}	DQS output access time from CK, /CK	min		2500			ps
		max		5500			ps
$t_{DQSCKDS}$	DQSCK Delta Short	max		330	450	540	ps
$t_{DQSCKDM}$	DQSCK Delta Medium	max		680	900	1050	ps
$t_{DQSCKDL}$	DQSCK Long	max		920	1200	1400	ps
t_{DQSQ}	DQS-DQ skew, DQS to last DQ valid, per group, per access	max		200	240	280	ps
t_{QHS}	Data Hold Skew Factor	max		230	280	340	ps
t_{QSH}	DQS output HIGH pulse width	min		t_{CH} - 0.05			t_{CK}
t_{QSL}	DQS output LOW pulse width	min		t_{CL} - 0.05			t_{CK}
t_{QHP}	Data half period	min		MIN (t_{QSH}, t_{QSL})			t_{CK}
t_{QH}	DQ-DQS hold, DQS to first DQ to go non-valid, per access	min		t_{HP} - t_{QHS}			ps
t_{RPRE}	READ Preamble	min		0.9			t_{CK}
t_{RPST}	READ postamble	min		t_{CL} - 0.05			t_{CK}
$t_{LZ(DQS)}$	DQS Low-Z from CK	min		$t_{DQSCK_{min}}$ - 300			ps
$t_{LZ(DQ)}$	DQ Low-Z from CK	min		t_{DQSCK}(MIN) - (1.4 × t_{QHS}(MAX))			ps
$t_{HZ(DQS)}$	DQS High-Z from CK	max		$t_{DQSCK_{max}}$ - 100			ps
$t_{HZ(DQ)}$	DQ High-Z from CK	max		t_{DQSCK}(MAX) + (1.4 × t_{DQSQ}(MAX))			ps
Write parameters							
t_{DH}	DQ and DM input hold time (V_{REF} based)	min		210	270	350	ps
t_{DS}	DQ and DM input setup time (V_{REF} based)	min		210	270	350	ps
t_{DIPW}	DQ and DM input pulse width	min		0.35			t_{CK}
t_{DQSS}	Write command to 1st DQS latching transition	min		0.75			t_{CK}
		max		1.25			t_{CK}
t_{DQSH}	DQS input high-level width	min		0.4			t_{CK}
t_{DQSL}	DQS input low-level width	min		0.4			t_{CK}
t_{DSS}	DQS falling edge to CK setup time	min		0.2			t_{CK}
t_{DSH}	DQS falling edge hold time from CK	min		0.2			t_{CK}
t_{WPST}	Write postamble	min		0.4			t_{CK}
t_{WPRE}	Write preamble	min		0.35			t_{CK}
CKE input parameters							
t_{CKE}	CKE min. pulse width (high and low)	min	3	3			t_{CK}
t_{ISCKE}	CKE input set-up time	min		0.25			t_{CK}

Symbol	Parameter	Min/ Max	Min	Speed Grade	Unit

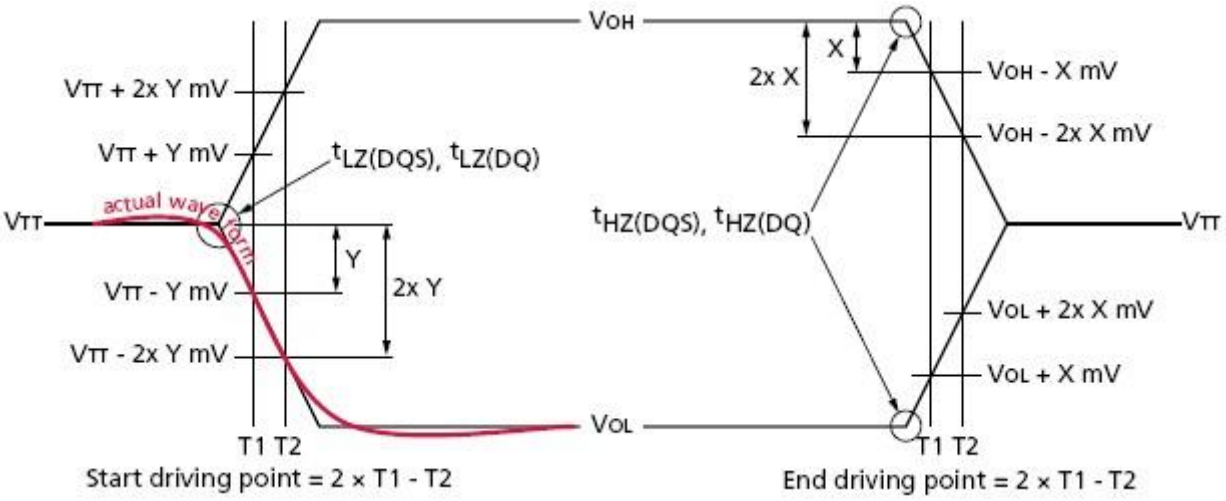
			t_{CK}	1066	800	667	
t_{IHCKE}	CKE input hold time	min		0.25			t_{CK}
Command / Address input parameters							
t_{IH}	Address and Control input hold time	min		220	290	370	ps
t_{IS}	Address and Control input setup time	min		220	290	370	ps
t_{IPW}	Address and Control input pulse width	min		0.4			t_{CK}
Mode register parameters							
t_{MRR}	MODE Register Read command period	min	2	2			t_{CK}
t_{MRW}	MODE Register Write command period	min	5	5			t_{CK}
SDRAM core parameters							
RL	Read Latency	min	3	8	6	5	t_{CK}
WL	Write Latency	min	1	4	3	2	t_{CK}
tCKESR	CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	min	3	15			ns
t_{XSR}	Exit SELF REFRESH to first valid command (min)	min	2	$t_{RFC_{AB}}$ +10			ns
t_{XP}	Exit power-down mode to first valid command	min	2	7.5			ns
t_{DPD}	Minimum Deep Power-Down time	min	-	500			us
t_{FAW}	Four-Bank Activate Window	min	8	50			ns
t_{WTR}	Internal WRITE to READ command delay	min	2	7.5			ns
t_{RC}	ACTIVE to ACTIVE command period	min		t_{RAS} + $t_{RP_{AB}}$ (with all-bank Precharge) t_{RAS} + $t_{RP_{PB}}$(with per-bank Precharge)			ns
t_{CCD}	CAS-to-CAS delay	min	2	2			t_{CK}
t_{RTP}	Internal READ to PRECHARGE command delay	min	2	7.5			ns
t_{RCD}	RAS-to-CAS delay	min	3	15			ns
t_{RAS}	Row Active Time	min	3	42			ns
		max	-	70			us
t_{WR}	Write recovery time	min	3	15			ns
$t_{RP_{PB}}$	PRECHARGE command period (single bank)	min	3	15			ns
$t_{RP_{PAB}}$	PRECHARGE command period (all banks – 8bnak)	min	3	18			ns
t_{RRD}	ACTIVE *bank-a* to ACTIVE *bank-b* command	min	2	10			ns
Temperature derating							
tDQSCK (derated)	tDQSCK derating	max		5620	6000	6000	ps
tRCD (derated)	Core timing temperature deration	min		tRCD + 1.875			ns
tRC (derated)		min		tRC + 1.875			ns
tRAS (derated)		min		tRAS + 1.875			ns
tRP (derated)		min		tRP + 1.875			ns

Symbol	Parameter	Min/ Max	Min	Speed Grade	Unit

			t_{CK}	1066	800	667	
tRRD (derated)	Core timing temperature deration	min		tRRD + 1.875			ns
Boot parameters (10MHz ~ 55MHz)							
t_{CKb}	Clock cycle time	min		18			ns
		max		100			ns
t_{ISCKEb}	CKE input setup time	min		2.5			ns
t_{IHCKEb}	CKE input hold time	min		2.5			ns
t_{ISb}	Input setup time	min		1150			ps
t_{IHb}	Input hold time	min		1150			ps
t_{DQSCKb}	Access window of DQS from CK, /CK	min		2.0			ns
		max		10.0			ns
t_{DQSQb}	DQS-DQ skew	max		1.2			ns

Notes:

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to VREF.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
7. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



Data Out measurement reference points

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS, /DQS.

8. Measured from the point when DQS, /DQS begins driving the signal to the point when DQS, /DQS begins driving the first rising strobe edge.
9. Measured from the last falling strobe edge of DQS, /DQS to the point when DQS, /DQS finishes driving the signal.
10. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK, /CK crossing.
11. CKE input hold time is measured from CK, /CK crossing to CKE reaching a HIGH/LOW voltage level.
12. Input set-up/hold time for signal (CA[9:0], /CS).
13. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
14. The LPDDR device will set some mode register default values upon receiving a RESET (MRW) command as specified in Mode Register Definition.
15. The output skew parameters are measured with default output impedance settings using the reference load.
16. The minimum tCK column applies only when tCK is greater than 6ns.
17. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-code.

Revision History

Date	Rev.	Description
2017-04-24	1.0	New revision