Constant On-Time Buck Converter
With Integrated Linear Regulator

FEATURES AND BENEFITS

- 2 MHz switching frequency
- Adjustable soft start timer
- Watchdog input
- Power-on reset output
- Adjustable buck and linear regulators
- Enable input
- 6 to 50 V supply voltage range
- Overcurrent protection
- Undervoltage lockout (UVLO)
- Thermal shutdown protection

APPLICATIONS:

AUTOMOTIVE ("K" VERSION)
- Power steering control units
- Transmission control units
- Lighting control units
- Infotainment
- Cluster
- Centerstack
- Other body control

COMMERCIAL ("E" VERSION)
- Photo and inkjet printers
- Industrial controls
- Distributed power systems
- Networking applications
- Point-of-sale
- Security systems

PACKAGE:

16-pin eTSSOP
with exposed thermal pad
(suffix LP)
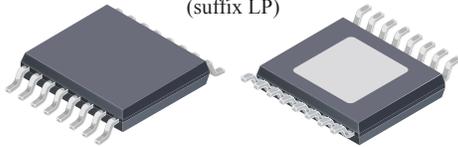
Not to scale

DESCRIPTION

The A4402 is a dual-output regulator, combining in a single package a constant on-time buck regulator and a linear regulator (LDO)—each with adjustable output voltages. It is ideal for applications that require two regulated voltages, such as in microcontroller- or DSP-based applications requiring core and I/O voltage rails.

The buck regulator output supplies the adjustable linear regulator to reduce power dissipation and increase overall efficiency. The switching regulator is capable of operating above 2 MHz, allowing the use of small low value inductors and capacitors while avoiding sensitive EMI frequency bands such as AM radio in automotive applications.

Protection features include undervoltage lockout and thermal shutdown. In case of a shorted load, each regulator features overcurrent protection.

The device has an integrated power-on reset with adjustable delay to monitor LDO output voltage and provide a signal that can be used to reset a DSP or microcontroller. It also includes a watchdog circuit.

The A4402 is provided in a 16-pin eTSSOP, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application

Efficiency vs. Output Current
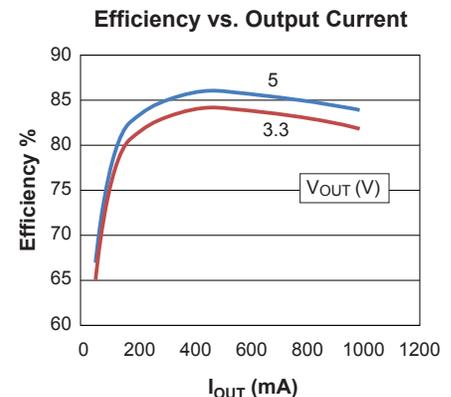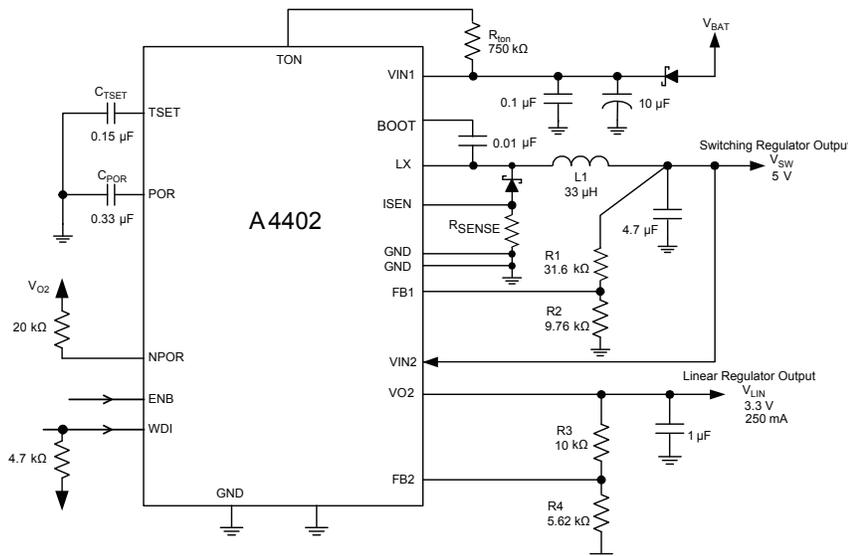
Data is for reference only. Efficiency data from circuit shown in left panel.

FUNCTIONAL BLOCK DIAGRAM

C_{TSET} 0.15 µF — TSET

C_{POR} 0.33 µF — POR

WDI

ENB

V_{O2} 20 kΩ — NPOR

WDI 4.7 kΩ

Soft Start Ramp Generator / Watchdog Timer

FAULT

V_{FB2}

Internal Regulator — V_{REG}, V_{REF}

ENB VIN1 VIN2

Switch PWM Control

Switch Disable

TSD

V_{REF}

TON BOOT Boot Charge

VIN1

LX

ISEN

GND
GND

FB1

VIN2 — V_{SW}

VO2

FB2

V_{REG} V_{REF}

0.01 µF

R_{ton} 750 kΩ — V_{BAT}

0.1 µF 10 µF

L1 33 µH — V_{SW} 5 V

R_{SENSE}

4.7 µF

R1 31.6 kΩ
R2 9.76 kΩ

V_{LIN} 3.3 V 250 mA

1 µF

R3 10 kΩ

R4 5.62 kΩ

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115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

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PINOUT DIAGRAM AND TERMINAL LIST

```
TON   1            16  ENB
GND   2            15  VIN1
FB2   3            14  GND
VIN2  4            13  LX
VO2   5    PAD     12  BOOT
WDI   6            11  ISEN
TSET  7            10  POR
NPOR  8             9  FB1
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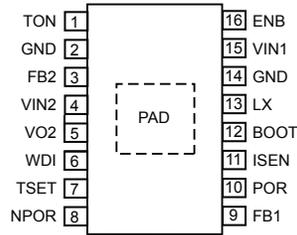
LP-16 PINOUT DIAGRAM

TERMINAL LIST TABLE

Number	Name	Function
1	TON	On time setting terminal
2	GND	Ground
3	FB2	Feedback for V_{LIN}
4	VIN2	Input voltage 2
5	VO2	Regulator 2 output
6	WDI	Watchdog input
7	TSET	Soft start and watchdog timing capacitor terminal
8	NPOR	Fault output
9	FB1	Feedback for V_{SW}
10	POR	POR delay
11	ISEN	Current sense, limit setting for switching regulator, connect to GND through series resistor
12	BOOT	Boot node for LX
13	LX	Switching regulator output
14	GND	Ground
15	VIN1	Input voltage 1
16	ENB	Enable input
–	PAD	Exposed thermal pad

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115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
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ELECTRICAL CHARACTERISTICS[1]: Valid for Temperature Range E version at T$_J$ = 25°C and for Temperature Range K version at T$_J$ = –40°C to 150°C, V$_{IN1}$ = 6 to 50 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Quiescent Current	I$_{IN(Q)}$	V$_{ENB}$ = 5 V, I$_{OUT}$ = I$_{SW}$ + I$_{LIN}$ = 0 mA, 13.5 V < V$_{IN1}$ < 50 V	1	–	6	mA
		V$_{ENB}$ = 0 V, 13.5 V < V$_{IN1}$ < 18V, I$_{OUT}$ = I$_{SW}$ + I$_{LIN}$ = 0mA	–	–	1	µA
ENB Logic Input Voltage	V$_{ENB}$	V$_{ENB}$ rising	2.0	2.28	2.56	V
ENB Hysteresis	V$_{ENBHYS}$		–	100	–	mV
ENB Logic Input Current [2]	I$_{ENB}$	High input level, V$_{ENB}$ = 3 V	–	–	100	µA
		Low input level, V$_{ENB}$ < 0.4 V	–2	–	2	µA
LINEAR REGULATOR						
Feedback Voltage	V$_{FB2}$	1 mA < I$_{O2}$ < 250 mA, 3.3 V < V$_{IN2}$ < 5 V	1.156	1.180	1.204	V
V$_{O2}$ Undervoltage Lockout Threshold	V$_{O2UVLO}$	V$_{O2}$ rising based on FB voltage	0.896	0.944	0.990	V
V$_{O2}$ Undervoltage Lockout Hysteresis	V$_{O2UVHYS}$		30	50	70	mV
Feedback Input Bias Current [2]	I$_{FB2}$		–100	100	400	nA
Current Limit	I$_{O2}$		250	–	350	mA
SWITCHING REGULATOR						
Feedback Voltage	V$_{FB1}$	I$_{OUT}$ = I$_{SW}$+ I$_{LIN}$ = 1 mA to 1.0 A, 8 V < V$_{IN1}$ < 18 V	1.139	1.180	1.221	V
Feedback Input Bias Current	I$_{FB1}$	V$_{IN1}$ = 6 V	–400	–100	100	nA
Switcher On Time	t$_{on}$	V$_{IN1}$ = 19.25 V, R$_{ton}$ = 750 kΩ	450	640	830	ns
		V$_{IN1}$ = 13.5 V, R$_{ton}$ = 750 kΩ	165	230	300	ns
		V$_{IN1}$ = 8 V, R$_{ton}$ = 750 kΩ	1050	1480	1925	ns
t$_{on}$ Low Voltage Threshold	V$_{PL}$	V$_{IN1}$ rising	8.1	9	9.9	V
t$_{on}$ High Voltage Threshold	V$_{PH}$	V$_{IN1}$ rising	15.75	17.5	19.25	V
Changeover Hysteresis	V$_{HYS}$		–	250	–	mV
Minimum On-Time	t$_{onmin}$		80	–	–	ns
Minimum Off-Time	t$_{offmin}$		130	–	–	ns
Buck Switch On-Resistance	R$_{DS(on)}$	T$_J$ = 25°C, I$_{LOAD}$ = 1 A	–	400	–	mΩ
		T$_J$ = 125°C, I$_{LOAD}$ = 1 A	–	650	–	mΩ
ISEN Voltage	V$_{ISEN}$		–150	–250	–350	mV
Valley Current Limit Threshold	I$_{lim}$	R$_{SENSE}$ = 0.27 Ω	–	740	–	mA
		6 V < V$_{IN1}$ < 8 V	–	–	550	mA
PROTECTION CIRCUITRY						
NPOR Output Voltage	V$_{NPOR}$	I$_{NPOR}$ = 1 mA	–	–	400	mV
NPOR Leakage Current	I$_{NPOR}$	V$_{NPOR}$ = 5.5 V	–	–	1.5	µA
NPOR Reset	V$_{NPORRESET}$	20 kΩ pullup connected to VOUT2	–	–	0.7	V
Thermal Shutdown Threshold	T$_{JTSD}$	T$_J$ rising	–	170	–	°C
Thermal Shutdown Hysteresis	T$_{JTSDHYS}$		–	15	–	°C

Continued on the next page...

ELECTRICAL CHARACTERISTICS [1] (continued): Valid for Temperature Range E version at T_J = 25°C and for Temperature Range K version at T_J = –40°C to 150°C, V_{IN1} = 6 to 50 V (unless otherwise noted)

| Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TIMING CIRCUITRY						
TSET Current, Watchdog Mode	$I_{TSETWDI}$	NPOR = high	7	10	14	µA
TSET Valley Voltage, Watchdog Mode	V_{TRIP}		–	1.2	–	V
TSET Reset Voltage, Watchdog Mode	V_{RESET}		–	0.48	–	V
WDI Frequency	f_{WDI}		–	–	100	kHz
WDI Duty Cycle	DC_{WDI}		10	–	90	%
WDI Logic Input	$V_{WDI(0)}$		V_{IN2} × 0.55	–	–	V
WDI Logic Input Current [2]	I_{WDI}	V_{WDI} = 0 to 5 V	–20	< 1.0	20	µA
WDI Input Hysteresis	V_{WDIHYS}		–	300	–	mV
TSET Current, Soft Start Mode	I_{TSETSS}	NPOR = low	14	20	26	µA
POR Current	I_{POR}		3.92	5.60	7.28	µA

[1] Temperature Range E version tested at T_J = 25°C with performance from –40°C to 85°C guaranteed by design and characterization.
[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified pin.

Allegro MicroSystems, LLC
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
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Power-Up and Power-Down Timing Diagrams

Using ENB

ENB

VIN1

18 V

6 V

t_{ss}

V_{SW}

V_{O2}

UVLO Rising

UVLO Falling

UVLO Rising

NPOR

t_{por}

t_{por}

Using VIN1

ENB

VIN1

t_{ss}

t_{ss}

V_{SW}

V_{O2}

UVLO Rising

UVLO Falling

UVLO Rising

NPOR

t_{por}

t_{por}

VPOR

VCTSET
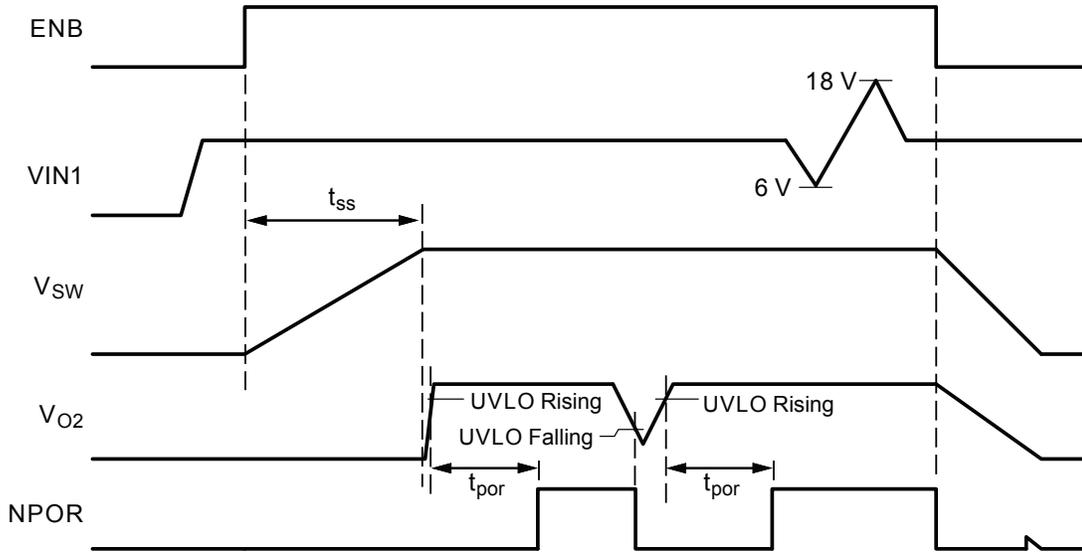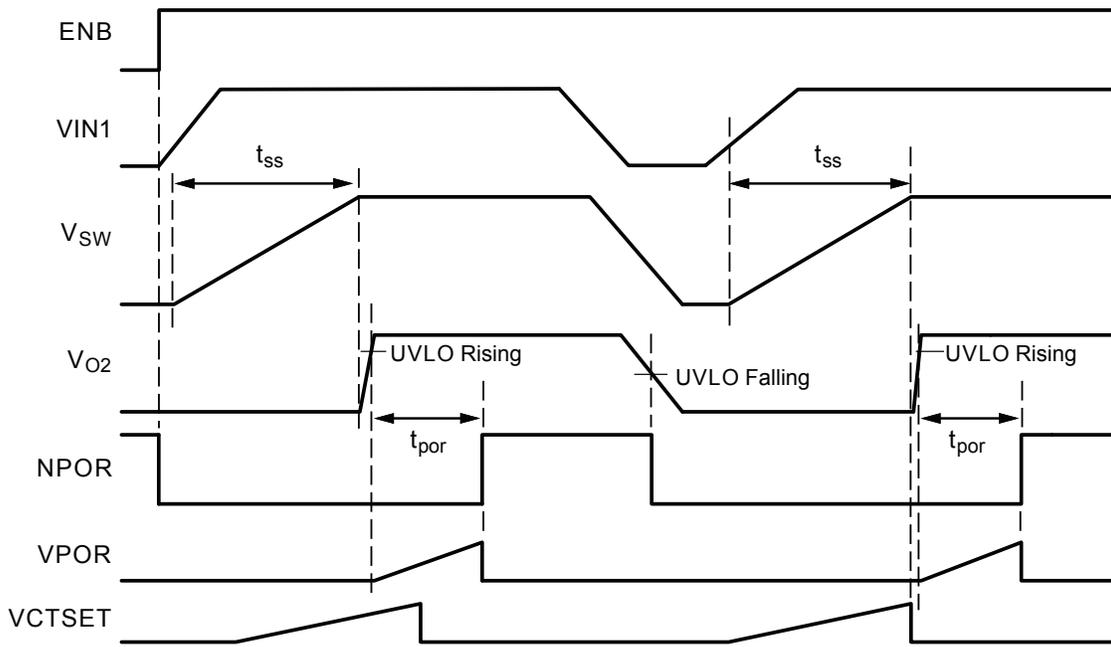
Watchdog Timing Diagram

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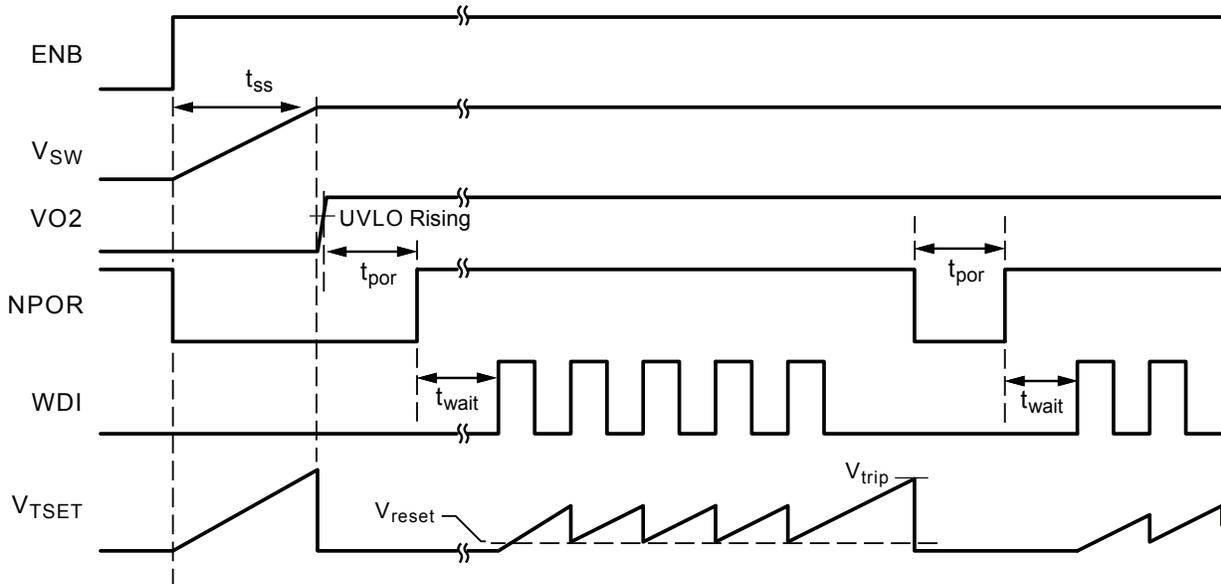
FUNCTIONAL DESCRIPTION

Basic Operation

The A4402 contains a fixed on-time, adjustable voltage buck switching regulator with valley sensing current mode control, and an adjustable linear regulator designed to run off the buck regulator output. The constant on-time converter maintains a constant output frequency because the on-time is inversely proportional to the supply voltage. As the input voltage decreases, the on-time is increased, maintaining a relatively constant period. Valley mode current control allows the converter to achieve very short on-times because current is measured during the off-time.

The device is enabled via the ENB input. When the ENB pin is pulled high, the converter starts-up under the control of an adjustable soft start routine whose ramp time is controlled by an external capacitor.

Under light load conditions, the switch enters pulse-skipping mode to ensure regulation is maintained. This effectively changes the switcher frequency. The frequency also is affected when the switcher is operating in discontinuous mode. In order to maintain a wide input voltage range, the switcher period is extended when either the minimum off-time at low V_{IN1}, is reached or the minimum on-time at high V_{IN1}.

Switcher Overcurrent Protection

The converter uses pulse-by-pulse valley current limiting, which operates when the current through the sense resistor rises to V_{ISEN}. During an overload condition, the switch is turned on for a period determined by the constant on-time circuitry. The switch off-time is extended until the current decays to the current limit value set by the selection of the sense resistor, at which point the switch turns on again. Because no slope compensation is required in this control scheme, the current limit is maintained at a reasonably constant level across the input voltage range.

Figure 1 illustrates how the current is limited during an overload condition. The current decay (period with switch off) is proportional to the output voltage. As the overload is increased, the output voltage tends to decrease and the switching period increases.

VIN1 and VIN2

VIN1 is a high voltage input, designed to withstand 50 V. Bulk capacitance of at least 10 µF should be used to decouple input supply VIN1. The VIN2 input is used to supply the linear regulator and should be connected directly to the output of the switch-

ing regulator when the target for the V_{SW} voltage is between 3 and 5.5 V. For voltages outside of that range, the bias supply for the IC is taken from VIN1 directly and affects overall efficiency.

For applications where the switcher voltage is greater than 5 V, a second supply between 3 and 5.5 V can be used to supply VIN2 bias current and the linear regulator. Note that the current into the VIN2 supply must supply both the i_{dd} bias current and any current load on the linear regulator.

Output Voltage Selection

The output voltage on each of the two regulators is set by a voltage divider off the regulator output, as follows:

$$V_{SW} = V_{FB1} \left(\frac{R1 + R2}{R2} \right) \quad , \quad (1)$$

$$V_{LIN} = V_{FB2} \left(\frac{R3 + R4}{R4} \right) \quad . \quad (2)$$

In order to maintain accuracy on the regulators the equivalent impedance on the FB node (R1 parallel with R2) should be approximately 10 kΩ.
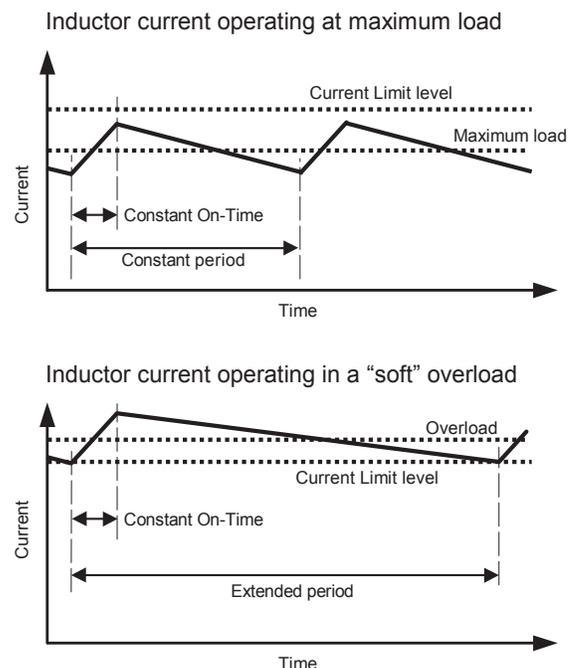
Figure 1. Current limiting during overload

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115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
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FB

Both output regulators use a resistive feedback network to set the output voltage. To prevent introducing noise into the FB network, it is important to keep the total impedance of the FB nodes low enough to prevent noise injection. For commercial applications, it is recommended that the impedances on the FB nodes are less than 50 kΩ. For automotive applications, it is recommended that the total impedance of the FB nodes is less than 25 kΩ.

TSET

The TSET pin serves a dual function by controlling the timing for both the soft start ramp and the WDI input. The current sourced from the TSET pin is dependant on the state of NPOR.

There are two formulas for calculating the time constants. C_{TSET} must be selected so that both the WDI frequency and soft start requirements are met. The formulas for calculating WDI and soft start timing are:

$$t_{WDI} = 7.2 \times 10^4 \times C_{TSET} \quad , \quad \text{and} \tag{3}$$

$$t_{SS} = 6.0 \times 10^4 \times C_{TSET} \quad , \tag{4}$$

where C_{TSET} is the value of the capacitor and the results, t_x, are in s.

Watchdog

The WDI input is used to monitor the state of a DSP or microcontroller. A constant current is driven into the capacitor on TSET, causing the voltage on the TSET pin to ramp upward until, at each rising edge on the WDI input, the ramp is pulled down to V_{RESET}. If no edge is seen on the WDI pin before the ramp reaches V_{TRIP}, the NPOR pin is pulled low.

The watchdog timer is not activated until the WDI input sees one rising edge. If the watchdog timer is not going to be used, the WDI pin should be pulled to ground with a 4.7 kΩ resistor.

Soft Start

During soft start, an internal ramp generator and the external capacitor on TSET are used to ramp the output voltage in a con-

trolled fashion. This reduces the demand on the external power supply by limiting the current that charges the output capacitor and any DC load at startup. Either of the following conditions are required to trigger a soft start:

- ENB pin input rising edge
- Reset of a TSD event

When a soft start event occurs, VO2 is held in the off state until the soft start ramp timer expires. Then the regulator will power up normally. Refer to timing diagrams for details.

BOOT

A bootstrap capacitor is used to provide adequate charge to the NMOS switch. The boot capacitor is referenced to LX and supplies the gate drive with a voltage larger than the supply voltage. The size of the capacitor must be 0.01 µF, X7R type, and rated for at least 25 V.

TON

A resistor from the TON input to VIN1 sets the on-time of the converter for a given input voltage. The formula to calculate the on-time, t_{ON} (ns), is:

$$t_{ON} = \frac{R_{TON}}{V_{IN1}} \times 3.12 \times 10^{-12} + 60 \times 10^{-9} \tag{5}$$

When the supply voltage is between 9 and 17.5 V, the switcher period remains constant, at a level based on the selected value of R_{ton}. At voltages lower than 9 V and higher than 17.5 V, the period is increased by a factor of 3.5.

If a constant period is desired over varying input voltages, it is important to select an on-time that under worst case conditions will not exceed the minimum off-time or minimum on-time of the converter. For reasonable input voltage ranges, the period of the converter can be held constant, resulting in a constant operating frequency over the input supply range.

More information on how to choose R_{ton} can be found in the Application Information section.

ISEN

The sense input is used to sense the current in the diode during the off-time cycle. The value for R_{SENSE} is obtained by the formula:

$$R_{SENSE} = V_{ISEN} / I_{VALLEY} \quad , \quad (6)$$

where I_{VALLEY} is the lowest current measured through the inductor during the off-time cycle.

It is recommended that the current sense resistor be sized so that, at peak output current, the voltage on ISEN does not exceed –0.5 V. Because the diode current is measured when the inductor current is at the valley, the average output current is greater than the I_{VALLEY} value. The value for I_{VALLEY} should be:

$$I_{VALLEY} = I_{OUT(av)} - 0.5\ I_{RIPPLE} + K \quad , \quad (7)$$

where:

$I_{OUT(av)}$ is the average of both output currents,

I_{RIPPLE} is the inductor ripple current, and

K is a guardband margin. The peak current in the switch is then:

$$I_{PEAK} = I_{VALLEY} + I_{RIPPLE} \quad . \quad (8)$$

The valley current must be calculated so that, at the worst-case ripple, the converter can still supply the required current to the load. Further information on how to calculate the ripple current is included in the Application Information section.

ENB

An active high input enables the device. When set low, the device enters sleep mode; all internal circuitry is disabled, and the part draws a maximum of 1 μA.

Thermal Shutdown

When the device junction temperature, T_J, is sensed to be at T_{JTSD}, a thermal shutdown circuit disables the regulator output, protecting the A4402 from damage.

Power-On Reset Delay

The POR function monitors the V_{FB2} voltage and provides a signal that can be used to reset a DSP or microcontroller. A POR event is triggered by either of the following conditions:

- V_{FB2} falls below its UVLO threshold. This occurs if the current limit on either regulator is exceeded, or if the switcher voltage falls due to TSD.

- After a rising edge on the WDI input, the voltage on TSET reaches V_{TRIP}.

An open drain output, through the NPOR pin, is provided to signal a POR event to the DSP or microcontroller. The reset occurs after an adjustable delay, t_{POR}, set by an external capacitor connected to the POR pin. The value of t_{POR} is calculated using the following formula:

$$t_{POR} = 214 \times 10^3 \times C_{POR} \quad , \quad (9)$$

where C_{POR} is the value of the POR capacitor in farads, and t_{POR} is the POR time in seconds.

Shutdown

The buck regulator will shutdown if one of the following conditions is present:

- TSD
- ENB falling edge

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115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
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APPLICATION INFORMATION

Switcher On-Time and Switching Frequency

In order for the switcher to maintain regulation, the energy that is transferred to the inductor during the on-time must be transferred to the output capacitor during the off-time. This relationship must be maintained for stable operation and governs the fundamental operation of a switching regulator. Each component along the current path changes the voltage across the inductor and therefore the energy that is transferred during each cycle. Summing the voltage from V_{IN} to V_{OUT} during each cycle gives a relationship of the voltage across the inductor during the on-time and during the off-time. These terms are represented as V_{ON} and V_{OFF}.

Given a target operating frequency, represent t_{ON} as:

$$t_{ON} = t \times D \tag{10}$$

where t equals $1/f_{SW}$, and D is the duty cycle.

Duty cycle can be represented as the voltage across the inductor during the off-time, divided by the total voltage of the off-time and on-time:

$$D = V_{OFF} / (V_{OFF} + V_{ON}) \tag{11}$$

Next, determine the voltage drops during the on cycle and the off cycle. Figure 2 shows the current path during the on-time and off-time.

Creating voltage summation during each cycle will give equations to represent V_{ON} and V_{OFF}:

$$V_{ON} = V_{IN} - V_{OUT} - (I_{OUT} \times R_L) - (R_{DS} \times I_{OUT}) \tag{12}$$

$$V_{OFF} = V_{OUT} + (I_{OUT} \times R_L) + V_f + (R_S \times I_{OUT}) \tag{13}$$

Now substituting V_{ON} and V_{OFF} into equation 11 gives a complete formula for duty cycle as it relates to the voltage across the inductor:

$$D = \frac{V_{OUT} \times (I_{OUT} \times R_L) + V_f + (R_S \times I_{OUT})}{\begin{array}{c} V_{OUT} + (I_{OUT} \times R_L) + V_f + (R_S \times I_{OUT}) + \\ V_{IN} - V_{OUT} - (I_{OUT} \times R_L) - (R_{DS} + I_{OUT}) \end{array}} \tag{14}$$

The effects of the voltage drop across the inductor resistance and trace resistance do have an effect on the switching frequency. However, the frequency variation due to these factors is small and is covered in the variation of the switcher period, t_{SW}, which is ±25% of the target. Removing these current-dependent terms simplifies the equation:

$$D = \frac{V_{OUT} + V_f + (R_S \times I_{OUT})}{\begin{array}{c} V_{OUT} + V_f + (R_S \times I_{OUT}) + \\ V_{IN} - V_{OUT} - (R_{DS} \times I_{OUT}) \end{array}} \tag{15}$$

Further simplification and grouping of terms yields:

$$D = \frac{V_{OUT} + V_f + (R_S \times I_{OUT})}{V_{IN} + V_f + (R_S \times I_{OUT}) - (R_{DS} \times I_{OUT})} \tag{16}$$

Substitute this simplified expression for duty cycle back into equation 10. The following formula results in the on-time, given a target switching frequency:

$$t_{ON} = \frac{1}{f_{SW}} \left(\frac{V_{OUT} + V_f + (R_S \times I_{OUT})}{V_{IN} + V_f + (R_S \times I_{OUT}) - (R_{DS} \times I_{OUT})} \right) \tag{17}$$

The formulas above describe how t_{ON} changes based on input and load conditions. Because load changes are minimal, and the output voltage is fixed, the dominant factor that effects on-time is the input voltage. The converter is able to maintain a constant period over a varying supply voltage because the on-time is proportional to the input voltage. The current into the TON terminal is derived from a resistor tied to VIN1, which sets the on-time proportional to the supply voltage. Selecting the resistor value, based on the t_{ON} calculated above, is done using the following formula:

$$R_{TON} = \frac{(t_{ON} - 60 \times 10^{-9}) \times V_{IN}}{3.12 \times 10^{-12}} \tag{18}$$

After the resistor is selected and a suitable t_{ON} is found, it must be demonstrated that t_{ON} does not, under worst-case conditions, exceed the minimum on-time or minimum off-time of the converter. The minimum on-time occurs at maximum input voltage and minimum load. The maximum off-time occurs at minimum supply voltage and maximum load. For supply voltages below 9.5 V and above 17 V, refer to the Low and High Voltage Operation section.
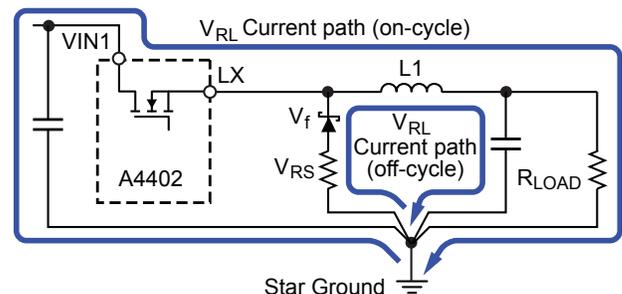

Figure 2. Current limiting during overload

Low and High Voltage Operation

The converter can run at very low input voltages. With a 5 V output, the minimum input supply can be as low as 6 V. When operating at high frequencies, the on-time of the converter must be very short because the available period is short. At high input voltages the converter must maintain very short on-times, while at low input voltages the converter must maintain long off-times. Rather than limit the supply voltage range, the converter solves this problem by automatically increasing the period by a factor of 3.5. With the period extended, the converter will not violate the minimum on-time or off-time. If the input voltage is between 9.5 and 17 V, the converter will maintain a constant period. When calculating worst-case on-times and off-times, make sure to use the multiplier if the supply voltage is between those values.

When operating at voltages below 8 V, additional care must be taken when selecting the inductor and diode. At low voltages the maximum current may be limited due to the IR drops in the current path. When selecting external components for low voltage operation, the IR drops must be considered when determining on-time, so the complete formula should be used to make sure the converter does not violate the timing specification.

Inductor Selection

Choosing the right inductor is critical to the correct operation of the switcher. The converter is capable of running at frequencies above 2 MHz. This makes it possible to use small inductor values, which reduces cost and board area.

The inductor value is what determines the ripple current. It is important to size the inductor so that under worst-case conditions I_{VALLEY} equals I_{AV} minus half the ripple current plus reasonable margin. If the ripple current is too large, the converter will be current limited. Typically peak-to-peak ripple current should be limited to 20% to 25% of the maximum average load current.

Worst-case ripple current occurs at maximum supply voltage. After calculating the duty cycle, DC, for this condition, the ripple current can be calculated. First to calculate DC:

$$ DC = \frac{V_{SW} + V_f + (R_{SENSE} \times I_{PEAK})}{V_{IN1}(max) + V_f + (R_{SENSE} \times I_{PEAK})} \qquad . \qquad (19)$$

Using the duty cycle, a ripple current can be calculated using the following formula:

$$ L = \frac{V_{IN1} - V_{OUT}}{I_{RIPPLE}} \times DC \times \frac{1}{f_{SW}(min)} \qquad , \qquad (20)$$

where I_{RIPPLE} is 25% of the maximum load current, and $f_{SW}(min)$ is the minimum switching frequency (nominal frequency minus 25%). For the example used above, a 1 A converter with a supply voltage of 13.5 V was the design objective. The supply voltage can vary by ±10%. The output voltage is 5 V, V_f is 0.5 V, V_{SENSE} is 0.15, and the desired frequency is 2.0 MHz. The duty cycle is calculated to be 36.45%. The worst-case frequency is 2 MHz minus 20% or 1.6 MHz. Using these numbers in the above formula shows that the minimum inductance for this converter is 9.6 µH.

Output Capacitor

The converter is designed to operate with a low-value ceramic output capacitor. When choosing a ceramic capacitor, make sure the rated voltage is at least 3 times the maximum output voltage of the converter. This is because the capacitance of a ceramic decreases as they operate closer to their rated voltage. It is recommended that the output be decoupled with a 10 µF, X7R ceramic capacitor. Larger capacitance may be required on the outputs if load surges dramatically influence the output voltage.

Output ripple is determined by the output capacitance and the effects of ESR and ESL can be ignored assuming recommended layout techniques are followed. The output voltage ripple is approximated by:

$$ V_{RIPPLE} = \frac{I_{RIPPLE}}{4 \times f_{SW} \times C_{OUT}} \qquad . \qquad (21)$$

Input Capacitor

The value of the input capacitance affects the amount of current ripple on the input. This current ripple is usually the source of supply-side EMI. The amount of interference depends on the impedance from the input capacitor and the bulk capacitance located on the supply bus. Adding a small value, 0.1 µF, ceramic capacitor as close to the input supply pin as possible can reduce EMI effects. The small capacitor will help reduce high frequency transient currents on the supply line. If further filtering is needed it, is recommended that two ceramic capacitors be used in parallel to further reduce emissions.

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Rectification Diode

The diode conducts the current during the off-cycle. A Schottky diode is needed to minimize the forward drop and switching losses. In order to size the diode correctly, it is necessary to find the average diode conduction current using the formula below:

$$I_{D(av)} = I_{LOAD} \times (1 - DC(min)) \quad , \qquad (22)$$

where $DC(min)$ is defined as:

$$DC(min) = \frac{V_{SW} + V_f}{V_{IN1} + V_f} \quad , \qquad (23)$$

where V_{IN1} is the maximum input voltage and V_f is the maximum forward voltage of the diode.

Average power dissipation in the diode is:

$$P_{D(diode)} = I_{LOAD(av)} \times DC(min) \times V_f \quad , \qquad (24)$$

The power dissipation in the sense resistor must also be considered using I^2R and the minimum duty cycle.

PCB Layout

The board layout has a large impact on the performance of the device. It is important to isolate high current ground returns, to minimize ground bounce that could produce reference errors in the device. The method used to isolate power ground from noise sensitive circuitry is to use a star ground. This approach makes sure the high current components such as the input capacitor, output capacitor, and diode have very low impedance paths to each other. Figure 3 illustrates the technique.

The ground from each of the components should be very close to each other and be connected on the same surface as the components. Internal ground planes should not be used for the star ground connection, as vias add impedance to the current path.

In order to further reduce noise effects on the PCB, noise sensitive traces should not be connected to internal ground planes. The feedback network from the switcher output should have an independent ground trace that goes directly to the exposed pad underneath the device. The exposed pad should be connected to internal ground planes and to any exposed copper used for heat dissipation. If the grounds from the device are also connected directly to the exposed pad the ground reference from the feedback network will be less susceptible to noise injection or ground bounce.

To reduce radiated emissions from the high frequency switching nodes, it is important to have an internal ground plane directly under the LX node. The plane should not be broken directly under the node as the lowest impedance path back to the star ground would be directly under the signal trace. If another trace does break the return path, the energy will have to find another path, which is through radiated emissions.
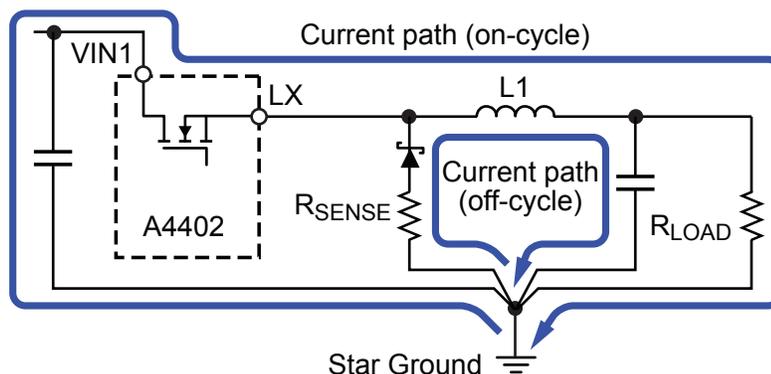

Figure 3. Star Ground Connection

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PCB LAYOUT DIAGRAM
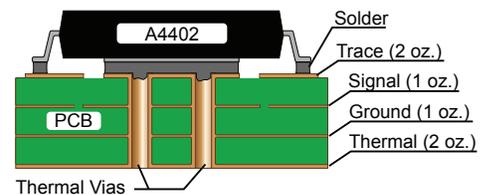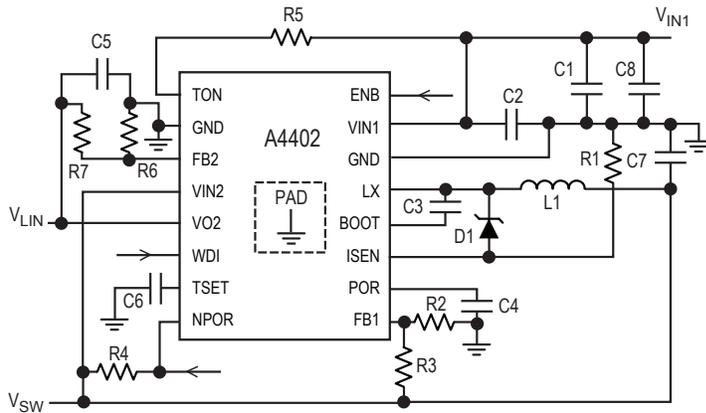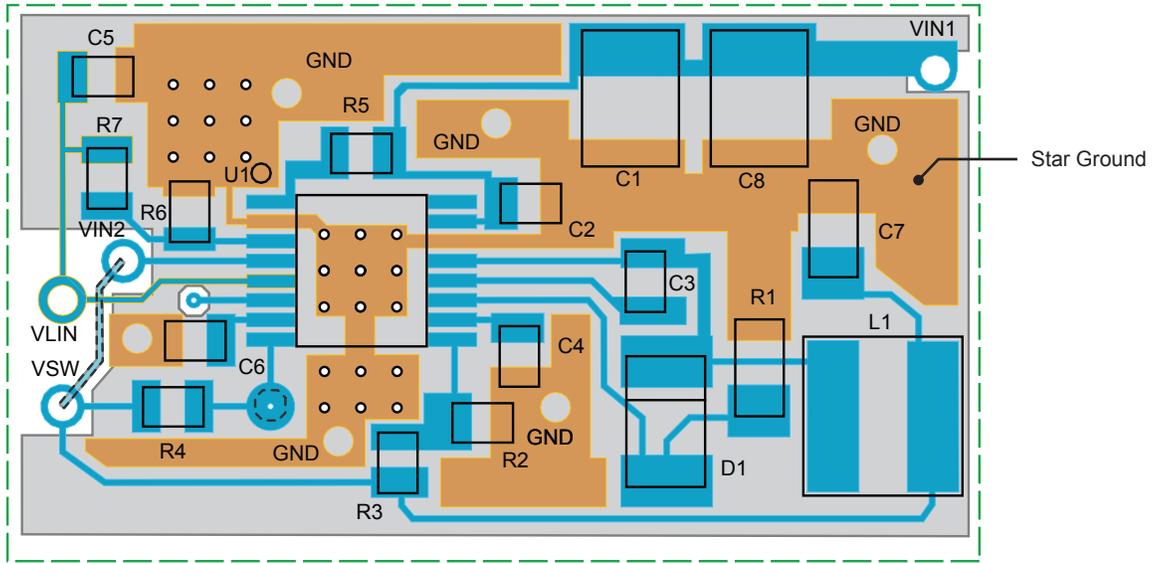
PIN CIRCUIT DIAGRAMS

Power Terminals

LX

54 V

GND   GND

BOOT V_{IN1}

10 V

10 V

LX

VO2 V_{IN2}

GND

TON V_{IN1}

GND

VIN1

54 V

GND

Logic Terminals

VIN2
FB1
FB2
WDI
TSET
NPOR
POR
ISEN
ENB

7 V

GND   GND

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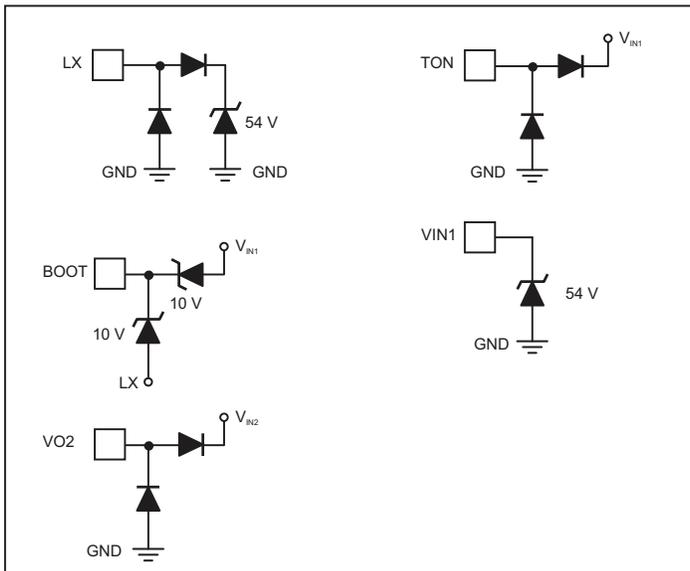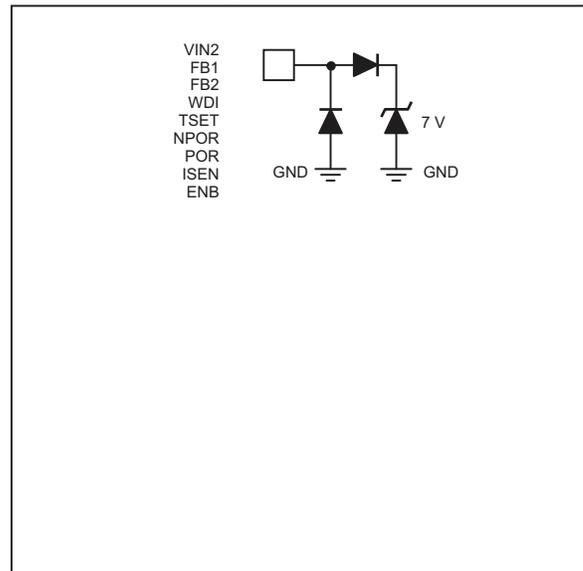
**Package LP, 16-Pin eTSSOP
with Exposed Thermal Pad**

5.00 ±0.10
16
3.00
4.40 ±0.10   6.40 ±0.20
1   2
3.00

16X
⬓ 0.10 C
0.25 +0.05 −0.06
0.65
SEATING PLANE
C
1.20 MAX
0.15 MAX

4° ±4
0.15 +0.05 −0.06
0.60 ±0.15
(1.00)
0.25
SEATING PLANE
GAUGE PLANE

0.45
16
0.65
1.70
3.00   6.10
1   2
3.00
⚠C PCB Layout Reference View
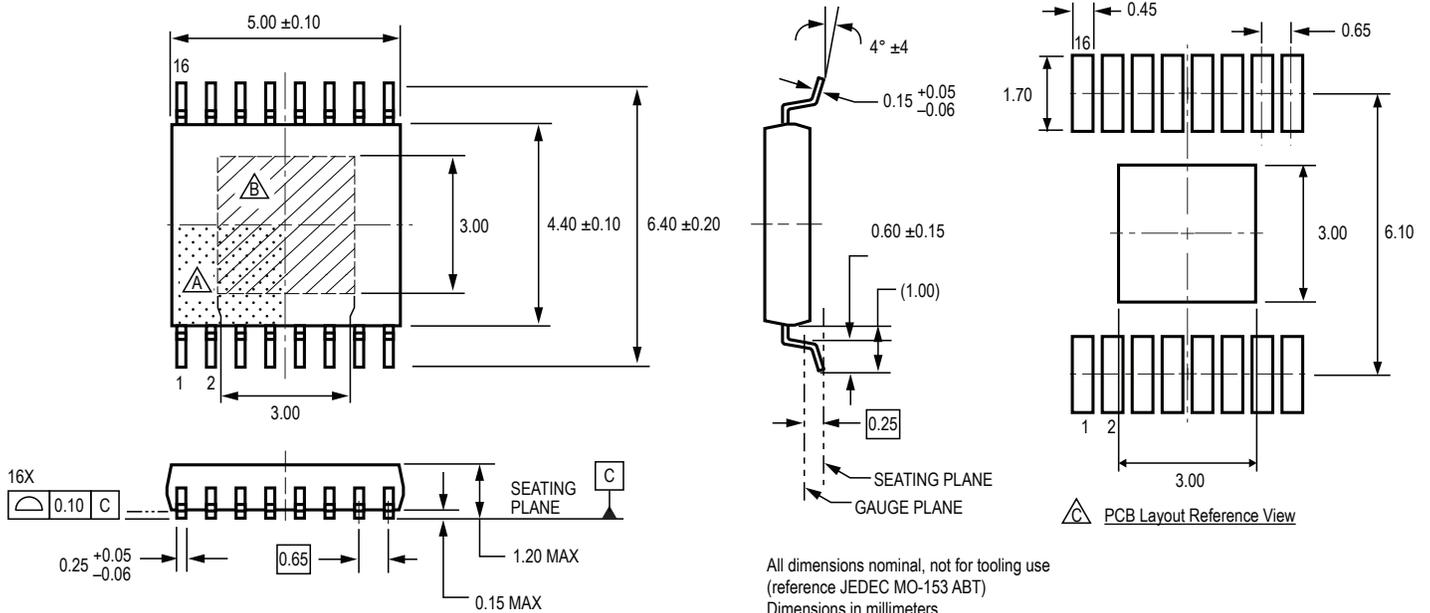
All dimensions nominal, not for tooling use
(reference JEDEC MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

⚠A Terminal #1 mark area

⚠B Exposed thermal pad (bottom surface)

⚠C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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Worcester, Massachusetts 01615-0036 U.S.A.
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Revision History

Number	Date	Description
10	August 27, 2013	Update TON description
11	March 26, 2014	Revised Functional Description and Pin Circuits
12	November 28, 2017	Corrected Equations 3 and 4 on page 10

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